New Fault Models And Efficient BIST Algorithms For Dual-Portmemories

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Summary

The testability problem of dual-port memories is investigated. A functional model is defined, and architectural modifications to enhance the testability of such chips are described. These modifications allow multiple access of memory cells for increased test speed with minimal overhead on both silicon area and device performance. New fault models are proposed, and efficient O(n) test algorithms are described for both the memory array and the address decoders. The new fault models account for the simultaneous dual-access property of the device. In addition to the classical static neighborhood pattern-sensitive faults, the array test algorithm covers a new class of pattern sensitive faults, duplex dynamic neighborhood pattern-sensitive faults (DDNPSF)

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