Performance Driven Standard-Cell Placement Using The Geneticalgorithm

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Summary

Current placement systems attempt to optimize several objectives, namely area, connection length, and timing performance. In this paper we present a timing-driven placer for standard-cell IC design. The placement algorithm follows the genetic paradigm. Besides optimizing for area and wire length, the placer minimizes the propagation delays on a predicted set of critical paths. The paths are enumerated using a new approach based on the notion of -criticality. Experiments with test circuits demonstrate delay performance improvement by up to 20%