On Efficient Extraction Of Partially Specified Test Sets For Synchronous Sequential Circuits

El-Maleh, A. Al-Utaibi, K.; King Fahd Univ. of Pet. & Miner., Dhahran, Saudi Arabia;

Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Symposium on;Publication Date: 25-28 May 2003;Vol: 5,On page(s): V-545- V-548 vol.5; ISBN: 0-7803-7761-3

King Fahd University of Petroleum & Minerals

http://www.kfupm.edu.sa

Summary

Testing systems-on-a-chip (SOC) involves applying huge amounts of test data, which is stored in the tester memory and then transferred to the circuit under test (CUT) during test application. Therefore, practical techniques, such as test compression and compaction, are required to reduce the amount of test data in order to reduce both the total testing time and the memory requirements for the tester. Relaxing test sequences, i.e. extracting partially specified test sequences, can improve the efficiency of both test compression and test compaction. In this paper, we propose an efficient test relaxation technique for synchronous sequential circuits that maximizes the number of unspecified bits while maintaining the same fault coverage as the original test set.

For pre-prints please write to:abstracts@kfupm.edu.sa

© Copyright: King Fahd University of Petroleum & Minerals;
http://www.kfupm.edu.sa