A New Static Differential CMOS Logic With Superior Low Power Performance

Elrabaa, M.E.S.; Comput. Eng. Dept., King Fahd Univ. of Pet. & Minerals, Saudi Arabia;
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King Fahd University of Petroleum & Minerals

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Summary

A new differential static CMOS logic (DSCL) family is devised. The new circuit is fully static, making it simple to design. The circuit topology of the DSCL and its operation is explained. Its performance in terms of delay, power, and area is compared to that of conventional static differential logic and dynamic differential logic. SPICE simulations using a 0.18 /spl mu/m technology with a power supply of 1.8 V was utilized to evaluate the performance of the three circuits. Two different sets of simulations were carried out; one with equal input capacitances of all circuits and another with equal circuit delays. For each design, all circuits were optimized for minimum delay. It is shown that at equal input capacitance, the DSCL achieved 40% less delay than the DCVSL at one third the power. Also, at equal delay, the DSCL achieved 20% of the power dissipation of the DCVSL and 78% of the DDCVSL making it the most energy-efficient among the three circuits.