# Iterative Heuristics For Multiobjective VLSI Standard Cellplacement

Sait, S.M. Youssef, H. El-Maleh, A.H. Minhas, M.R.;Dept. of Comput. Eng., King Fahd Univ. of Pet.Miner., Dhahran;

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King Fahd University of Petroleum & Minerals

**http://www.kfupm.edu.sa**

## Summary

We employ two iterative heuristics for the optimization of VLSI standard cell placement. These heuristics are based on genetic algorithms (GA) and tabu search (TS) respectively. We address a multiobjective version of the problem, in which power dissipation, timing performance, and interconnect wire length are optimized while layout width is taken as a constraint. Fuzzy rules are incorporated in order to design a multiobjective cost function that integrates the costs of three objectives in a single overall cost value. A series of experiments is performed to study the effect of important algorithmic parameters of GA and TS. Both the techniques are applied to ISCAS-85/89 benchmark circuits and experimental results are reported and compared