Timing Driven Genetic Algorithm For Standard-Cell Placement

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Summary

In this paper we present a timing-driven placer for standard-cell IC design. The placement algorithm follows the genetic paradigm. At early generations, the search is biased toward solutions with superior timing characteristics. As the algorithm starts converging toward generations with acceptable delay properties, the objective is dynamically adjusted toward optimizing area and routability. Experiments with test circuits demonstrate delay performance improvement by up to 20%. Without any noticeable loss in solution quality, sizable reduction in runtime is obtained when population size is allowed to decrease in a controlled manner whenever the search hits a plateau