High-Speed Self-Timed Carry-Skip Adder

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Summary

An efficient self-timed carry-skip adder with low area overhead and fast operation is proposed. The adder combines delay-insensitive and bounded delay completion signal detection techniques to define a novel, reliable, area-efficient and high-speed completion-detection circuit. The circuit employs double-rail encoded carry signals together with process-tracking delay circuit elements to efficiently produce a final completion signal of tight acknowledge slack time under different operating conditions. In addition the proposed adder employs carry-skip speed-up circuitry resulting in a novel self-timed carry-skip adder that is quite efficient in terms of both speed and area