General Iterative Heuristics For VLSI Multiobjective Partitioning

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Summary

The problem of partitioning appears in several areas ranging from VLSI, parallel programming, to molecular biology. The interest in finding an optimal partition especially in VLSI has been a hot issue in recent years. In VLSI circuit partitioning, the problem of obtaining a minimum cut is of prime importance. With current trends, partitioning with multiple objectives which includes power, delay and area, in addition to minimum cut is in vogue. In this paper, we engineer two iterative heuristics for the optimization of VLSI netlist bi-Partitioning. These heuristics are based on Genetic Algorithms (GAs) and Tabu Search (TS) and incorporate fuzzy rules in order to handle the multiobjective cost function. Both heuristics are applied to ISCAS-85/89 benchmark circuits and experimental results are reported and compared.