

DESIGN AND SIMULATION OF A WIDE RANGE AND HIGHLY LINEAR CURRENT TO TIME CONVERTER

BY
MAZEN MOHAMED ABOUELEZZ

A Thesis Presented to the
COLLEGE OF GRADUATE AND INTERDISCIPLINARY STUDIES
KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE
In
ELECTRICAL ENGINEERING

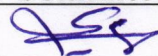
DECEMBER 2024

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
DHAHRAN 31261, SAUDI ARABIA

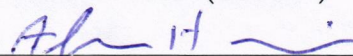
DEANSHIP OF GRADUATE STUDIES

This thesis, written by **MAZEN MOHAMED ABOUELEZZ** under the direction of his thesis adviser and approved by his thesis committee, has been presented to and accepted by the Dean of Graduate Studies, in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE IN ELECTRICAL ENGINEERING**.

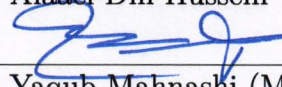
Thesis Committee



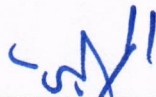
Dr. Muneer Al-Absi (Adviser)



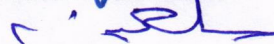
Dr. Alaael-Din Hussein (Member)



Dr. Yaqub Mahnashi (Member)



Dr. Mohammad AlMuhaini
Department Chairman



Dr. Suliman Al-Homidan
Dean of Graduate Studies

Date



©Mazen Abouelezz
2024

*I dedicate this work to my family that helped in every step of my
journey*

ACKNOWLEDGMENTS

First, I thank the almighty and only god Allah. This thesis would never have been possible if not for Allah's guidance and blessings. My thanks extend to my family. Their heartfelt support was always appreciated and their encouragement was a part of Allah's blessings. I am also grateful to my supervisor, Dr. Muneer Ahmed Al-absi for his continuous guidance and support. It has been and it will always be - a pleasure working with you.

TABLE OF CONTENTS

ACKNOWLEDGMENTS	vi
LIST OF TABLES	ix
LIST OF FIGURES	x
ABSTRACT (ENGLISH)	xv
ABSTRACT (ARABIC)	xvii
CHAPTER 1 INTRODUCTION	1
1.1 Motivation	5
1.2 Proposed Idea	6
1.3 Organization of this thesis	6
CHAPTER 2 LITERATURE REVIEW	7
2.1 Voltage to Time Converter (VTC)	8
2.2 Applications of VTCs in Time to Digital Converters	15
2.3 Current to Time Converters	21
CHAPTER 3 PROPOSED CURRENT TO TIME CONVERTER	24
3.1 Exponential and logarithmic functions circuit implementations	26
3.2 Proposed Basic Cell for PVT independent implementation of Exponential/logarithmic functions	49
3.2.1 Performance Analysis	56
3.3 Proposed Exponential Function	57
3.3.1 Simulation Results	58

3.3.2	Post-layout Simulation Results	62
3.3.3	Simulation Vs Theory	68
3.4	Logarithmic Function	69
3.4.1	Simulation Results	70
3.4.2	Post-layout Simulation Results	74
3.4.3	Simulation Vs Theory	80
3.5	Inverse Function	81
3.5.1	Simulation Results	83
3.5.2	Post-layout Simulation Results	86
3.5.3	Simulation Vs Theory	90
3.6	CTC with Inverse Function	92
3.6.1	Post-layout Simulation Results	96
CHAPTER 4 CONCLUSION		102
4.1	Future Work and Recommendations	103
REFERENCES		104
VITAE		118

LIST OF TABLES

Table 2.1	Comparison between different VTCs	20
Table 3.1	Sizes of all transistors used in the design of the basic cell shown in Fig.3.24	51
Table 3.2	Sizes of all transistors used in the design of the exponential circuit shown in Fig3.30.	58
Table 3.3	Summary of exponential circuits comparison	67
Table 3.4	Sizes of all transistors used in the design of the logarithmic circuit shown in Fig3.44.	70
Table 3.5	Summary of logarithmic circuit comparison	79
Table 3.6	Comparison between different CTCs	100

LIST OF FIGURES

Figure 1.1	Block diagram for time based analog to digital converter TDC. .	3
Figure 1.2	General current starved VTC circuit using CMOS technology. .	4
Figure 2.1	Circuit proposed by [2].	8
Figure 2.2	General block design of [3].	9
Figure 2.3	Circuits of work (a) t_{rise} and (b) t_{fall} [3].	9
Figure 2.4	VTC circuit realization proposed by [4].	10
Figure 2.5	Block diagram of the complete VTC proposed by the work of [4]. VTC core is shown in Fig. 2.4	10
Figure 2.6	Circuit proposed by [5], where several VTCs are used.	11
Figure 2.7	Circuit proposed by [6].	11
Figure 2.8	nMOS VTC circuit proposed by [7].	12
Figure 2.9	pMOS VTC circuit proposed by [7].	12
Figure 2.10	Circuit proposed by [7].	13
Figure 2.11	VTC circuit proposed by [10].	14
Figure 2.12	VTC circuit proposed by [11].	15
Figure 2.13	Block diagram of the two-step pipelined 8-bit TDC [13].	16
Figure 2.14	Block diagram of the combined VTC and TDC [14].	16
Figure 2.15	Schematic diagram of the low power and low speed TDC [15]. .	17
Figure 2.16	Comparator used in the design of TDC [16].	18
Figure 2.17	Block diagram of the hybrid ADC design [19].	19
Figure 3.1	Block diagram of the proposed current to time converter.	25
Figure 3.2	Block diagram of the proposed inverse function used in Fig.3.1.	26

Figure 3.3	Block diagram of the circuit to approximate the exponential/logarithmic. [78]	33
Figure 3.4	Circuit to produce the square root needed for the exponential/logarithmic.[78]	33
Figure 3.5	Circuit to produce the exponential approximation.[79]	34
Figure 3.6	Circuit to square input current.[81]	35
Figure 3.7	Circuit to produce square root of the input current.[81]	36
Figure 3.8	Circuit to produce logarithmic function approximation of the input current.[81]	36
Figure 3.9	Circuit to produce exponential function approximation of the input current in weak inversion region.[82]	37
Figure 3.10	Circuit used to multiply I_x and I_y [84].	38
Figure 3.11	Circuit used to generate x^2 and x [47].	40
Figure 3.12	Output current I_A [47].	42
Figure 3.13	Output current I_B [47].	42
Figure 3.14	Block diagram of exponential circuit implemented [47].	43
Figure 3.15	Block diagram of the proposed logarithmic function [47].	43
Figure 3.16	Results of realization of the approximated exponential using basic cell [47].	44
Figure 3.17	Results of realization of the approximated $\ln(x)$ using basic cell [47].	44
Figure 3.18	Effect of temperature on I_A [47].	46
Figure 3.19	Effect of temperature on I_B [47].	46
Figure 3.20	Temperature performance for exponential circuit in [47].	47
Figure 3.21	Temperature performance for the logarithmic circuit in [47].	48
Figure 3.22	Results of realization of $\ln(x)$ using $\exp(x)$ and $\ln(x)$ built with basic cell before modification [47].	48
Figure 3.23	Temperature performance before the improvement [47].	49
Figure 3.24	Proposed Basic Cell	50
Figure 3.25	Output current after modification on I_A	52

Figure 3.26 Effect of temperature after modification on I_A	53
Figure 3.27 Corner Analysis of IA	54
Figure 3.28 (a) Plot of I_B (b) Effect of process variation on I_B of the pro- posed circuit	55
Figure 3.29 Block diagram of exponential circuit implemented.	57
Figure 3.30 The proposed current-mode exponential function generator's circuit schematic	58
Figure 3.31 Results of realization of exponential using proposed basic cell. .	59
Figure 3.32 Temperature performance using the proposed basic cell.	59
Figure 3.33 Plots for corner analysis of exponential circuit	60
Figure 3.34 Plot of the AC analysis of the exponential circuit	61
Figure 3.35 Histogram of the Monte Carlo simulation of the exponential function schematic showing the number of samples at input $x=0\mu A$.	62
Figure 3.36 Layout of the exponential circuit	62
Figure 3.37 Plots of post-layout and schematic of the exponential function. .	63
Figure 3.38 Temperature analysis of the extracted view of the exponential circuit	64
Figure 3.39 Corner analysis of the extracted view of the exponential circuit	64
Figure 3.40 AC analysis of the extracted view of the exponential circuit. .	65
Figure 3.41 Histogram of the Monte Carlo simulation of the exponential function post-layout showing the number of samples at input $x=0\mu A$	66
Figure 3.42 Plots of theory, approximated and schematic simulation for $\exp(x)$.	68
Figure 3.43 Block diagram of logarithmic circuit implemented.	69
Figure 3.44 The proposed current-mode logarithmic function generator's cir- cuit schematic	70
Figure 3.45 Results of realization of logarithmic function using proposed basic cell.	71
Figure 3.46 Temperature analysis of the logarithmic function using the pro- posed basic cell.	71
Figure 3.47 Plots for corner analysis of logarithmic circuit	72

Figure 3.48 Plot of the AC analysis of the logarithmic circuit	73
Figure 3.49 Histogram of the Monte Carlo simulation of the logarithmic function schematic showing the number of samples at input $x=1\ \mu\text{A}$.	74
Figure 3.50 Layout of the logarithmic circuit	74
Figure 3.51 Plots of post-layout and schematic of the logarithmic function. .	75
Figure 3.52 Temperature analysis of the extracted view of the logarithmic circuit	76
Figure 3.53 Corner analysis of the extracted view of the logarithmic circuit .	76
Figure 3.54 AC analysis of the extracted view of the logarithmic circuit. . .	77
Figure 3.55 Histogram of the Monte Carlo simulation of the logarithmic function post-layout showing the number of samples at input $x=1\ \mu\text{A}$.	78
Figure 3.56 Plots of theory, approximated and schematic simulation for $\ln(x)$. .	80
Figure 3.57 Block diagram of inverse function.	81
Figure 3.58 The proposed current-mode inverse function generator's circuit schematic	82
Figure 3.59 Results of realization of inverse function using proposed basic cell. .	83
Figure 3.60 Temperature analysis of the inverse function using the proposed basic cell.	84
Figure 3.61 Plots for corner analysis of inverse circuit	84
Figure 3.62 Plot of the AC analysis of the inverse circuit	85
Figure 3.63 Histogram of the Monte Carlo simulation for inverse function schematic showing the number of samples at input $x=0.9\ \mu\text{A}$	86
Figure 3.64 Layout of the inverse circuit	86
Figure 3.65 Plots of post-layout and schematic of the inverse function. . . .	87
Figure 3.66 Temperature analysis of the extracted view of the inverse circuit .	88
Figure 3.67 Corner analysis of the extracted view of the inverse circuit . . .	88
Figure 3.68 AC analysis of the extracted view of the inverse circuit.	89
Figure 3.69 Histogram of the Monte Carlo simulation for inverse function post-layout showing the number of samples at input $x=0.9\ \mu\text{A}$	90
Figure 3.70 Plots of theory, approximated and schematic simulation for $\text{inv}(x)$. .	90

Figure 3.71	Block diagram of the current to time conveter.	92
Figure 3.72	Plots of the output as a function of time for the proposed CTC .	93
Figure 3.73	Plot of the delay as a function of the input current.	93
Figure 3.74	Delay of CTC using valid input for $\text{inv}(x)$	94
Figure 3.75	Plots of temperature analysis on the delay at $x = 0.5\mu A$	95
Figure 3.76	Plots of the corner analysis at $x = 0.5\mu A$	95
Figure 3.77	Histogram of the Monte Carlo simulation for CTC schematic showing the number of samples at input $x = 0.9\mu A$	96
Figure 3.78	Layout of the proposed CTC.	97
Figure 3.79	Plots of the output voltage for pre- and post-layout simulation for the CTC	97
Figure 3.80	Temperature analysis of the extracted view of the CTC circuit .	98
Figure 3.81	Corner analysis of the extracted view of the CTC circuit	98
Figure 3.82	Histogram of the Monte Carlo simulation for CTC post-layout showing the number of samples at input $x = 0.9\mu A$	99

THESIS ABSTRACT

NAME: Mazen Mohamed Abouelezz

TITLE OF STUDY: Design and Simulation of a Wide Range and Highly Linear
Current to Time Converter

MAJOR FIELD: Electrical Engineering

DATE OF DEGREE: December 2024

The Analog to Digital Converters (ADCs) are regarded as one of the most crucial components for embedded systems, Ultra Wide Band (UWB) receivers, Software Defined Radio (SDR), and biomedical applications. Most of today's integrated circuits (ICs) are a combination of digital and analog systems that take use of the expanding capabilities of Digital Signal Processing (DSP). Power consumption and processing speed are only two of the numerous reasons why DSP is better than analog signal processing. Therefore a high demand for high-speed low power Analog to Digital Converters (ADCs) has led to the design of time-based ADCs which combines the high speed of current-based ADCs and the lower power consumption of voltage-based ADCs. In time-based ADCs, the input signal (current/voltage) is controlling the delay of the output pulse by using Signal to Time Converter (STC) and then the pulse is converted

to digital by using Time-to-Digital Converter (TDC). Also, TDC can take advantage of the scalability of CMOS technology. The performance of TDC is determined by the quality of the STC used. STC (current/voltage) is an important and crucial stage of TDC. There are two Types of STCs which are the Voltage to Time Converter (VTC) and Current to Time Converter (CTC). There are many designs of VTCs and CTCs that have been reported in the literature. However, they suffer from one or more of the following: 1-nonlinearity 2-high power consumption 3-PVT dependence 4- low input range. This thesis introduces a new CTC design that uses inverse function to solve the challenges of previous designs. The CTC's full input range is $1.6\mu A$ with a maximum linearity error less than 1.8%. The design is PVT independent where the error due to temperature is less than 0.5% and error due to corner process is less than 3%. The proposed CTC can operate up to 1.115 MHz

ملخص الرسالة

الاسم:

مازن محمد ابوبكر الصديق ابوالعز

عنوان الدراسة:

تصميم ومحاكاة محول تيار إلى زمن واسع النطاق وخطي للغاية

التخصص:

الهندسة الكهربائية

تاريخ الدرجة العلمية: ديسمبر 2024

عند كتابة ملخص ، ضع في اعتبارك مجرد ملخص هو ملخص وصفي قصير لأطروحتك. قد يختلف أدى الطلب المرتفع على محولات الإشارة المستمرة إلى رقمية (م-ر) ذات التحويل عالي السرعة ومنخفضة الطاقة إلى تصميم محولات تعتمد على الوقت في نقل المعلومات. في المحولات (م-ر) القائمة على الوقت، يتم تحويل الإشارة المدخلة (التيار - الجهد) إلى نبضة تأخير في الوقت باستخدام محول الإشارة إلى الوقت ثم يتم تحويل النبضة إلى رقمية باستخدام محول الوقت إلى الرقمي (و-ر). يتمتع (و-ر) بالعديد من المزايا مقارنة بالمحول (م-ر) التقليدي مما يجعله مناسباً للتطبيقات ذات السرعة المنخفضة والعالية. يتم تحديد أداء (و-ر) من خلال جودة محول الإشارة بداخله المستخدم. محولات الإشارة (التيار / الجهد) هي مرحلة مهمة وحاسمة من (و-ر). هناك نوعان من محولات الإشارة هما محول الجهد إلى الوقت (ج-و) ومحول التيار إلى الوقت (ت-و). هناك العديد من تصميمات (ج-و) و (ت-و) التي تم الإبلاغ عنها في الأبحاث المسبقة. ومع ذلك، فإنها تعاني من واحد أو أكثر مما يلي: 1- عدم الخطية 2- استهلاك الطاقة العالي 3- اعتمادها على الحرارة وتغيرات التشغيل 4- نطاق الإدخال المنخفض.

يقدم هذا العمل تصميمًا جديدًا لـ (ت-و) يستخدم الدالة العكسية لحل تحديات التصميمات السابق ذكرها. يبلغ نطاق الإدخال الكامل لـ (و-ت) إلى 1.6 مايكرو امبير مع خطأ خطي لا يتعدى 1.8 بالمئة. التصميم مستقل عن تغيرات درجة الحرارة والعمليات التشغيل حيث يكون الخطأ الناتج عن درجة الحرارة أقل من 0.5 بالمئة والخطأ الناتج عن عملية التشغيل أقل من 3 بالمئة. يمكن أن يعمل هذا (ت-و) حتى 1.115 ميغا هرتز

CHAPTER 1

INTRODUCTION

Every signal in our environment is a continuous analog signal as we live in an analog universe. Our ability to comprehend and digest these messages is essential to our lives. Nowadays, the tendency in electronics industry tries to perceive, monitor, and control everything in our environment. The researchers in the electronics area have designed and still designing many analog to digital converters to meet customer demands due to the outstanding advancements in the field of digital signal processing (DSP). Through the conversion of analog signals to digital signals, the analog to digital converters seemed to bridge the gap between the analog and digital processing domains. As a result, most integrated circuits in use today are hybrid analog/digital circuits that require ADCs. Also, signal processing is a vital area of research, extracting new ideas and insights from raw data. This process needs to be fast and consume low power. There many types of ADCs depending on the input signal. Most popular types are:

- Voltage-based ADCs
- Current-based ADCs

- Time-based ADCs

Voltage-based ADCs are simpler to use and more robust since they have been optimized over very long period. This type of ADCs are fast, but require a lot of space due to many active and passive components used, like flash ADCs.

Current-based ADCs are faster but need many switches. Also, they consume high power due to the constant currents running that most of the time are idle, especially when it comes to current-steering ADCs.

Time-based ADCs utilize the time difference between two signals. One signal is a basis that the system generates, and the other is a shifted version that is affected by the incoming data. Time Mode Signal Processing (TMSP) is the term for this method.

Coding, quantization, and sampling are the main steps in the ADC process. Using voltage as the input signal and generating digital outputs, voltage-based ADCs were the first kind. ADCs based on current use more power than those based on voltage, while being quicker. Given its advantages over both voltage- and current-based ADCs in terms of high-speed operation and low power consumption, time-based ADCs (T-ADCs) are a promising field of study [1].

Scaling down the CMOS technologies have improved the performance when dealing with digital signals, which can be utilized in T-ADCs due to the digital nature of the time mode signal [2]. The first stage of T-ADC is the Signal to Time Converter (STC). The main factor limiting the T-ADC performance is the STC. The desired STC is required to have good linearity, small area, low power consumption and immunity to

process, voltage, and temperature variations (PVT).

There are two types of STCs: Voltage to Time Converters (VTCs) and Current to Time Converter (CTCs). Both CTC and VTC share the same desired characteristics.

This literature shows that the VTC design using current starved inverter in Fig.1.2. But VTCs suffers from two major setbacks which are the inverse relation and squaring relation between the input voltage and delay.

On the other hand, CTC has only one setback which is the inverse relation. This made recent work focus on CTCs more as it shows more potential

The general block diagram for T-ADC is shown in Fig.1.1. The VTC is the core block in T-ADC.

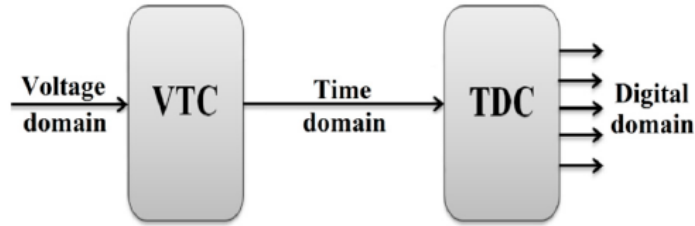


Figure 1.1: Block diagram for time based analog to digital converter TDC.

The VTC takes the analog input voltage and produces a series of delayed pulses, while the CTC takes current input and controls the discharging current to produce the delayed pulses. A simple CMOS VTC circuit is shown in Fig. 1.2.

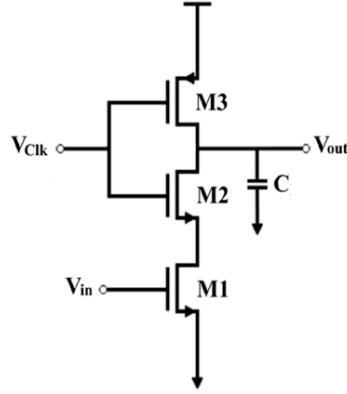


Figure 1.2: General current starved VTC circuit using CMOS technology.

With reference to Fig.1.2 , a clock signal V_{clk} is applied at the gate of $M2$ and $M3$. This will result at a delayed inverted signal at the output V_{out} . The time edge required to have the falling edge can be controlled using a Biased $M1$ with the input voltage V_{in} . The relation between the time delay at the output and the input voltage that is applied at the gate of $M1$ is as follows:

$$I_D = C \frac{dV}{dt} \quad (1.1)$$

$$dt = C \frac{dV}{I_D} \quad (1.2)$$

$$dt = C \frac{dV}{0.5K \frac{W}{L} (V_{in} - V_T)^2} \quad (1.3)$$

Where C is the total capacitance at the output, I_D is the drain current of $M1$ in saturation and dt is the time delay. K , L , W , V_T are electron/hole mobility, length, saturation and dt is the time delay.

width and threshold voltage of the transistors used.

As seen from Eq.1.3 the relation between the input voltage and delay square and inverse. Similarly, in Eq.1.3 the relation is inverse between the drain current of $M1$ and the delay dt . This makes the work of CTC more appealing since it requires solving only the inverse issue without the squaring.

1.1 Motivation

As technology advances, advancements in digital circuits outpace advancements in analog circuits. There are two primary causes. First, as technology advances, the supply voltage decreases, which lessens the voltage swing. But the noise does not scale with the technology, resulting in a lower signal to noise ratio that weakens the analog system's immunity to noise. Secondly, the supply voltage and the threshold voltage do not scale with the same factor. On the other hand T-ADCs takes advantage of the technology advances. CTCs show better performance in theory due to having only inverse relation instead of inverse squaring like VTCs, which make CTCs a better core block for the T-ADCs,.

This thesis proposes a new CTC block that outperforms all CTCs and VTCs blocks in the literature. The new CTC block utilize an inverse function in strong inversion to achieve high linearity, while being PVT independent, compact and have high speed.

1.2 Proposed Idea

The new proposed CTC will use an inverse function circuit to control the current of M1 in Fig.1.2. This will result in a linear relation between the input current and the delay at the output. But an inverse function circuit with the required characteristics is not found in the literature. A new inverse function circuit that satisfies the requirements is proposed, then the function is used to derive the current in the starved current inverter using current mirrors.

1.3 Organization of this thesis

This thesis is structured as follows: First literature of VTC and CTC design and some application in T-ADCs are discussed. Then a literature of a way to build an inverse function using exponential and logarithmic functions approximation is discussed. Finally, the proposed CTC with the inverse function circuit is discussed in details with simulation results as well as post-layout simulation results of each block in the circuit.

CHAPTER 2

LITERATURE REVIEW

VTC has been a subject of considerable research interest due to their critical role in various applications, particularly in T-ADC. This chapter delves into the existing literature on VTC designs, highlighting the significant advancements and ongoing challenges in this field. The non-linearity of output delay concerning the input voltage, as derived from Eq. 1.3, necessitates innovative solutions to achieve a STC with excellent linearity and insensitive to PVT variation. Recent years have witnessed a many VTC designs to improve linearity, expanding the input range, and boosting the operational speed. By synthesizing the findings from various studies, this chapter provides a comprehensive overview of the state-of-the-art in time-mode designs, setting the stage for the subsequent chapters that will introduce novel approaches to address the identified gaps and limitations.

2.1 Voltage to Time Converter (VTC)

In recent years, many designs of VTC, applications and investigations were proposed to solve the issues present in Eq. 1.3. These designs mainly focus on improving the linearity, input range or operation speed. These designs are mainly in voltage domain.

The works of [2], [3],[4],[5],[6], and [7] used the current starved as the basis of their design. The authors in [2], proposed a high speed VTC that uses the current starved and folded cascode as shown in Fig. 2.1. The $Pb2$ transistor is used to pre-charge the drain of both $Pb3$ and $Na3$ to V_{dd} .

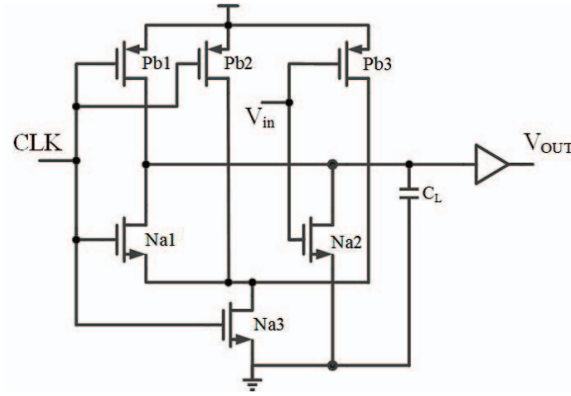


Figure 2.1: Circuit proposed by [2].

The design of [3] consists of four blocks as shown in Fig. 2.2. The work focused on improving the current starved inverter shown in Fig. 1.2 for the two blocks of t_{fall} and t_{rise} . The proposed circuit for each block is shown in Fig. 2.3. As shown in 2.3 the two circuits are simple current starved with an additional current path in case if the input transistor is OFF. This additional current path is provided by using $Pb3$ in Fig. 2.3 (a) and $Na1$ in Fig. 2.3 (b). Finally, the outputs of the two t_{fall} and t_{rise} blocks are fed to XNOR gate to produce the output puls that can be used in TDC.

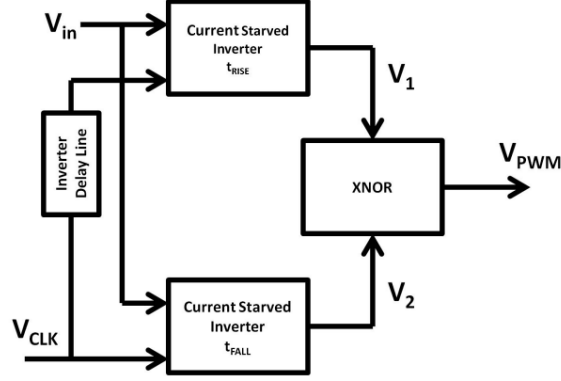


Figure 2.2: General block design of [3].

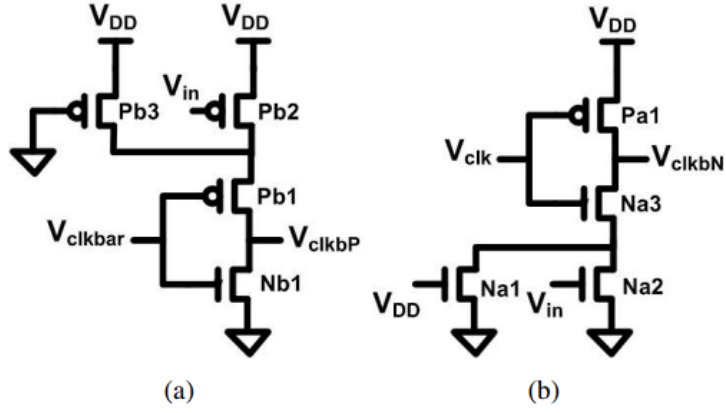


Figure 2.3: Circuits of work (a) t_{rise} and (b) t_{fall} [3].

The main VTC circuit in Fig. 1.2 has been modified by the authors in [4], where M6 and M5 in their design function as charging and discharging gates to the drain of M2 and the drain of M3, respectively. Lastly, M4 is used to regulate the circuit's delay. The delay in this design is partially due to the drain capacitance of M3. and V_{cap} can regulate this delay before repeating the circuit. The circuit depicted in Fig. 2.4 is the core VTC design that is shown in Fig. 2.5. The section with constant delay (below path) is designed to delay the clock signal entering the TDC by an identical amount

to the initial above path without any input, leaving only the delay generated by the input.

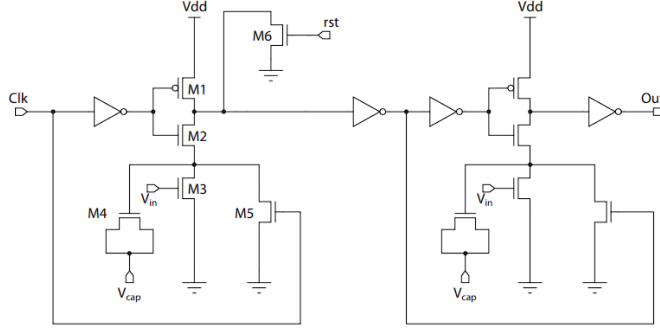


Figure 2.4: VTC circuit realization proposed by [4].

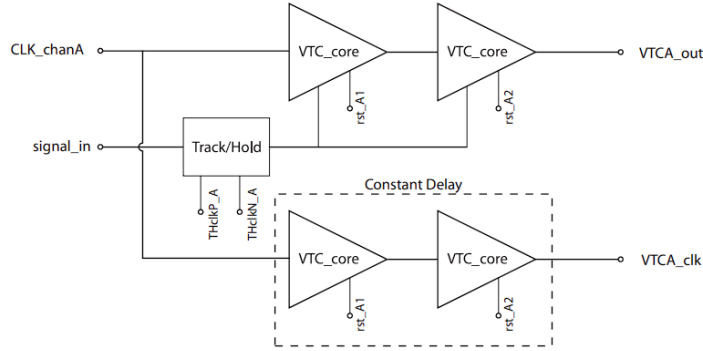


Figure 2.5: Block diagram of the complete VTC proposed by the work of [4]. VTC core is shown in Fig. 2.4

Another approach of modifying the general current starved VTC circuit in Fig. 1.2 is done by [5], where the authors used several current starved VTC as shown in Fig. 2.6. The circuit is mirrored to produce the delayed signal and its complement. The inverters are used as output buffer for capacitive load. With reference to Fig.2.6, M1,M2 and M5 are normal current starved VTC. M7 is used for degeneration and M11 and M13 are used to provide extra delay at certain range of V_{in} . This is achieved

by biasing M11 and M13 differently from M5. M9 is weak device to ensure a current path for low input voltages.

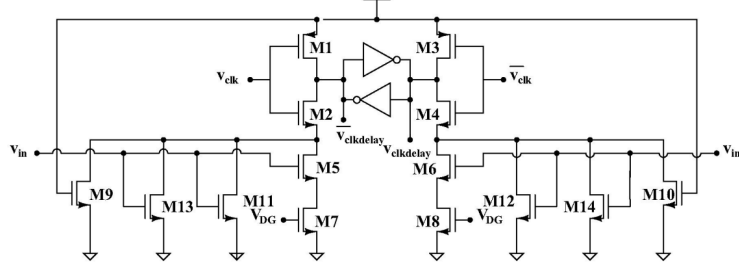


Figure 2.6: Circuit proposed by [5], where several VTCs are used.

The design in [6] is shown in Fig.2.7. It is an ultra-low power design and is achieved by cascading transistors to the general current starved in Fig. 1.2(a) to bias the circuit using two voltages. The bias voltages limit the current flowing in the circuit during the charging and discharging process. This design is expanded by using two matched current starved as shown in Fig. 2.7(b)

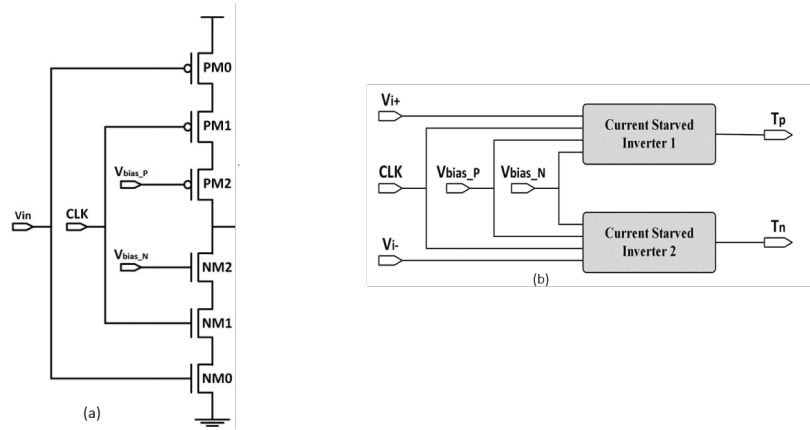


Figure 2.7: Circuit proposed by [6].

In reference [7], a new design is proposed where the input signal is applied from the bulk of the current starved. Applying the input from bulk allowed the authors in

[7] to propose two designs. One design where the input is applied to the bulk of the nMOS. The second design the input is applied to the bulk of the pMOS. Both designs are displayed in Fig. 2.8 and Fig. 2.9.

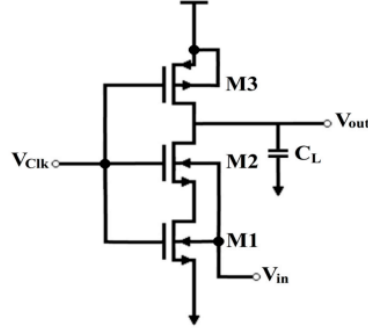


Figure 2.8: nMOS VTC circuit proposed by [7].

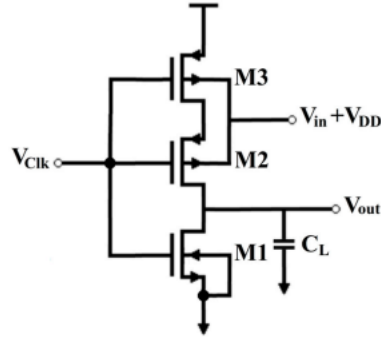


Figure 2.9: pMOS VTC circuit proposed by [7].

The delay time for both designs is given by Eq.2.1

$$dt = \frac{K_1 C dV}{K_1^2 - K_2^2 V_{BS}^2} - \frac{K_1 C dV V_{BS}}{K_1^2 - K_2^2 V_{BS}^2} \quad (2.1)$$

where

$$K_1 = \frac{K_n}{2} (V_{GS} - V_T)^2 \quad (2.2)$$

and

$$K_2 = \frac{K_n \gamma}{2\sqrt{2}\phi_f} (V_{GS} - V_T) \quad (2.3)$$

In both designs, the input to the transistors is fixed to V_{Clk} . Since the input voltage is applied to the body of nMOS in Fig. 2.8, the V_T changes. Similarly in Fig. 2.9, V_T changes due to the input voltage at the bulk of pMOS. This results in different V_{OV} and introduces different delays at V_{out} . This design suffers from having low input range due to the need of having V_{BS}^2 much smaller than V_{BS} to achieve linearity.

Also [7] proposed adding more transistors in series in Fig. 2.8 and connecting the body of all transistors to V_{in} as shown in Fig. 2.10(a). For the pMOS design, transistors are added in a similar way as seen in Fig. 2.10(b). This addition of transistors improve the linearity but decreases the speed of operation.

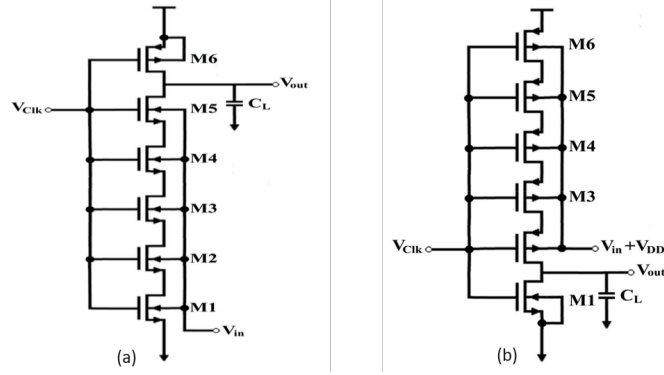


Figure 2.10: Circuit proposed by [7].

In [8], the authors designed a differential input VTC using switch capacitor and logic gates. The VTC is connected to a time amplifier through inverters to introduce suitable delay. Two flip-flops are used by the time amplifier for the positive and negative inputs, respectively. The design shows high input range of $2V$ and operates

at 1 GS/s.

The work of [9] used the general VTC in Fig. 1.2 and S/H circuits. The S/H circuits (implemented using switching capacitors) allowed [9] to have constant slope while charging and discharging. This constant slope improved the linearity for their design.

The authors in [10] proposed the VTC depicted in Fig. 2.11. It is composed of a comparator, buffer and switching capacitors that switches between the V_{inP} and V_{inN} . This VTC operates at a speed of 500-MHz.

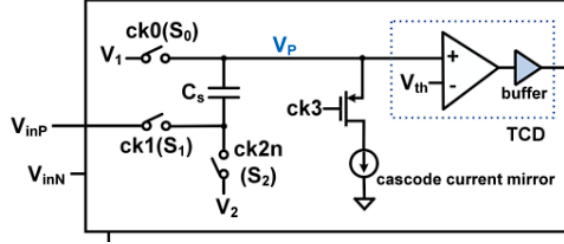


Figure 2.11: VTC circuit proposed by [10].

In reference [11] a VTC that operates at 7-GHz with high linearity is proposed. The schematic of this VTC is shown in Fig. 2.12. The ramp control generator provides the clock, reset signal V_{res} and starting signal V_{sw} . These signals are used to make sure that the capacitor C_s is discharged and the ramp generator is at constant slope. The ramp generator is followed by a chain of current starved inverters with different threshold voltages to provide fine delay transition. But the design suffers from small input range and the delay is so small of 6 fs/mV .

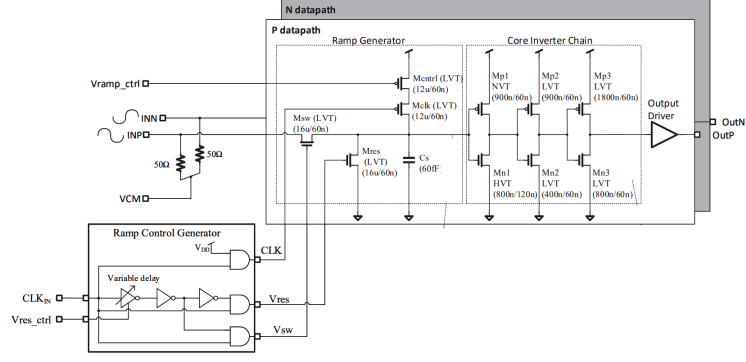


Figure 2.12: VTC circuit proposed by [11].

2.2 Applications of VTCs in Time to Digital Converters

The VTC is a core block in the T-ADC. The authors in [12], proposed a successive approximation register ADC that is based on dyadic digital pulse modulation. The VTC in their design has the advantage of low area and low power consumption but suffers from slow operating speed of 2.8 kHz.

In [13], a two-step pipelined 8-bit TDC is proposed with dynamic time amplification (DTA). The full TDC consists of two smaller TDCs named coarse TDC (CTDC) and fine TDC (FTDC) that has 16 and 32 delay cells, respectively. The output of CTDC is used in Time to voltage converter (TVC). In order to achieve a finer time delay at the TDC output terminal, the voltage signal is amplified by entering a VTC that has a certain gain V_{gain} . Finally the time signal from the VTC output enters the FTDC. The VTC and TVC are the DTA in the circuit. Finally the output of FTDC and a copy of CTDC output are connected to 64-8 bit decoder. The block diagram of

the design is shown in Fig. 2.13.

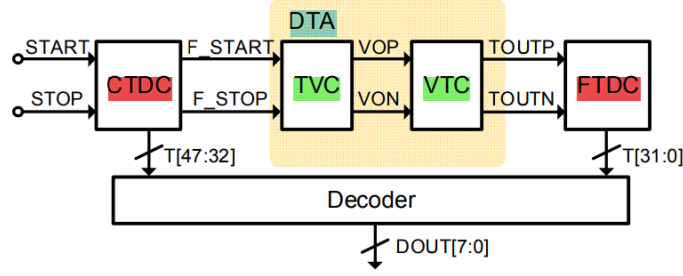


Figure 2.13: Block diagram of the two-step pipelined 8-bit TDC [13].

The authors in [14] proposes a 7-bit TDC that can operate at high frequency of 4 GS/s. The design consists of a 2-bit coming from the VTC designed and 5-bit from the TDC as shown in Fig. 2.14. The TDC has the disadvantages of having large area and high power consumption due to the use of multiple VTCs, comparators and time amplifications. But it has the advantage of being convenient to expand to more than 7-bits by adding VTCs at the cost of speed, area and power.

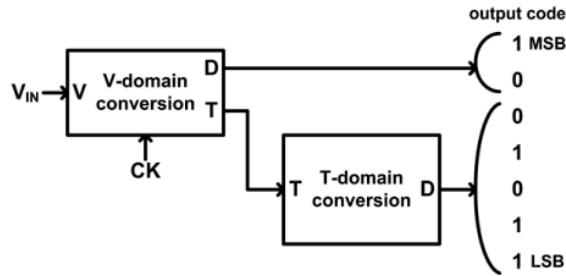


Figure 2.14: Block diagram of the combined VTC and TDC [14].

In [15], a very low power and extreme low speed TDC is proposed. The design is used for low frequency applications such as electrocardiogram. The design achieves the VTC without the use of current starved inverters as shown in Fig. 2.15. The VTC

consists of a subtractor, comparator, ramp generator and integrator. The comparator compares between the ramp generated signal and the subtracted signal of $V_{in}(n) - V_{in}(n-1)$ to produce a PWM signal. the integrator provides feedback and sampling by providing $V_{in}(n-1)$.

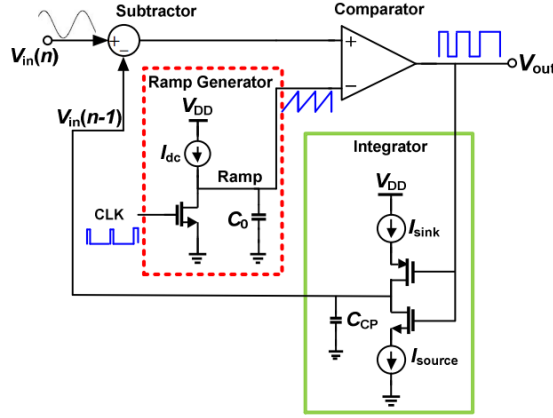


Figure 2.15: Schematic diagram of the low power and low speed TDC [15].

Reference [16] suggests an alternative method in which a TDC is constructed by 8x phase interpolation. To implement the VTC, the design makes use of switching capacitors, comparator, and ramp generator. A differential pair is utilized in the design by to reduce the noise. They minimized the delay variance caused by the comparator circuit by using a rail-to-rail comparator. The comparator can be seen in Fig. 2.16.

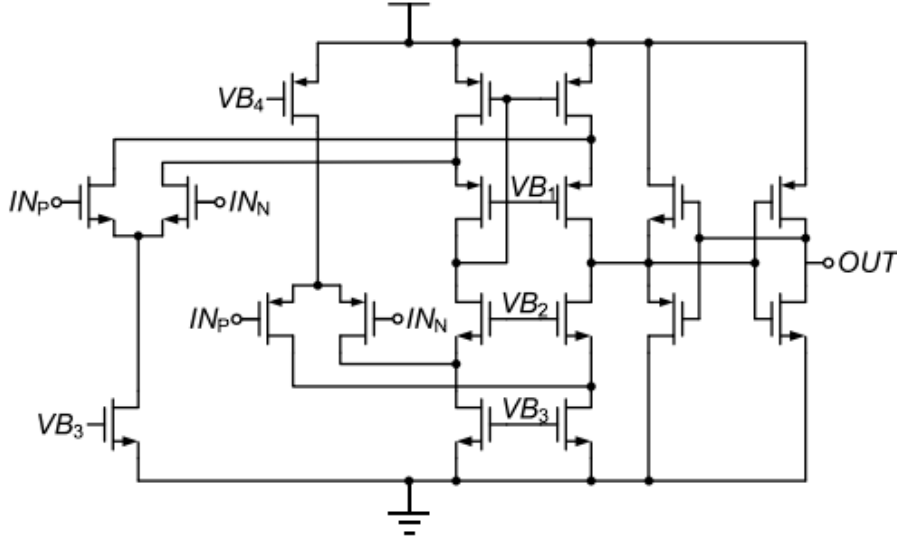


Figure 2.16: Comparator used in the design of TDC [16].

A TDC is proposed by [17], where the VTC proposed by [9] is used. The design used asynchronous pipeline successive approximation to reduce the quantization time required to approximate the correct time-domain output. The TDC achieves high sampling speed of 8-GS/s and a resolution of 8-bits with 85.3-mW power dissipation.

A 10-bit TDC that operates at 350 MHz is introduced in [18]. The design used a phase averaged coupled ring oscillator to improve the conversion of the time signal provided by their VTC to a digital signal.

A hybrid between voltage ADC and TDC design is proposed by [19]. An overall design of 11-bit V/TDC is achieved, where 3-bit is coded by the voltage domain part and 8-bit coded by the time domain part. The circuit is able to operate at 1 GS/s while consuming 14.9mW. The full schematic is shown in Fig. 2.17

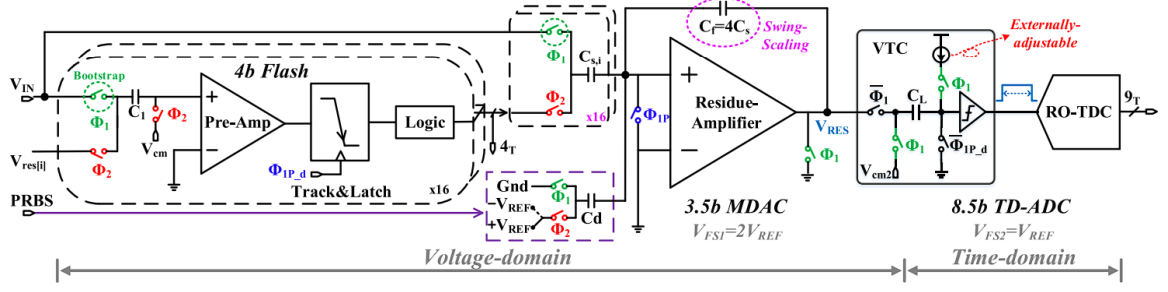


Figure 2.17: Block diagram of the hybrid ADC design [19].

The VTCs that are used in [14], [15], and [16] suffers from being tailored made to their design and cannot be used in other TDC designs. A comparison between the VTCs mentioned is shown in Table 2.1.

Table 2.1: Comparison between different VTCs

	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[13]	[14]	[15]	[16]
Year	2017	2013	2009	2006	2016	2020	2019	2022	2022	2023	2020	2021	2021	2023
Technology	65nm	65nm	90nm	130nm	130nm	65nm	65nm	65nm	28nm	28nm	65nm	65nm	180nm	65nm
Supply Voltage (V)	1.2	Not Reported	1	Not Reported	1	1.2	1.2	1	0.6	0.9/2.5	1.2	Not Reported	1	0.8
Input Range (V)	1 (differential)	0.15	0.1	0.2	0.24 (differential)	0.8	0.8	2 (differential)	0.6 (differential)	0.9	0.5	Not Reported	0.2 (per VTC)	0.3
Input values (V)	-0.5 to 0.5	0.2 to 0.35	0.3 to 0.4	0 to 0.2	0.65 to 0.8	-0.4 to 0.4	-0.4 to 0.4	-1 to 2	-0.3 to 0.3	0.5 to 1.4	-0.25 to 0.25	Not Reported	-0.1 to 0.1	-0.15 to 0.15
Power (mW)	0.477	Not Reported	3.6	Not Reported	0.668×10^{-3}	0.018	0.015	1.1	2.1	4.27	5.2	0.065	11.3	0.163×10^{-3}
Area (mm ²)	Not Reported	Not Reported	0.0068	Not Reported	Not Reported	26.67×10^{-3}	11.16×10^{-3}	Not Reported	0.0012	0.011	2.0×10^{-3}	Not Reported	0.011	Not Reported
Operating Frequency (GHz)	5	4	5	2	0.001	0.5	0.5	1	5	0.5	3	0.4	4	4×10^{-6}
Delay (ps/mV)	0.1	3.46	1	2.5	187	0.25	0.3	80	0.035	Not Reported	0.016	1.75	0.8	Not Reported
Linearity maximum error	2.5%	<1%	Not Reported	2.0%	0.4%	0.55%	0.4%	Not Reported	Not Reported	Not Reported	0.36%	Not Reported	6%	Not Reported

2.3 Current to Time Converters

Recently, the literature shown potential to use current to time conversion instead instead of VTC. One advantage can be seen in from Eq.2.4, that the relation between current to time is only inverse instead of inverse squared in VTC.

$$dt = C \frac{dV}{I_D} \quad (2.4)$$

The simple relation between teh delay and the inverse of the current makes CTCs achieve better linearity over VTCs with a simpler design. There are many designs for CTCs in the open literature. The author in [20] proposed a CTC that takes a differential voltage input and converts it into differential current then into a time delay. The design suffers from containing two capacitors and two resistors. Also, the design requires many switches and 3 comparators to function. The CTC work proposed in [21] is linear due to the inversion of current making the relation of current and delay

to be linear but the circuit suffers from using many passive components and the use of BJT which can't be integrated in CMOS technology. The authors in [22] built a CTC with a circuit that inverse the input current. The circuit shows good linearity, but the MOS used are working in weak inversion making it only suitable for low frequency application. Moreover, the input range of the circuit is very low of only 30 nA and the circuit is corner process dependent. The CTC circuit presented in [23] realizes the CTC with the use of many inductors to create a time advanced or delayed signal. This makes it very bulky and not integrable. Another CTC design that is working in weak inversion is presented in the work done by [24]. The design suffers from the same issues as the work in [22]. The authors in [25] proposed CTC that achieved pseudo-linearity with current mirrors only. But the design is very sensitive to temperature and corner process variation that makes it unreliable. The CTC design in [26] uses simple current to time converter with switches and many tail current transistors to minimize the leakage current and control the delay. The design is operating in subthreshold making the design not suitable for high speed operation. Also, the design linearity is very poor. The authors CTC work in [27] is suitable for high speed application up to 25 MHz with good linearity, but to maintain this linearity many voltage and current biases must remain constant since they all appear in time delay derived in their circuit. Also, the design is sensitive to temperature. The CTC design proposed by [28] is built using two op-amps, 4 conventional resistor, one capacitor and a magneto resistance. The input current is applied in such a way that it changes the magneto resistor and then the delay of the circuit is controlled by the value of the magneto resistor. The design suffers from needing a condition to operate that the magneto resistor has to

be higher than multiplication of the ratio of the other normal resistors. Also, the magneto resistance has to be kept in its linear range. Finally, their design can not be integrated due to the many passive components and the magneto resistance. The CTC proposed in [29] suffers from the use of 8 capacitors, 2 resistors and 2 inductors where the values of all passive components should be kept precisely constant to achieve the linear operation. The CTC design in [30] works by sensing the resistance variation in the input variable resistance then copy the current produced due to resistance change into a current starved inverter. The design linearity is poor due to not addressing the inverse relation in 2.4. Also, the corner process performance is very poor.

All previous designs share one or more issues of the following:

- BJT Implementation.
- Many passive elements are utilized.
- linearity issues.
- Using MOSFET in subthreshold and hence will be suitable for low frequency applications only.
- very small input range.
- Sensitive to PVT.

The motivation of this thesis is to build a CTC that overcomes all previous drawbacks. The comparison table including this thesis work is shown at the end of the proposed design in Table 3.6

CHAPTER 3

PROPOSED CURRENT TO TIME CONVERTER

As seen from the previous literature, the work focused on transforming voltage into time domain. This conversion follows Eq.1.3, requiring the VTC to be linear which is difficult to achieve due the inverted and squared relation. While in the current to time converter Eq.3.1 will be used and will be dealing with inverse function only.

This thesis proposes a PVT independent CTC. The CTC will take the input current X and inverts it then use the inverted current to achieve a highly linear current to time converter. According to Eq.3.1, the relation between the input current and the delay will be linear as seen in Eq.3.3.

$$dt = C \frac{dv}{I_D} \quad (3.1)$$

$$X = \frac{1}{I_D} \quad (3.2)$$

$$dt = CXdv \quad (3.3)$$

The proposed CTC block diagram is shown in Fig.3.1. The input current is applied to a natural log function then inverted. The inverted output is fed to the exponential block. The output of the exponential function will be the inverse of the input current X . This inverted current will be used to control the discharging the current in the starved starved inverter. Theoretically, this process achieves linearity between input current and output delay. Where the Inverse function is as shown in Fig.3.2.

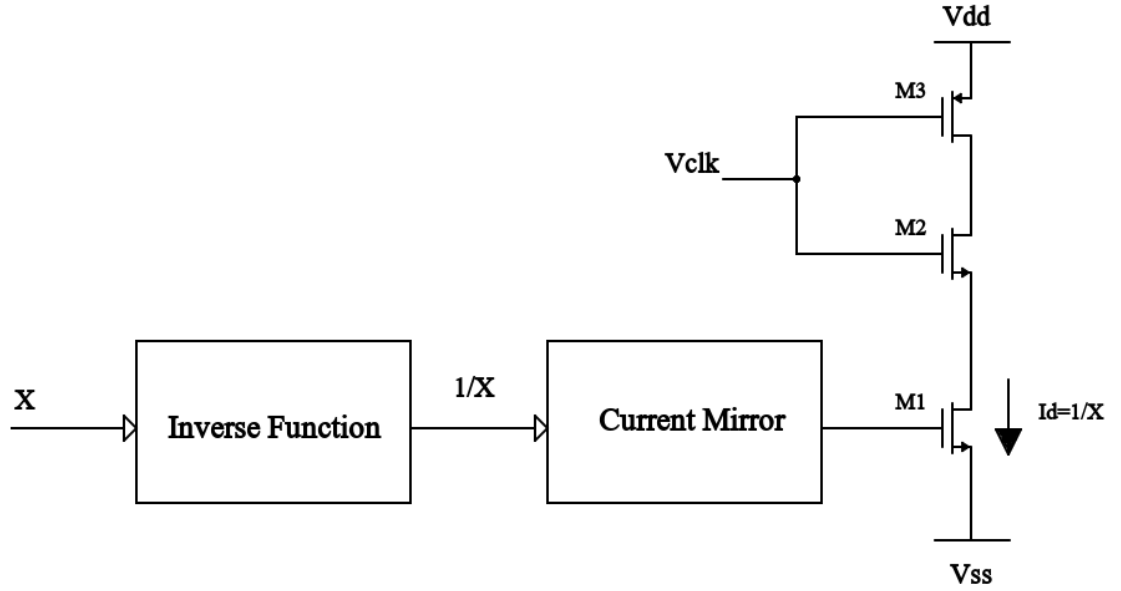


Figure 3.1: Block diagram of the proposed current to time converter.

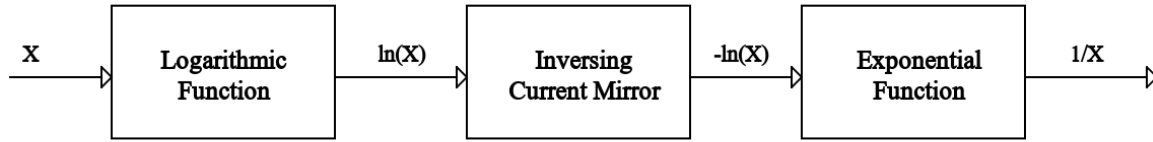


Figure 3.2: Block diagram of the proposed inverse function used in Fig.3.1.

The blocks shown in Fig.3.1 and Fig.3.2 will be individually discussed in details. The natural logarithmic and exponential blocks are approximated implementation using CMOS technology.

3.1 Exponential and logarithmic functions circuit implementations

A way to eliminate the inverse relation between the current and the delay is to have the input also related to the current inversely. So the relation between the input signal (current/voltage) is linear with the delay observed at the output. This inversion is achieved using inverse function. But the inverse function cannot be implemented directly using CMOS technology. This leads to the use of approximations techniques. One technique is using logarithmic and exponential circuits approximation to establish an inverse function. A logarithmic/exponential function is a nonlinear function whose output is proportional to the logarithm/exponential of the input. Circuits with such features are widely employed in a variety of applications such as medical equipment, instrumentation, telephones, active filters, disk drives, and neural networks. The works of [31], [32], [33], [34], [35], [36], and [37] implemented a logarithmic function using

BJT. The design in [31] uses a four stage consisting of dual-gain and limiters. Each stage contains four resistors, making the design bulky and not possible to integrate. The authors in [32] developed a programmable current source logarithmic function using BJT. This allows the logarithmic behavior to be changed to attenuation or amplification on demand by inverting the function. However, the logarithmic function implemented has high error and used many resistors. The researchers in [33] summarized different designs. All the designs suffers from using many resistors, capacitors and high power consumption. Also, the designs can be used in mid to high frequencies applications only. The design in [34], implemented the gain and limiting circuit using triple-tail cell. The cell is a BJT circuit consisting of a single tail current connected to a three common-emitter transistors. The circuit proposed the logarithmic function accuracy but it requires many stable biasing voltages in addition, many resistors and capacitors are used. The authors in [35] developed a low-voltage squaring circuits and used these circuits to implement the logarithmic function. The authors show two implementation of the log function, one using BJT and then replicated the circuit using MOS. The circuit suffers from being bulky needs multiple amplifying stages and the use of many passive components. The authors in [36] implemented a logarithmic function using BJT. But, the circuit utilizes a current to voltage converter. The work in [37] utilize the exponential property of BJT to implement the logarithmic function. The design is complex,used many passive elements and many amplifiers. In addition, it sensitive to temperature variations and is suitable for low frequency applications. Other works implemented the logarithmic function using Op-Amps and CFOAs such as [38], [39], [40], [41], [42], [43]. The researchers in [38] developed a high

speed logarithmic function that can be used in frequencies between 2 - 18 GHz. The author in [39] developed a good temperature insensitive logarithmic circuit, but the design uses many passive components. The design in [40] developed a temperature independent logarithmic function. The circuit requires two capacitors and a resistor and only useful for high frequency applications. The design in [41] is complicated and uses over 20 passive components with precise value that need to be kept constant for optimal operation. The authors in [42], used BJT based Op-Amp with a diode connected BJT in the feed-back loop to achieve logarithmic behavior. The circuit is complicated and uses 12 resistors and capacitor. The work in [43] used MOSFET Op-Amps with feed-back loop using BJT and passive components and biasing voltage. The works of [44] and [45] use multiple stages of amplifiers and limiters to implement the pseudo-logarithmic function using MESFET. Both designs are complicated and use over 20 passive components in each stage. The work in [46] adopted the idea of using several stages of amplifiers and limiters similar to previous work. The design has a better input range. However, the circuit suffers from the need of match resistors in the implementation. The authors in [47] used Taylor series expansion to implement a pseudo-logarithmic function but the design is very sensitive to temperature variations. The works in [48] and [49] use MOSFETs in weak inversion to utilize the exponential properties of MOSFETs. Both designs can only be used in very low frequency applications. The work in [50] uses a sixth-order general approximation to implement the logarithmic function. The circuit has a low normalized input range and it is sensitive to PVT. The authors in [50], [51] and [52] have used a complicated approximation methods and hence complicated designs that is difficult to integrate

into other applications. The authors in [53] developed an exponential function then swapped the input and output loops to realize logarithmic function.

The literature focused on exponential function implementation compared to the logarithmic function. Some did direct implementation using BJT exponential properties, or MOS properties in Weak Inversion. But most works focused on the approximation method to take advantage of the CMOS technology in strong inversion. a comprehensive of the works on exponential is as follow:

The work of [54] uses BJT's exponential properties to create the exponential function. The design contains six passive transistors and 4 independent sources. Other works used CMOS technology with an approximation implementation. The author in [55] designed an exponential circuit. The design is simple using CMOS technology, but suffers from the approximation used has high error and the circuit is temperature and process dependant. The work of [56] proposed an exponential circuit that uses the fourth order Taylor series approximation. The circuit suffer from containing 8 independent current sources that are producing different ratios of the biasing current. The circuit is very susceptible to any changes in the current due to temperature, since the ratio need to stay constant. The design of the exponential function in [57] suffers from being complicated design with a cutoff in the input range mentioned from $-0.4 \mu\text{A}$ to $0.4 \mu\text{A}$ at zero. To achieve the mentioned range the circuit needs to be duplicated with different biasing values. The authors in [58] proposed two exponential circuits. Current-mode and voltage-mode exponential circuits. Both designs consume large amount of power. Similar to the work in [57], the circuit in [59] input range is split into two requiring duplication of the circuit to achieve the full range. In addition

to that the approximation is complicated and thus the circuit is complicated as a result. Also, the circuit is sensitive to temperature but has the advantage of working at very high frequencies up to 5 GHz. The authors in [60] developed an approximated exponential circuit in an FPGA. The design proposed by [61] built an exponential function approximation circuit. The circuit is built using a capacitor and switches with current mirrors. The circuit works by charging and discharging the current in the capacitor to approximate an exponential behavior of the current over time. The authors in [62] used the particle swarm optimization algorithm to approximate the exponential function and build a circuit accordingly. The approximation is very good and with good normalized input range but the circuit is temperature sensitive and uses a capacitor in its design. Various designs used different approximations such as Taylor series, psuedo-Taylor series and many other approximation techniques are introduced in the works [63], [64], [65], [66], [67], [68], [69], [70], [71], [72], [73], [74], [75], [76]. While other works focused on implementing exponential using the CMOS exponential properties in Weak Inversion (WI) region such as the work in [77]. The work in [63] built an exponential function approximation circuit that has a tune able input range by biasing current with the advantage of being simple design but suffers from poor temperature performance. The exponential circuit designs in [64] and [65] have very wide range output range of over 70 dB but similar to [63], they both suffers from temperature and process dependency. An exponential circuit approximation proposed by [66] has an operating frequency of 105 kHz with very high output range of 96 dB with an temperature error of ± 1.27 dB. This temperature error is still considered high in precise application. Also, the design is very complicated. The work in [67] focused on

high speed exponential implementation. Their exponential circuit design operates in frequencies between 70 -150 MHz but the design consumes high power and sensitive to temperature and process variation. The work in [68] focused on designing a low power and simple exponential function approximation using Taylor series. Although the design is simple with low power consumption and can be integrated easily in other circuits, it has low input and output range and very sensitive to PVT variations. The authors in [69] used Op-Amps to implement an exponential current generator. The design suffers of being bulky, high power consumption, inability to be integrated, and the use of around 20 passive components. [70] designed a universal function based on sixth-order Taylor series expansion. The circuit is not optimized for all functions and performance varies for each one. In the case of the exponential the function, the design is sensitive to temperature. The circuit proposed in [71] is an exponential V-I converter that is insensitive to voltage variations with low power consumption. But the design suffers from large area and sensitivity to temperature. Works similar to [71] in the input being different signal from the output are [59],[74], and [77]. These works requires their integration to have voltage to current converters or vice-versa in a current mode or voltage mode circuits. The exponential circuit design in [72] employs the Taylor series expansion approximation for e^x . But the main disadvantage of this design is that, it is extremely sensitive to temperature changes. The design in [73] an exponential function approximation is insensitive to temperature but the transistors are in WI. Similar to [73], the designs in [66], [75], [76], and [77] are operating in WI, making them suitable only for small current and low speed applications. The authors in [74], [75], and [76] have used a complicated approximation methods and

hence complicated designs.

The best work in the literature of exponential and logarithmic function are mentioned in details as follows: [78] proposed a new way to implement the exponential/logarithmic using a combination of square root and linear functions.

The implementations of the log and exponential are as follow in Eq.3.4 and Ea.3.5, respectively.

$$|\ln(x)| \approx 6.529\sqrt{x} - 2.51x - 3.947 \quad (3.4)$$

$$\exp(-x) \approx -1.206\sqrt{x} + 0.2657x + 1.311 \quad (3.5)$$

Where x is the input signal and in this case is the input current. The input range and output range for each function is normalized to the bias current. The input range for exponential is 3.0 and 1.0 for the logarithmic function. [78] circuit consists of the block diagram shown in Fig.3.3.

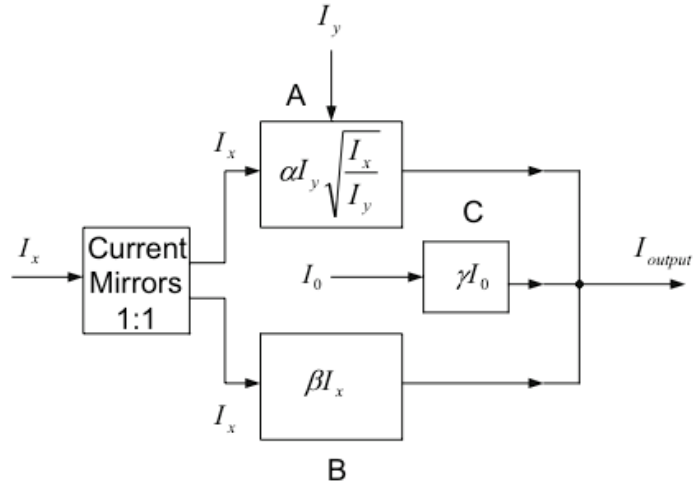


Figure 3.3: Block diagram of the circuit to approximate the exponential/logarithmic.

[78]

The Circuit used to realize the square root is shown in Fig.3.4.

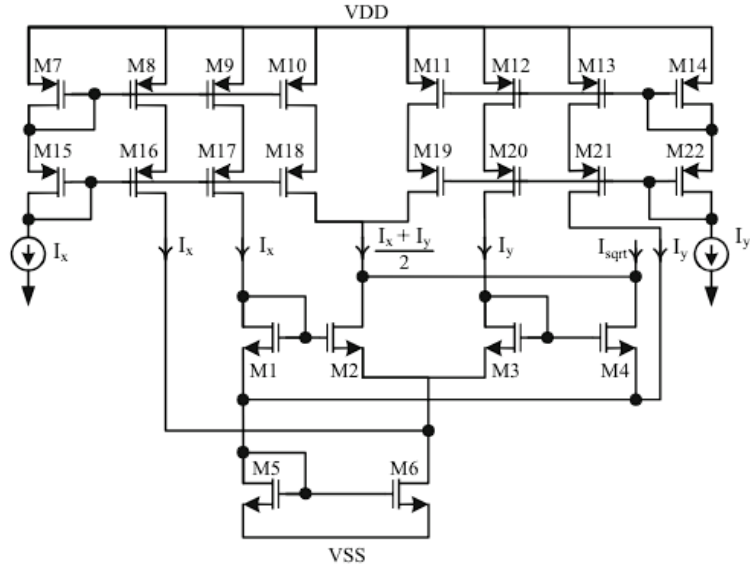


Figure 3.4: Circuit to produce the square root needed for the exponential/logarithmic.[78]

$$\exp(-x) \approx 0.19x^2 - 0.82x + 1 \quad (3.9)$$

The circuit is a better approximation compared to [78], but it has lower input range. The two circuits follow the same idea with the remove of the term x^2 to achieve better input range with minimal loss in the accuracy of the approximation.

A recent approximation is proposed [81] using translinear loop configuration. The approximation is using Taylor series expansion up to the square term. The advantage of its circuit that square root circuit is achieved with lower number of transistors. The circuit to produce x^2 and x is shown in Fig.3.6 and Fig.3.7, respectively. The square and square root circuits are used to realize the exponential function.

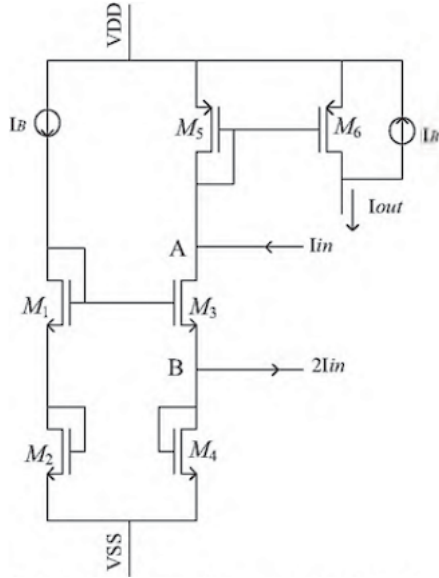


Figure 3.6: Circuit to square input current.[81]

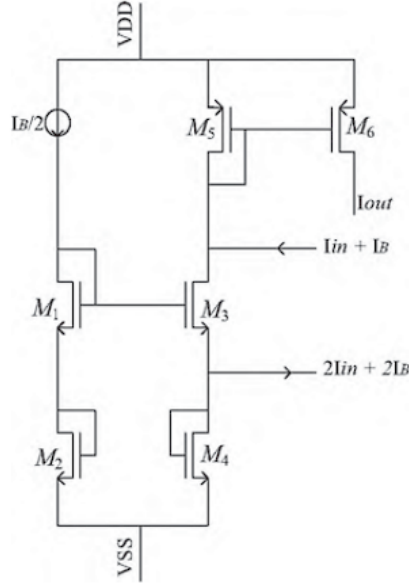


Figure 3.7: Circuit to produce square root of the input current.[81]

For the logarithmic function , the circuit shown in Fig.3.8 shows the complete implementation of the logarithmic generator. The work suffers from low normlized input range of 0.5 for both the exponential and logarithmic.

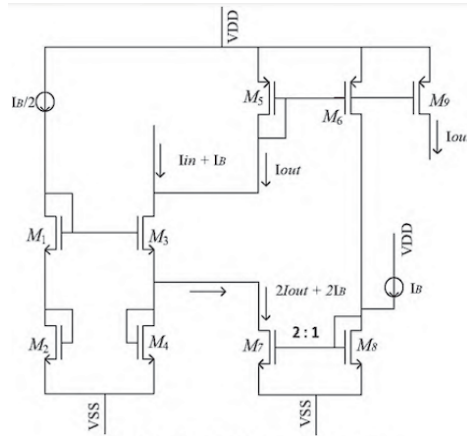


Figure 3.8: Circuit to produce logarithmic function approximation of the input current.[81]

The design in [82] is another exponential approximation. The new current-mode

CMOS exponential generator operates in the Weak Inversion (WI) region. The design has low power consumption of only 4.92 μW , and low supply voltage ($\pm 0.65\text{ V}$). The proposed circuit achieves an extensive output range of 146.5 dB, with a silicon area requirement of 0.0126 mm^2 . The design suffers from very low input range -46 nA to 125 nA only.

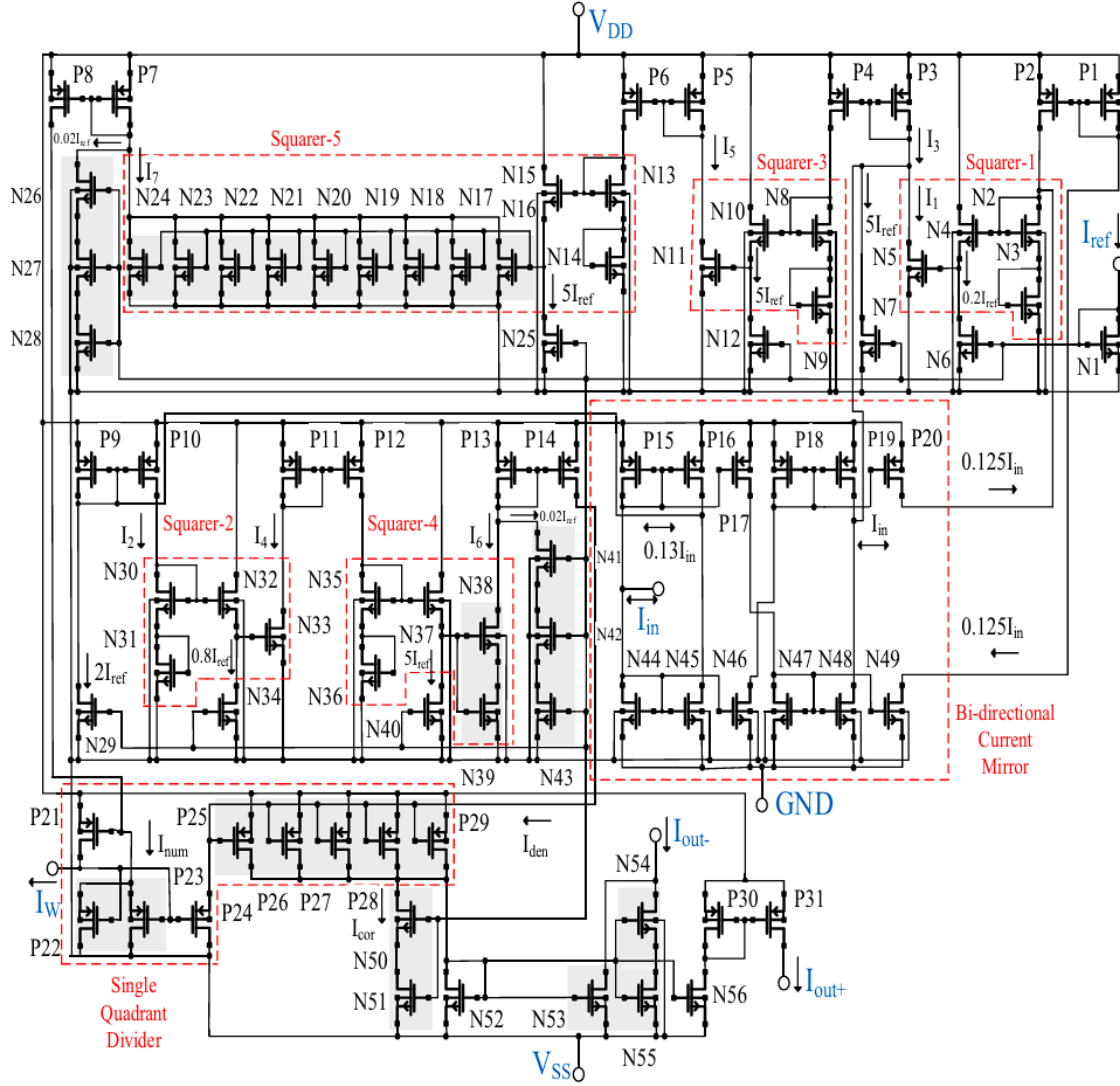


Figure 3.9: Circuit to produce exponential function approximation of the input current in weak inversion region.[82]

A work on providing an exponential function with variable gain and temperature independent is done by [83]. The design is insensitive to temperature over a range of 100 degrees Celsius and have good linearity with 96 dB output dynamic range. But similarly to [82], the input range is in nA range from around -140 nA to 140 nA.

Other works that can be considered are the designs of squarer, root function. Since these designs can be used in approximating exponential and logarithmic functions.

The authors in [84] proposes a multiplier circuit. This circuit uses two squaring circuits to square the addition and subtraction of two currents $(I_x + I_y)^2$ and $(I_x - I_y)^2$ then add the two results to achieve multiplication. The circuit is shown in Fig.

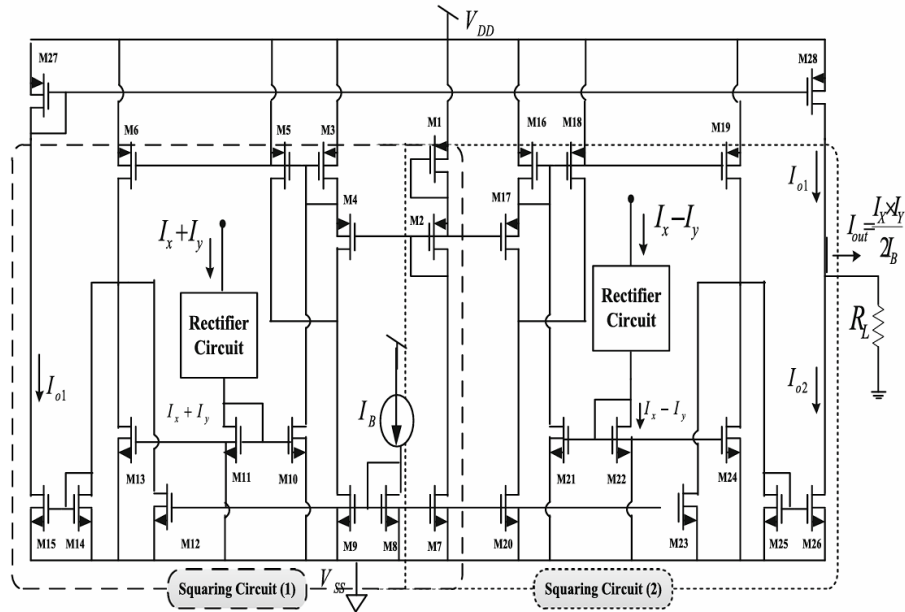


Figure 3.10: Circuit used to multiply I_x and I_y [84].

This circuit needs a rectifier stage. Also, it has the issue of large area and high power consumption. The best implementation found in literature from speed, simplicity and compactness is [47]. The design in [47] will be used as basis for the proposed

CTC design. The design had a major issue that it is PVT dependent making this design use of as an inverse function not appealing but a solution for the PVT dependency is proposed making the new design has all the advantages of the old design while being PVT independent.

The design of [47] simulations and PVT dependency is discussed in details as follows:

The work of [47] builds logarithmic/Exponential function circuits using Taylor series approximation given in equations (3.10) and (3.11).

$$\ln(x) \approx (x - 1) - \frac{1}{2}(x - 1)^2 \quad (3.10)$$

$$e^x \approx 1 + x + \frac{1}{2}x^2 \quad (3.11)$$

Realization of the function in equation (3.10) will require a basic cell to provide the needed terms and current mirrors to scale up or down the current values. The block diagram of the proposed design to realize logarithmic function using MOS in strong inversion is show in Fig.3.11[47]. However, the design is very sensitive to process, voltage and temperature variations (PVT) as will be heightened later on.

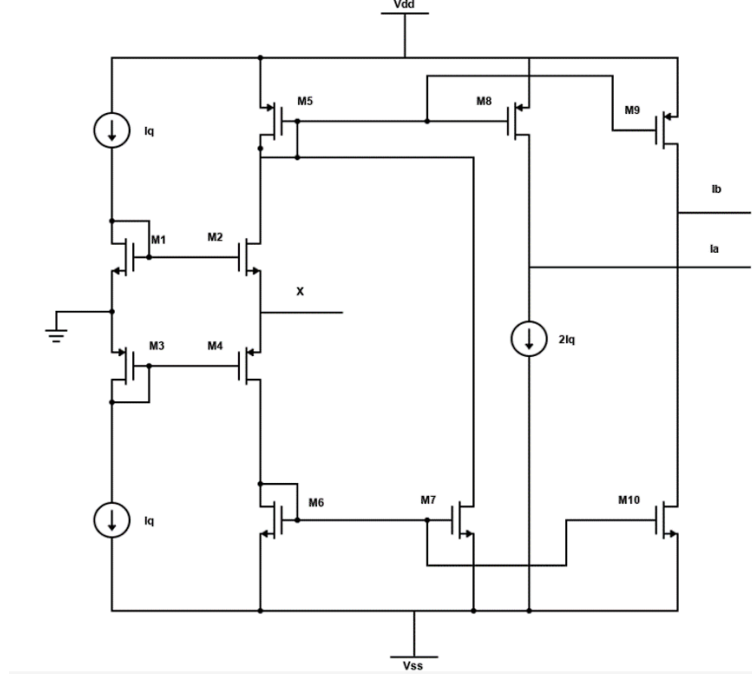


Figure 3.11: Circuit used to generate x^2 and x [47].

with reference to Fig.3.11 and assuming that M1 and M2 as well as M3 and M4 are well matched. By applying the translinear principle in [85], the equation of I_A and I_B are obtained as follows:

$$2\sqrt{I_q} = \sqrt{I_{D2}} + \sqrt{I_{D4}} \quad (3.12)$$

$$I_{D2} + x = I_{D4} \quad (3.13)$$

By combining equation Eq.3.12 and Eq.3.13, the currents I_{D2} and I_{D4} can be expressed as shown in Eq.3.14 and Eq.3.15, respectively.

$$\frac{I_{D2}}{I_q} = 1 - \frac{1}{2} \frac{x}{I_q} + \left(\frac{x}{4I_q}\right)^2 \quad (3.14)$$

$$\frac{I_{D4}}{I_q} = 1 + \frac{1}{2} \frac{x}{I_q} + \left(\frac{x}{4I_q}\right)^2 \quad (3.15)$$

The current in M5 can be expressed using KCL as follows:

$$\frac{I_{D5}}{I_q} = 2 + \frac{1}{8} \left(\frac{x}{I_q}\right)^2 \quad (3.16)$$

Finally, I_A and I_B can be expressed as seen in Eq.3.17 and Eq.3.18, respectively.

$$\frac{I_A}{I_q} = \frac{1}{8} \left(\frac{x}{I_q}\right)^2 \quad (3.17)$$

$$\frac{I_B}{I_q} = \frac{\frac{1}{2}I_{D5} - I_{D4}}{I_q} = -\frac{1}{2} \frac{x}{I_q} \quad (3.18)$$

Where I_A and I_B are the output currents of the basic cell. I_q is the biasing current and x is the input current. This basic cell circuit generates x and x^2 needed for the Taylor series expansion approximation for exponential and logarithmic. The output currents I_A and I_B graphs are seen in Fig.3.12 and Fig.3.13, respectively.

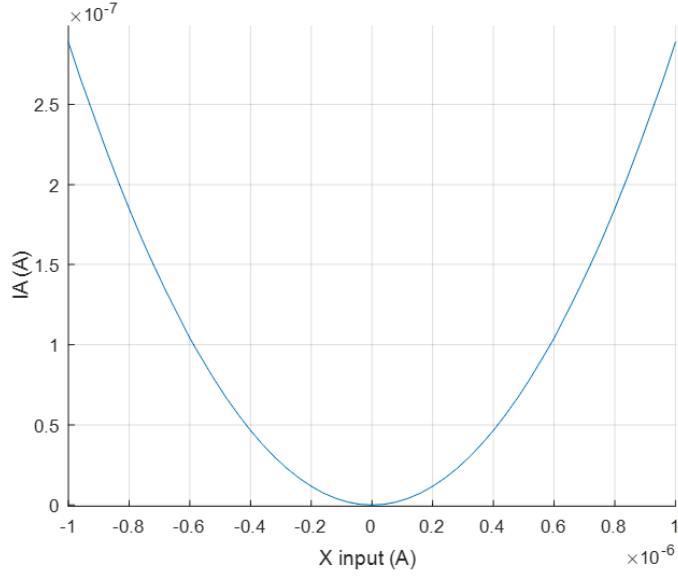


Figure 3.12: Output current I_A [47].

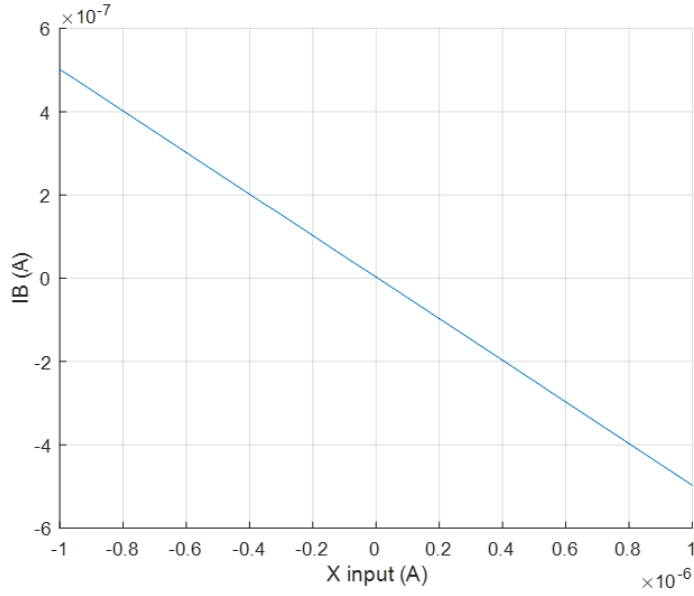


Figure 3.13: Output current I_B [47].

The block diagram for each of the logarithmic and exponential functions are seen in Fig3.14 and Fig3.15, respectively.

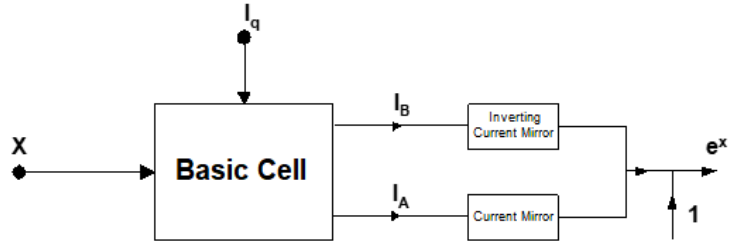


Figure 3.14: Block diagram of exponential circuit implemented [47].

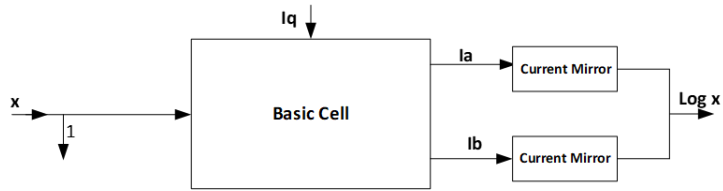


Figure 3.15: Block diagram of the proposed logarithmic function [47].

The resulting exponential and logarithmic are good and follows Taylor series exactly as seen in Fig.3.16 and Fig.3.17.

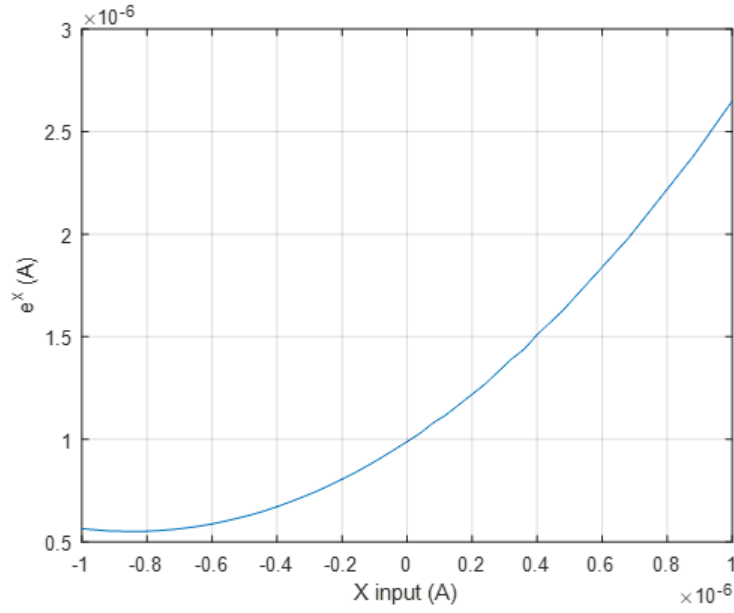


Figure 3.16: Results of realization of the approximated exponential using basic cell [47].

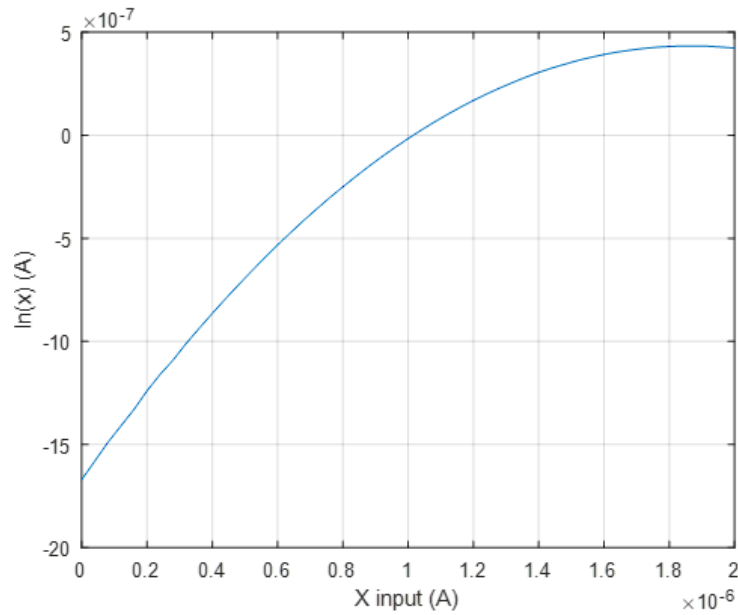


Figure 3.17: Results of realization of the approximated $\ln(x)$ using basic cell [47].

But this current mirror suffers from a high temperature dependency due to the

current squarer. This effect can be modeled as a variation in x due to temperature.

The equations of the two with temperature effect of the output currents I_A and I_B

can be derived as follows:

$$\frac{I_{D2}}{I_q} = 1 - \frac{1}{2} \frac{x + \Delta t}{I_q} + \left(\frac{x + \Delta t}{4I_q} \right)^2 \quad (3.19)$$

$$\frac{I_{D4}}{I_q} = 1 + \frac{1}{2} \frac{x + \Delta t}{I_q} + \left(\frac{x + \Delta t}{4I_q} \right)^2 \quad (3.20)$$

Combing equations (3.19) and (3.20), the drain current of M5 is given by:

$$\frac{I_{D5}}{I_q} = \frac{I_{D2} + I_{D4}}{I_q} = 2 + \frac{1}{8} \left(\frac{x + \Delta t}{I_q} \right)^2 \quad (3.21)$$

The current I_b is given by:

$$\frac{I_b}{I_q} = \frac{\frac{1}{2}I_{D5} - I_{D4}}{I_q} = -\frac{1}{2} \frac{x + \Delta t}{I_q} \quad (3.22)$$

By subtracting a constant current $= 2I_q$ from I_{D5} , the current I_a can be expressed

as

$$\begin{aligned} \frac{I_a}{I_q} &= \frac{I_{D2} + I_{D4}}{I_q} - 2 = \frac{1}{8} \left(\frac{x + \Delta t}{I_q} \right)^2 \\ &= \frac{1}{8} \frac{x^2 + 2\Delta tx + \Delta t^2}{I_q^2} \end{aligned} \quad (3.23)$$

The effect of temperature can be seen in Fig.3.18 and Fig.3.19.

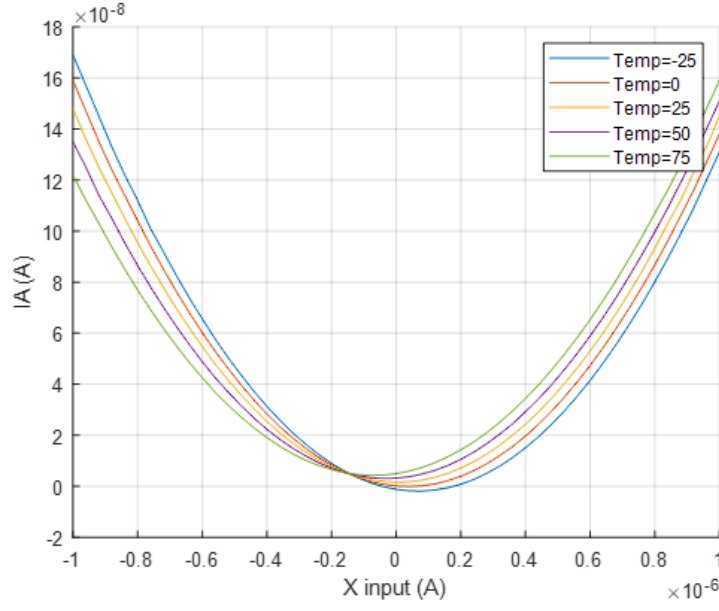


Figure 3.18: Effect of temperature on I_A [47].

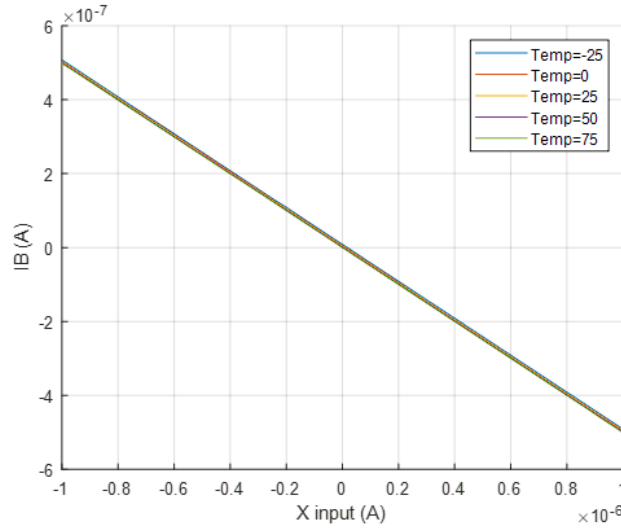


Figure 3.19: Effect of temperature on I_B [47].

As seen from above figures the effect of temperature on I_A is significant, while the effect of temperature on I_B is negligible. This is due to the squaring. By expanding

the square term $(x + \Delta t_x)^2$ we obtain $x^2 + 2x\Delta t_x + \Delta(t_x)^2$. The main contributor to the temperature dependency is the middle term $2x\Delta t_x$. This can be seen clearly from Fig.3.18. By following one trace (temp=75), It is seen that I_A values go below the trace (temp=25) when the value of $2x\Delta t_x$ is negative and above when the value is positive.

The effect is clearly seen affecting the implementation of exponential and logarithmic functions using this basic as seen in Fig.3.20 and Fig.3.21. It is evident that both circuits are temperature dependant. Finally, Fig.3.22 and Fig. 3.23 show the resultant inverse function and its temperature analysis, respectively.

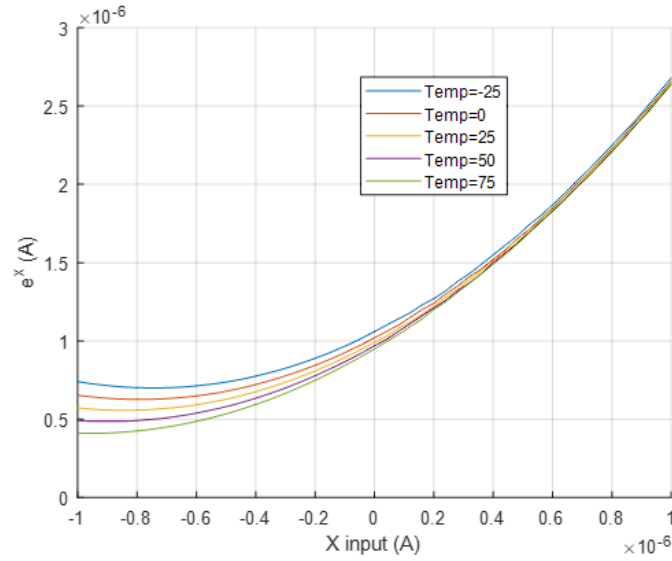


Figure 3.20: Temperature performance for exponential circuit in [47].

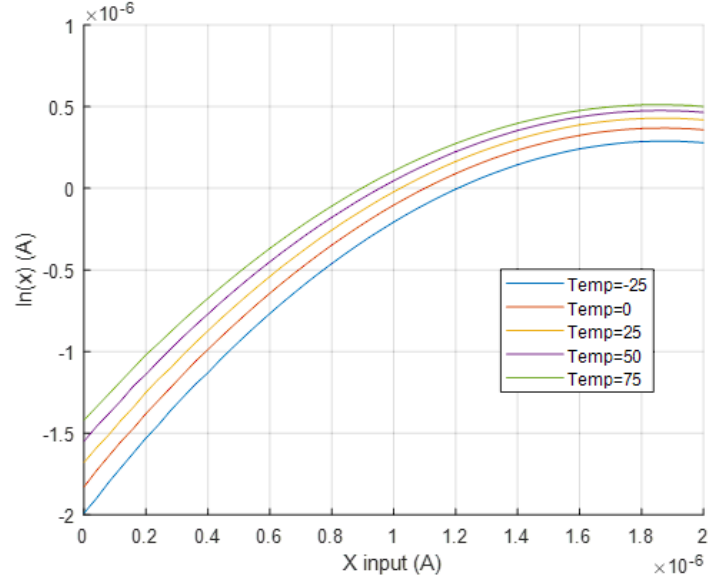


Figure 3.21: Temperature performance for the logarithmic circuit in [47].

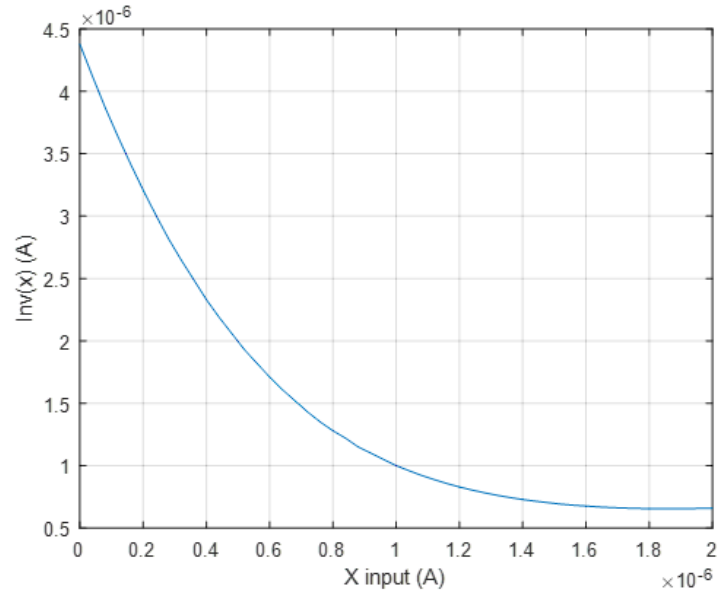


Figure 3.22: Results of realization of $\text{inv}(x)$ using $\text{exp}(x)$ and $\text{ln}(x)$ built with basic cell before modification [47].

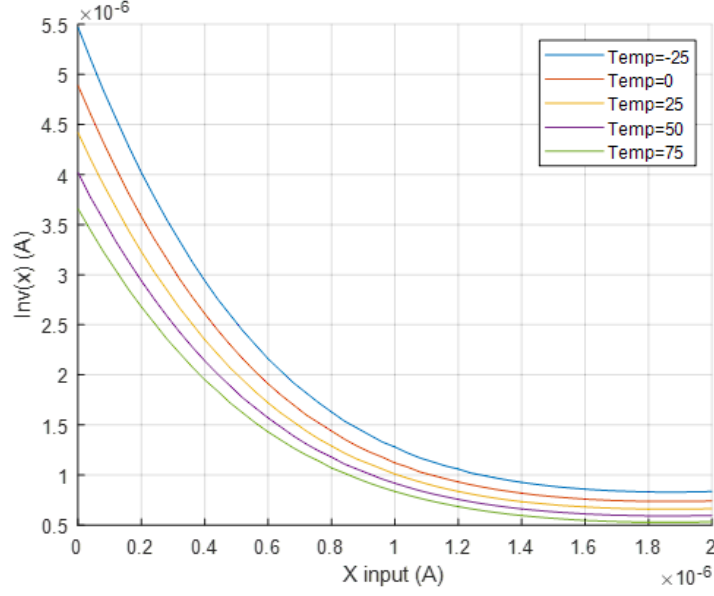


Figure 3.23: Temperature performance before the improvement [47].

3.2 Proposed Basic Cell for PVT independent implementation of Exponential/logarithmic functions

The issue of temperature dependency due to the middle term is solved by making the circuit input two-ended. With reference to Fig.3.24, the current (x) is applied to node 1 and the negative of it ($-x$) is applied to node 2.

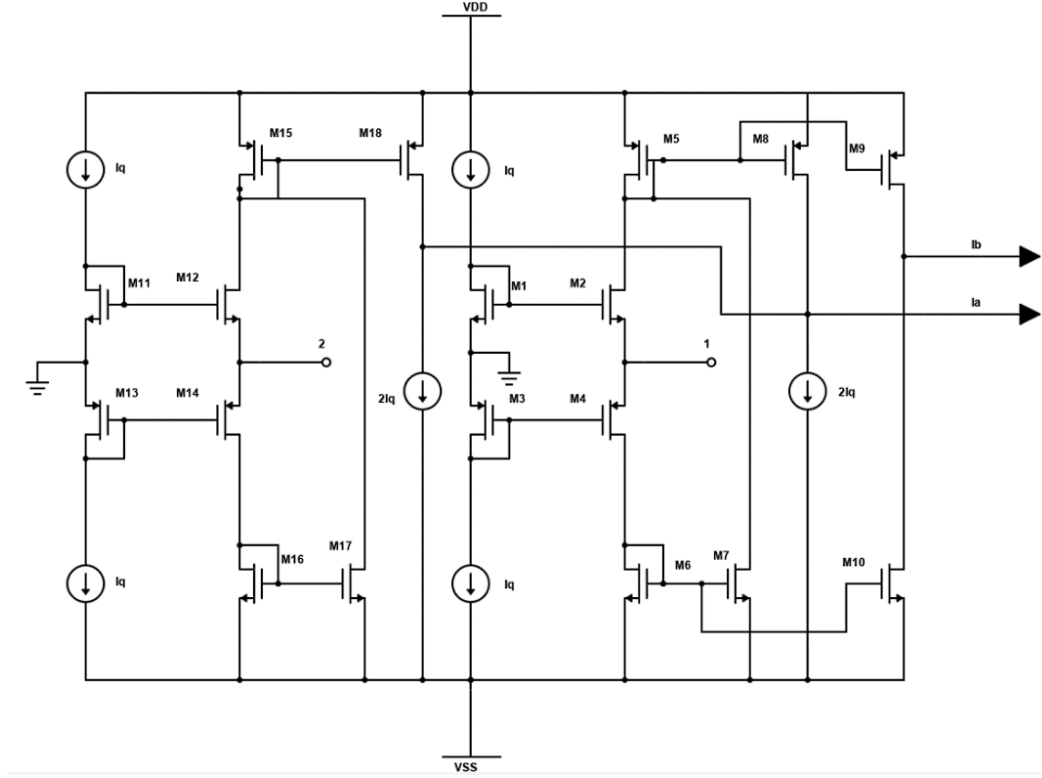


Figure 3.24: Proposed Basic Cell

The new resulting output currents I_A and I_B can be derived easily to be:

$$\frac{I_a}{I_q} = \frac{1}{4} \left(\frac{x}{I_q} \right)^2 \quad (3.24)$$

$$\frac{I_b}{I_q} = \frac{\frac{1}{2} I_{D5} - I_{D4}}{I_q} = -\frac{1}{2} \frac{x}{I_q} \quad (3.25)$$

The temperature effect on I_A and I_B are as shown in 3.26 and 3.27.

$$\begin{aligned}
\frac{I_a}{I_q} &= \frac{I_{D2} + I_{D4}}{I_q} + \frac{I_{D12} + I_{D14}}{I_q} - 4 \\
&= \frac{1}{8} \left(\frac{x + \Delta t}{I_q} \right)^2 + \frac{1}{8} \left(\frac{-x + \Delta t}{I_q} \right)^2 \\
&= \frac{1}{4} \frac{x^2 + \Delta t^2}{I_q^2}
\end{aligned} \tag{3.26}$$

$$\frac{I_b}{I_q} = \frac{\frac{1}{2}I_{D5} - I_{D4}}{I_q} = -\frac{1}{2} \frac{x + \Delta t}{I_q} \tag{3.27}$$

In Equation (3.26), the term $2\Delta tx$ is canceled. This indicates that the current I_a is almost insensitive to temperature fluctuation. That is because the term Δt is small and squaring it will make it much smaller. The simulation results provided later confirms the theory. The aspect ratio of the transistor in Fig.3.24 are given in Table 3.1.

Table 3.1: Sizes of all transistors used in the design of the basic cell shown in Fig.3.24

Transistor	M1&M11	M2&M12	M3&M13	M4&M14	M5&M15	M6&M16	M7&M17	M8&M18	M9	M10
L(μm)	18	18	4.35	4.35	6	13.2	13.44	6.06	6	13.35
W(μm)	3	3	3	3	6	6	6	6	2.94	6

The new I_A can be seen in Fig.3.25

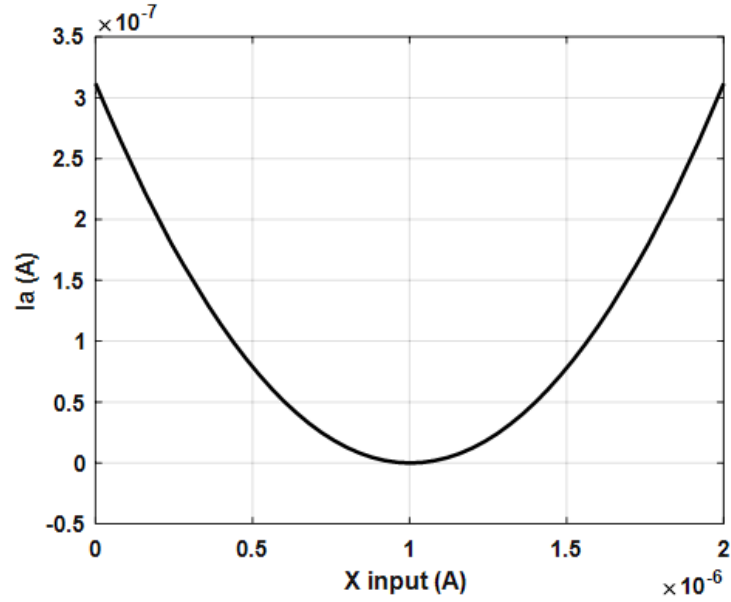


Figure 3.25: Output current after modification on I_A

The basic circuit is simulated for temperature analysis. The temperature was varied from -25°C to 75°C . Plots of the current I_a as a function of x for different temperature are shown in Fig. 3.26. It is evident from the figure that the current I_a is almost insensitive to the temperature variations. Where the maximum temperature variation error is around 2%

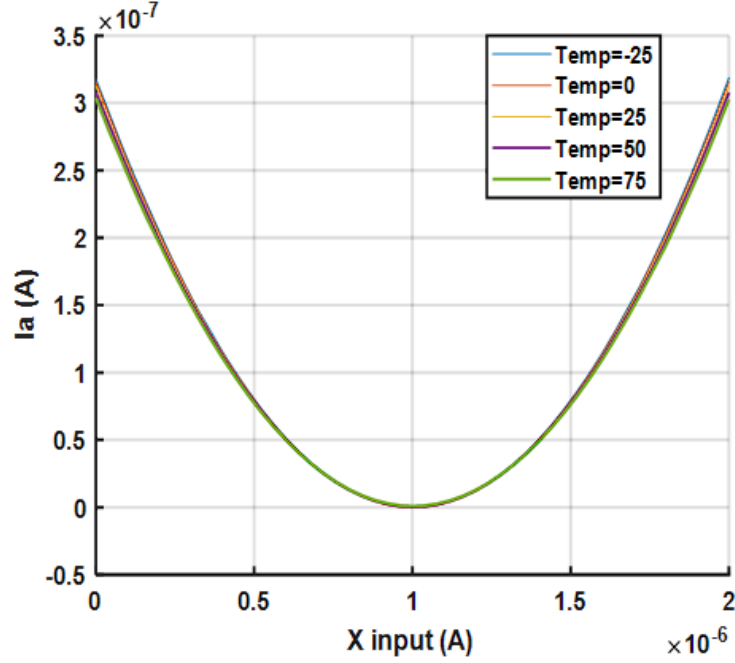


Figure 3.26: Effect of temperature after modification on I_A

The basic cell corner simulation was performed, and the plots of I_a are displayed in Fig.3.27. The plots clearly show that the cell is functioning normally, with a constant shift up or down around the normal case. The maximum error of the process variation is found to be 5%. The process variation simulation is performed to check the circuit functionality with slight error in manufacturing and to ensure the circuit is robust to the variations. Finally, the results of I_B and corner simulation are shown in Fig.3.28. The temperature and process variation on I_B is even less than I_A .

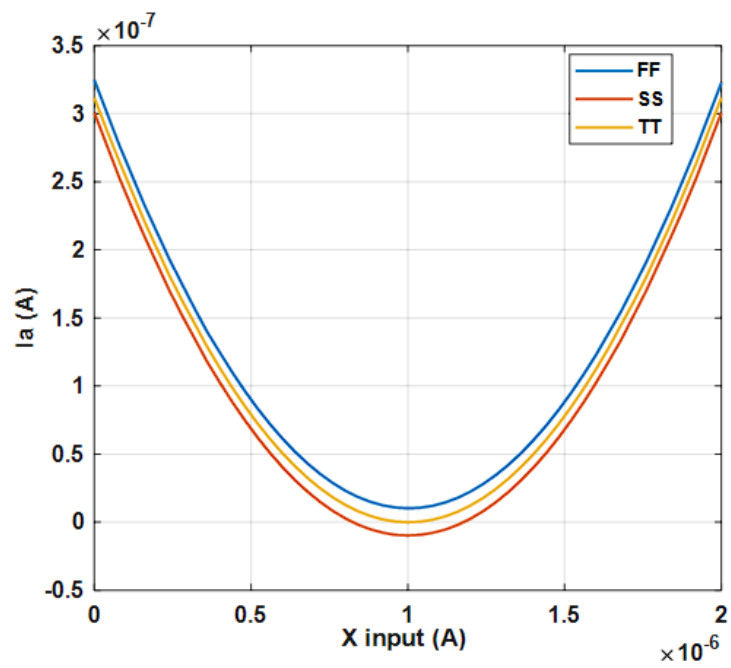
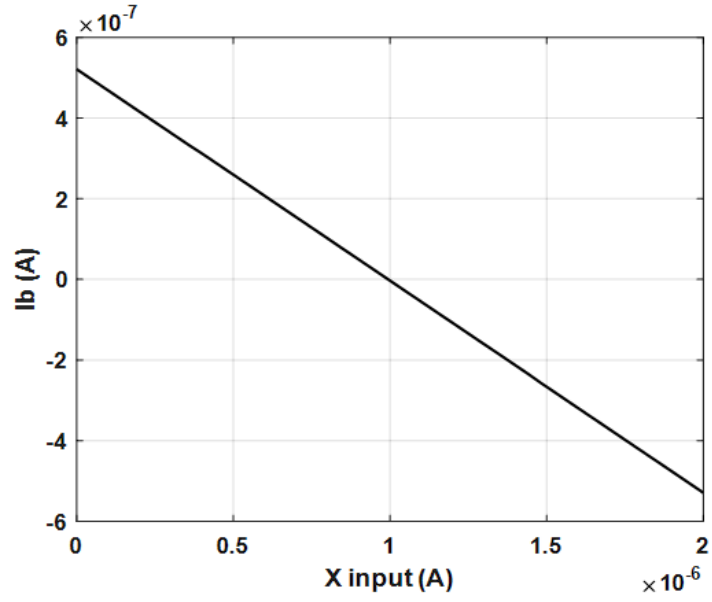
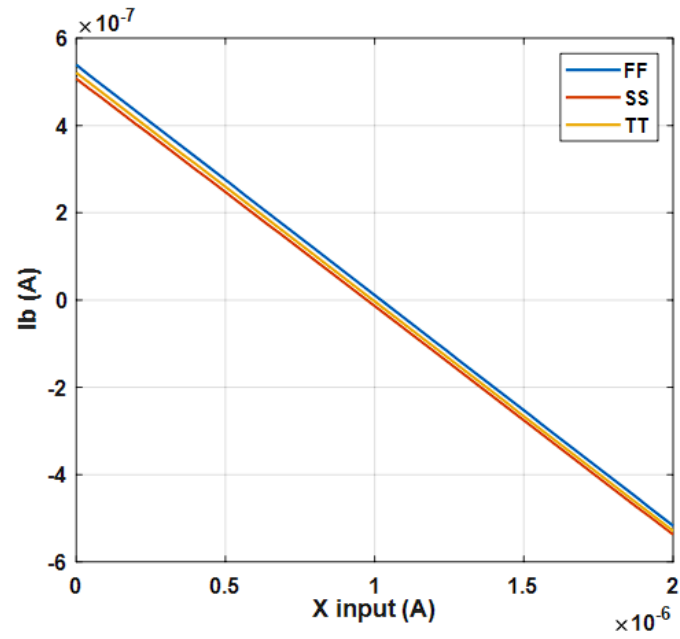


Figure 3.27: Corner Analysis of IA



(a)



(b)

Figure 3.28: (a) Plot of I_B (b) Effect of process variation on I_B of the proposed circuit

3.2.1 Performance Analysis

The previous given analysis for the basic cell is under the assumption that the transistors M1-M4 in Fig. 3.24 are working in saturation and obeys perfect square-law equation. Also, the assumption of nMOS and pMOS transconductance are equal. The perfect square-law equation is proven experimentally to a great extent in long channels by [86]. The channel length is chosen to be long to avoid destroying the square-law. But if the circuit is scaled down to short channel length the second-order effects should be taken into consideration such as channel length modulation, body effect, velocity saturation and mobility reduction. This long channel will affect the maximum operating frequency.

This basic cell performance is then tested in the exponential and logarithmic functions approximated implementation.

3.3 Proposed Exponential Function

To build an exponential function using basic circuit shown in Fig. 3.24, a Taylor series approximation is utilized. The exponential approximation is as follows in Eq.3.28

$$e^x \approx 1 + x + \frac{1}{2!}x^2 \quad (3.28)$$

Using this approximation a realization of exponential function is possible using current mirrors to correct the constant. The block diagram showing the implementation is shown in Fig.3.29. The full circuit implementation is shown in Fig.3.30 with the sizes of each transistor in Table.3.2

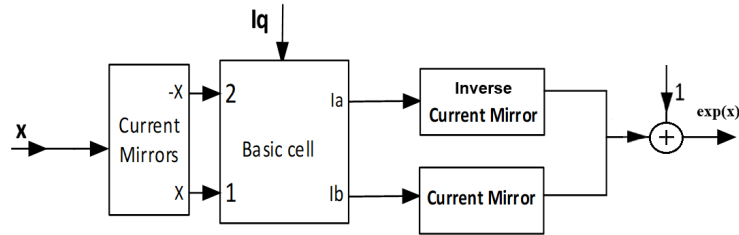


Figure 3.29: Block diagram of exponential circuit implemented.

Where the first block is used to generate x and negative x . The second block is the proposed basic cell. The last current mirrors are used to adjust the current I_A and I_B to achieve the Taylor's approximation.

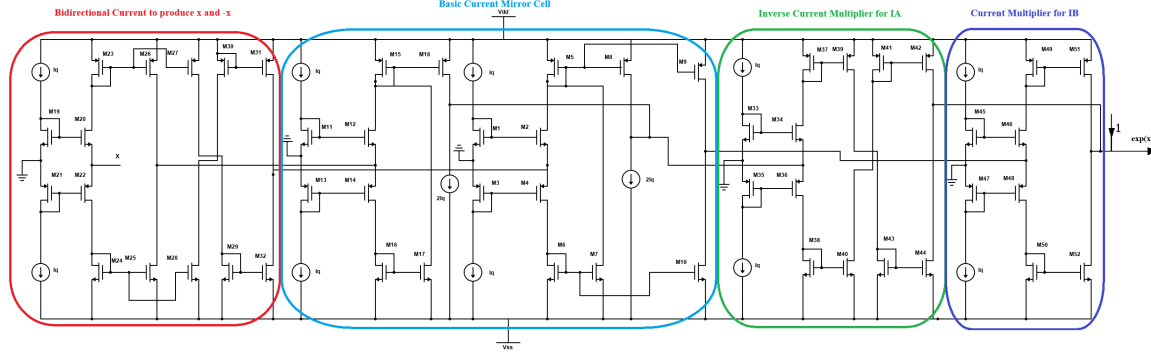


Figure 3.30: The proposed current-mode exponential function generator's circuit schematic

Table 3.2: Sizes of all transistors used in the design of the exponential circuit shown in Fig3.30.

Transistor	L(μm)	W(μm)
M19,M20,M24,M25,M28,M29,M32,M33,M34,M38,M45,M46,M50	2	2
M21,M22,M23,M26,M27,M30,M31,M35,M36,M47,M48	2	4
M37	2.035	4
M39,M41,M42	2	6.205
M40,M43,M44	2	3.105
M49	2.095	4
M51	2	7.3
M52	2	3.65

3.3.1 Simulation Results

The results of using the basic cell are shown in Fig.3.31 and Fig.3.32. Fig.3.31 shows the values of the realization of exponential using the basic cell, while Fig.3.32 shows the value variation in the exponential due to temperature.

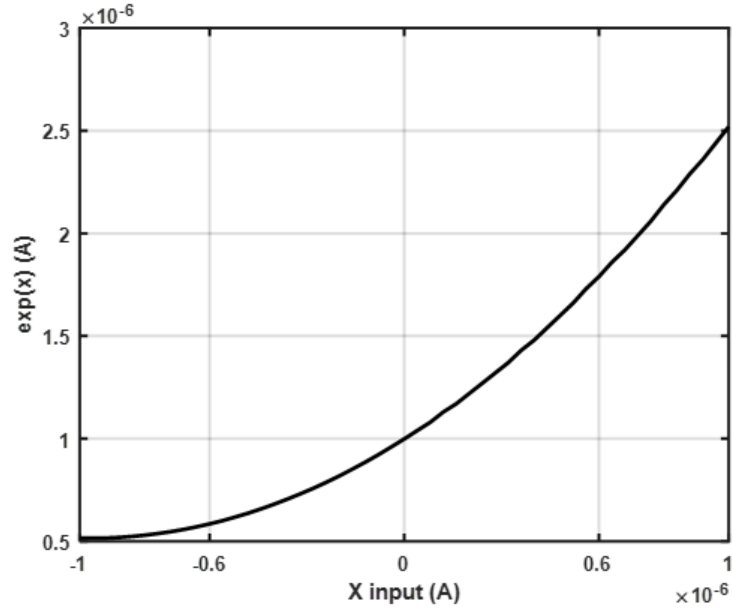


Figure 3.31: Results of realization of exponential using proposed basic cell.

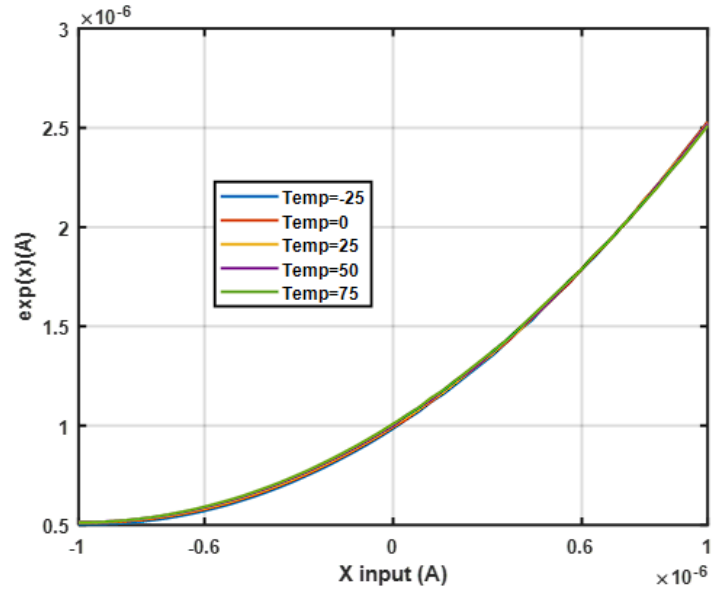


Figure 3.32: Temperature performance using the proposed basic cell.

Fig.3.32 shows that the exponential circuit is immune to temperature variation from -25°C to 75°C . The corner analysis is done on the circuit and shown in Fig.3.33

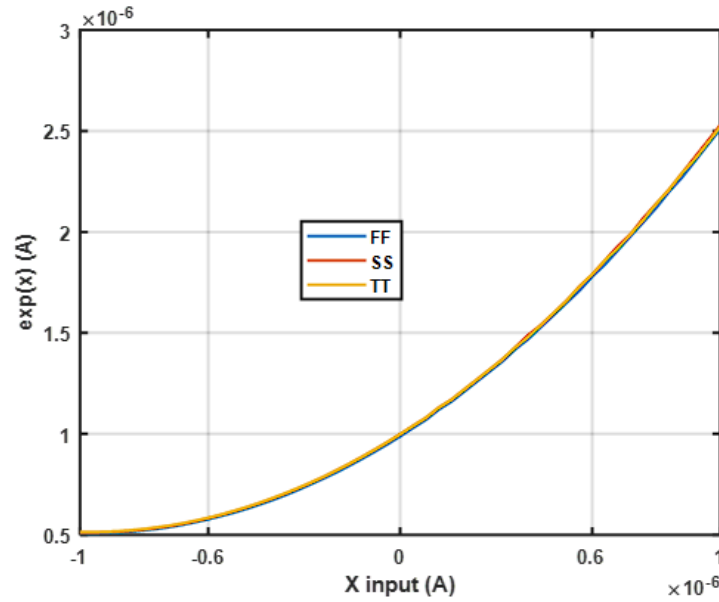


Figure 3.33: Plots for corner analysis of exponential circuit

From Fig.3.33, it is clear that the exponential circuit is immune to process as well.

The frequency range of the circuit is found using AC analysis simulation. Plots of the simulation is shown in Fig.3.34. The circuit 3 dB cutoff is around 1.25 MHz.

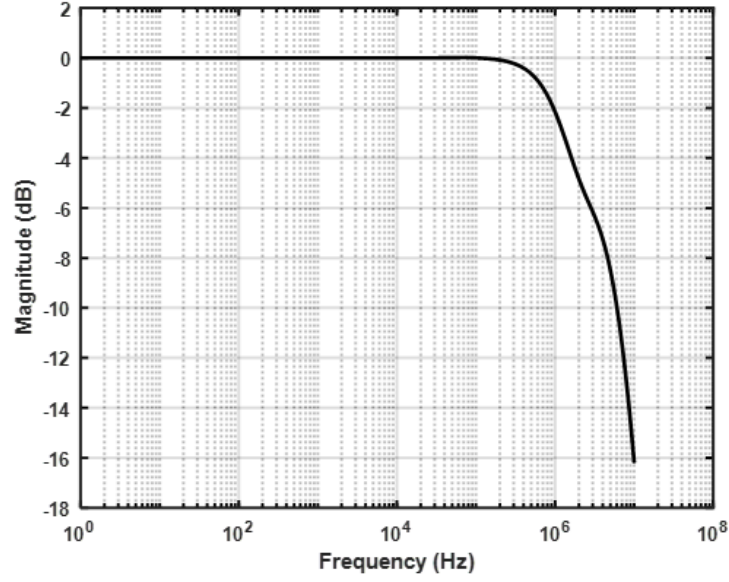


Figure 3.34: Plot of the AC analysis of the exponential circuit

Finally, to test the reliability of the proposed exponential circuit approximation design, the Monte Carlo analysis is performed. The input x is taken to be in the middle of the range of the exponential circuit with 1000 runs of Monte Carlo analysis shown in Fig.3.35. The Monte Carlo analysis is found to be Gaussian with a mean of $1.174 \mu\text{A}$. The standard deviation is calculated to be around $\sigma=12.22 \text{ nA}$. The majority of the samples falls within to 2σ with more than 95% of the samples.

Fig.3.37 shows that the layout is very close to the pre-layout simulation with a slight shift.

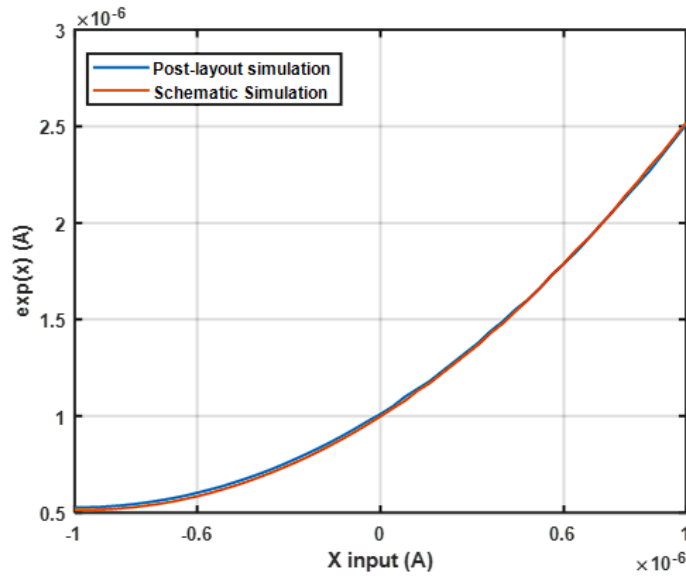


Figure 3.37: Plots of post-layout and schematic of the exponential function.

Similar to schematic various analysis are done to the post-layout. Temperature analysis, corner analysis, and AC analysis simulation are shown in Fig.3.38 - Fig.3.40, respectively. Fig.3.38 shows that the circuit is still almost immune to temperature. Fig.3.39 shows that the function is still the same with a very slight shift due to process. The frequency response shown in Fig.3.40 is similar to the schematic with a 3 dB cutoff frequency around 1.238 MHz, which is less than 1% error. The simulations shows that the post-layout and schematic simulations are very close.

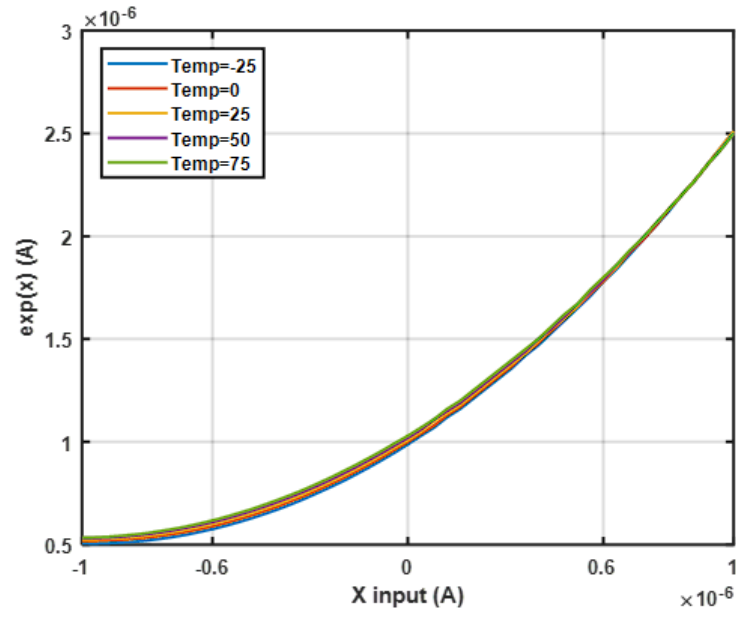


Figure 3.38: Temperature analysis of the extracted view of the exponential circuit

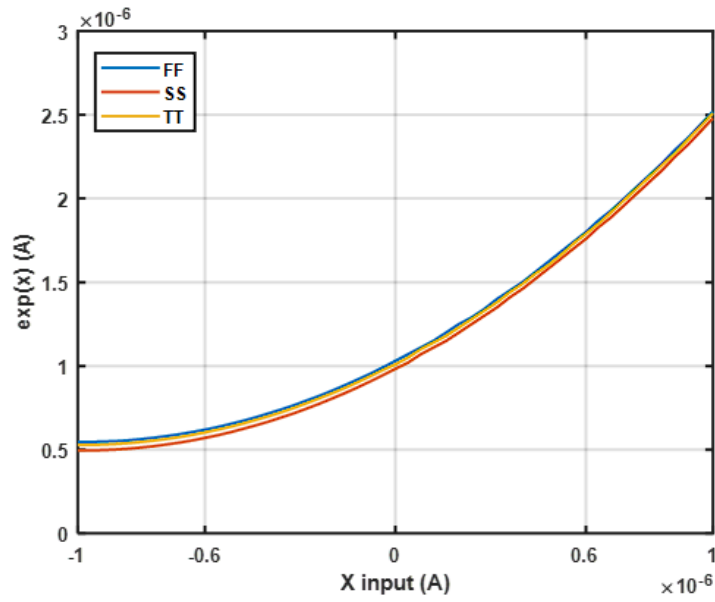


Figure 3.39: Corner analysis of the extracted view of the exponential circuit

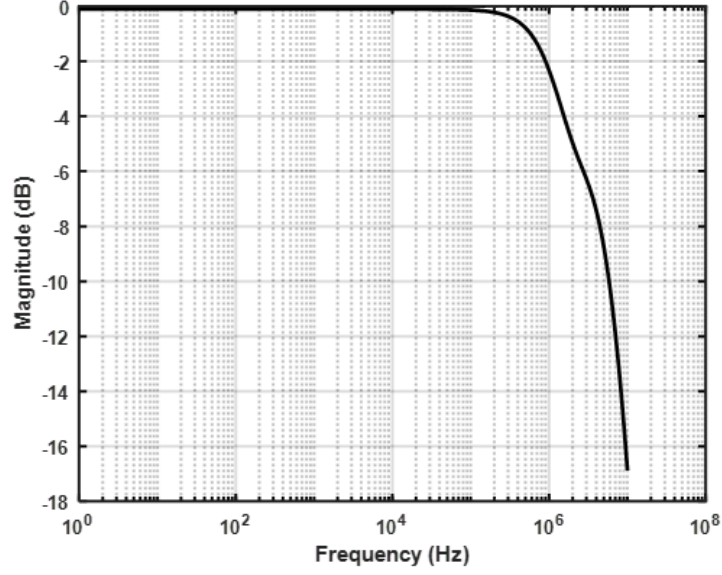


Figure 3.40: AC analysis of the extracted view of the exponential circuit.

Finally, to test the reliability of the post-layout of proposed exponential circuit approximation design, the Monte Carlo analysis is performed. The input x is taken to be in the middle of the range of the exponential circuit with 1000 runs of Monte Carlo analysis shown in Fig.3.41. The Monte Carlo analysis is found to be Gaussian with a mean of $1.181 \mu\text{A}$. The standard deviation is calculated to be around $\sigma=12.08 \text{ nA}$. The majority of the samples falls within to 2σ with more than 95% of the samples.

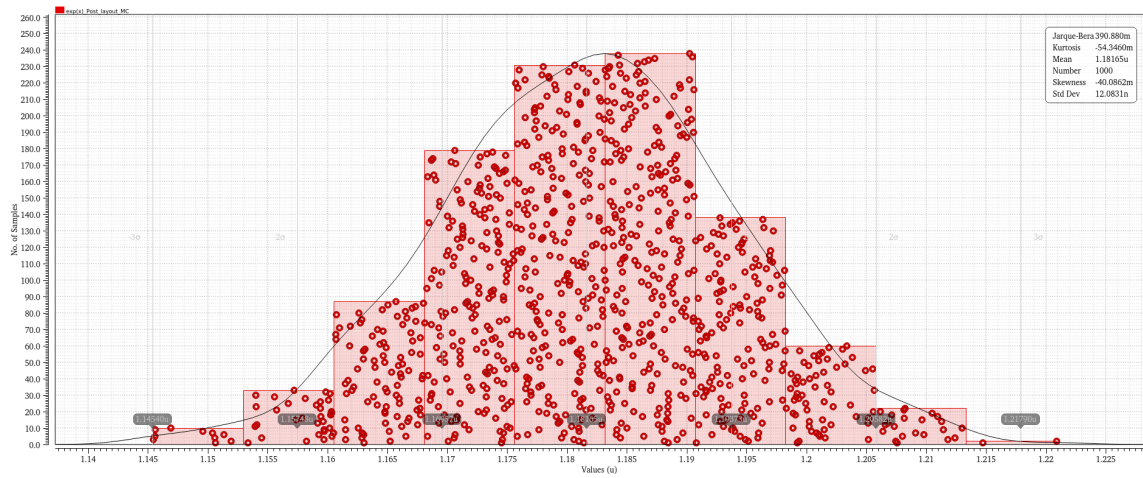


Figure 3.41: Histogram of the Monte Carlo simulation of the exponential function post-layout showing the number of samples at input $x= 0 \mu A$

The exponential circuit design was compared to earlier artwork and summarized in Table 3.3. It is evident from the table that the proposed design outperforms all other designs.

Table 3.3: Summary of exponential circuits comparison

Author	[74]	[77]	[75]	[59]	[76]	This work
Technology (um)	0.18	0.35	0.18	0.18	0.18	0.18
Year	2017	2012	2017	2016	2021	2024
Operation region	SI	WI	WI	SI	WI	SI
Supply Voltage (V)	± 0.75	1.5	± 0.5	± 0.75	± 0.65	± 1.25
I/P : O/P Signals	Current : Voltage	Voltage : Current	Current : Current	Current : Voltage	Current : Current	Current : Current
Normalized input range	± 3.7	± 3.7	± 3	± 4	-4.6:12.55	± 1
Approximation used	$0.04 - 0.013x + (1 + 0.25x)^2$ $0.04 + 0.013x + (1 - 0.25x)^2$	Exact (no approximation)	$0.155 + (1 + 0.28x)^2$ $0.155 + (1 - 0.28x)^2$	$\frac{x^2 + 10x + 28}{e^2(x^2 - 2x + 4)}$ and $\frac{e^2(x^2 + 2x + 4)}{x^2 - 10x + 28}$	$0.004 + [1 + 0.2x + (0.125x)^2]^4$ $0.004 + (1 - 0.065x)^4$	$1 + x + \frac{1}{2}x^2$
Temperature range	Not mentioned	-10 : 70	-60 : 50	-40 : 125	-10 : 75	-25 : 75
Temperature error (dB)	Not mentioned	± 3	± 2.5	± 4.7	± 3	± 0.13
Bandwidth (MHz)	Not mentioned	Not mentioned	0-0.123	0.1-5000	0-0.09	0-1.25

3.3.3 Simulation Vs Theory

A comparison between theory and schematic is done. Plots of $\exp(x)$, approximated $\exp(x)$ and the schematic simulation are shown in Fig.3.42.

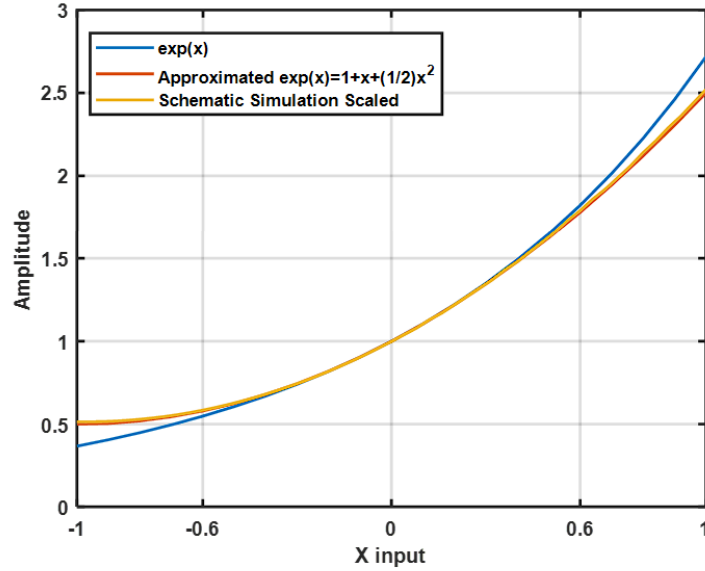


Figure 3.42: Plots of theory, approximated and schematic simulation for $\exp(x)$.

It is clear that the schematic simulation is identical to the approximation. Both simulation and approximation are close to theoretical $\exp(x)$ for values between -0.6 to 0.6. This result is expected since the approximation used (Taylor series) is valid for small values of x around the center value of the approximation ($x=0$ in this case). The exponential circuit can be used as $\exp(x)$ only within the values, where the Taylor series is valid.

3.4 Logarithmic Function

Similar to the exponential the basic cell shown in Fig.3.24 is used to implement the Taylor series approximation. The approximation used is as shown in Eq.3.29.

$$\ln(x) \approx (x - 1) - \frac{1}{2}(x - 1)^2 \quad (3.29)$$

Using this approximation a realization is possible using current mirrors to correct the constant. The block diagram showing the implementation is shown in Fig.3.43. The full circuit implementation is shown in Fig.3.44 with the sizes of each transistor in Table.3.4

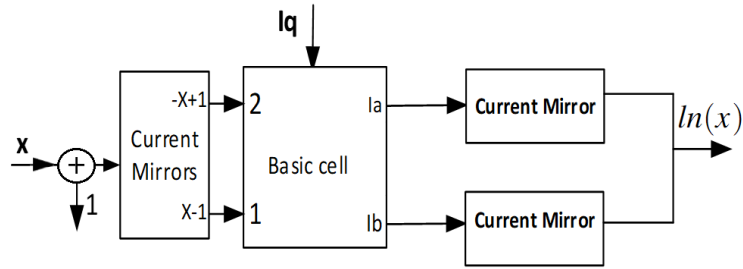


Figure 3.43: Block diagram of logarithmic circuit implemented.

Where the first block is used to generate $(x-1)$ and its negative $(-x+1)$. The second block is the proposed basic cell. The last current mirrors are used to adjust the current I_A and I_B to achieve the Taylor's approximation.

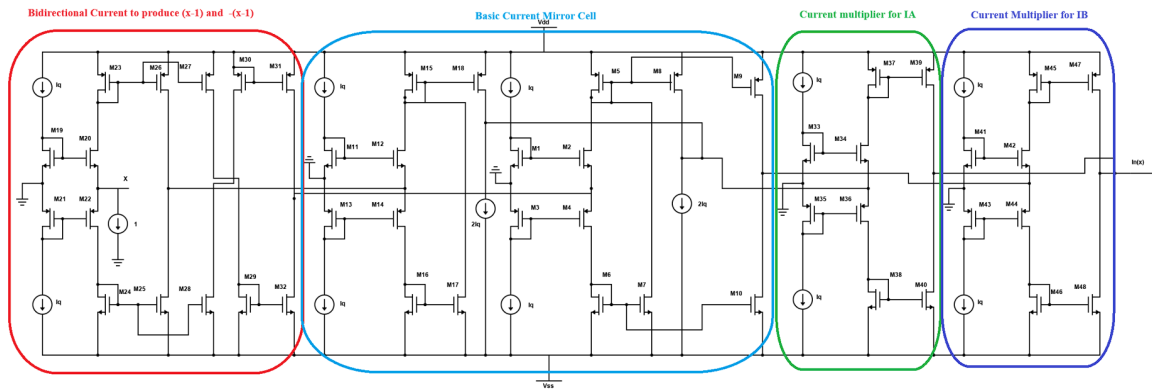


Figure 3.44: The proposed current-mode logarithmic function generator's circuit schematic

Table 3.4: Sizes of all transistors used in the design of the logarithmic circuit shown in Fig3.44.

Transistor	L(μm)	W(μm)
M19,M20,M24,M25,M28,M29,M32,M33,M34,M38,M41,M42,M46	2	2
M21,M22,M23,M26,M27,M30,M31,M35,M36,M43,M44	2	4
M37	2.05	4
M39	2	6.205
M40	2	3.105
M45	2.095	4
M47	2	7.3
M48	2	3.65

3.4.1 Simulation Results

The results of using the proposed basic cell are shown in Fig.3.45 and Fig.3.46. Fig.3.45 shows the values of the realization of logarithmic using the basic cell, while Fig.3.46 shows the value variation in the logarithmic due to temperature.

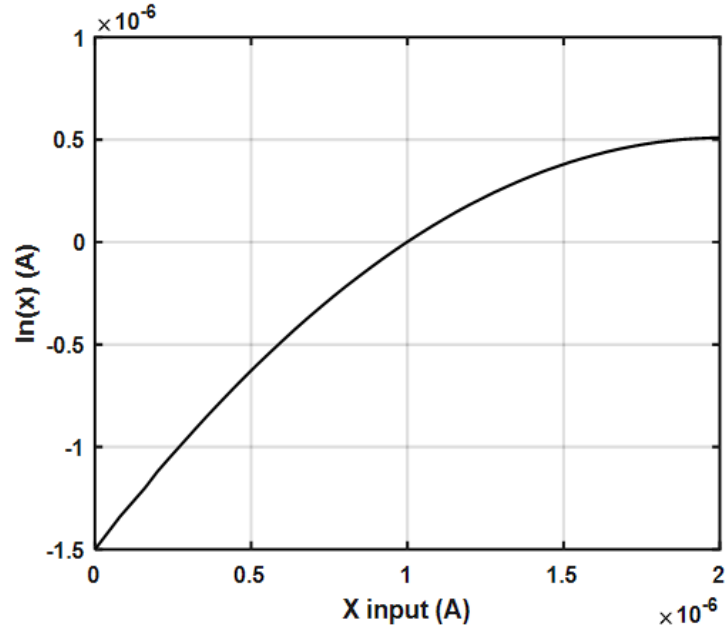


Figure 3.45: Results of realization of logarithmic function using proposed basic cell.

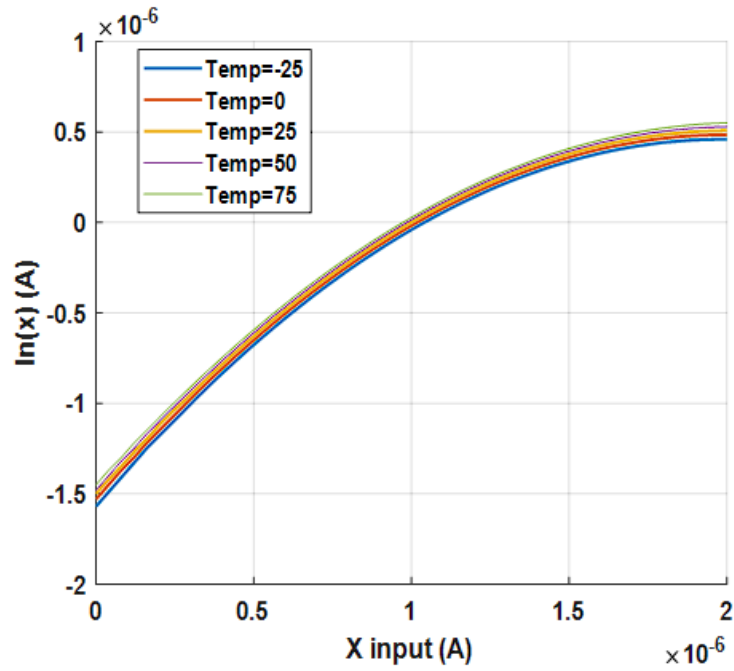


Figure 3.46: Temperature analysis of the logarithmic function using the proposed basic cell.

Fig.3.46 shows that the exponential circuit is almost immune to temperature variation from -25°C to 75°C . The corner analysis is done on the circuit and shown in Fig.3.47

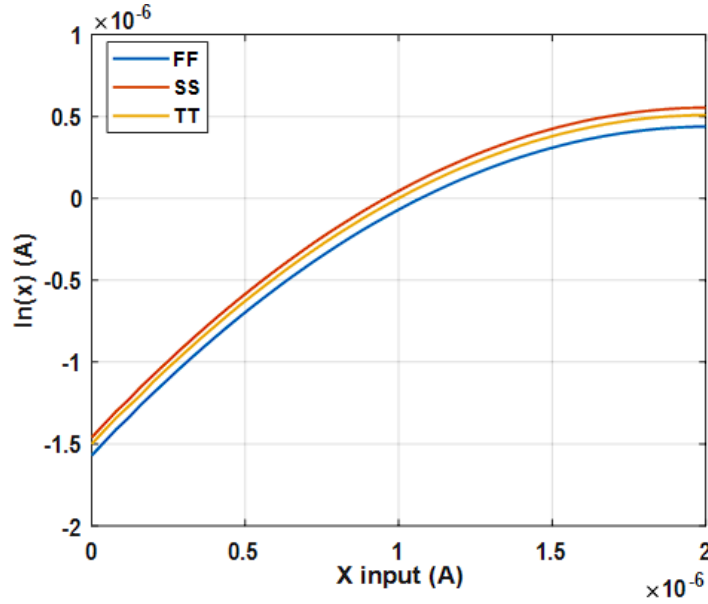


Figure 3.47: Plots for corner analysis of logarithmic circuit

From Fig.3.47, it is clear that the logarithmic circuit is immune to process as well.

The frequency range of the circuit is found using AC analysis simulation. Plots of the simulation is shown in Fig.3.48. The circuit 3 dB cutoff is around 2.8 MHz.

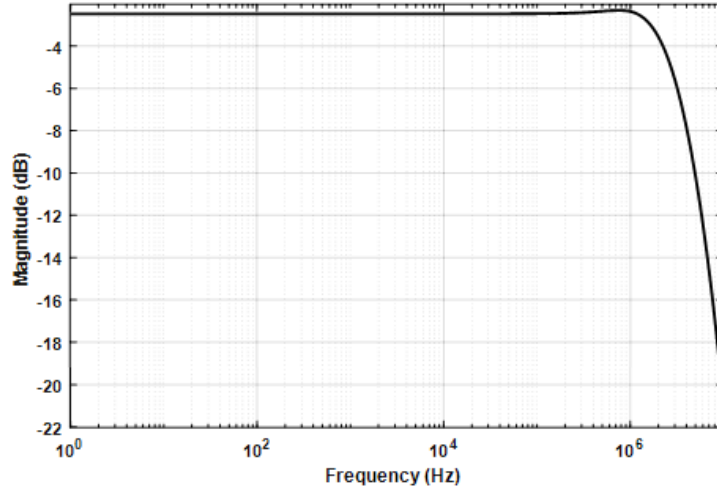


Figure 3.48: Plot of the AC analysis of the logarithmic circuit

Finally, to test the reliability of the proposed logarithmic circuit approximation design, the Monte Carlo analysis is performed. The input x is taken to be in the middle of the range of the logarithmic circuit with 1000 runs of Monte Carlo analysis shown in Fig.3.49. The Monte Carlo analysis is found to be Gaussian with a mean of -164.67 nA. The standard deviation is calculated to be around $\sigma=33.4$ nA. The majority of the samples falls within to 2σ with more than 94% of the samples.

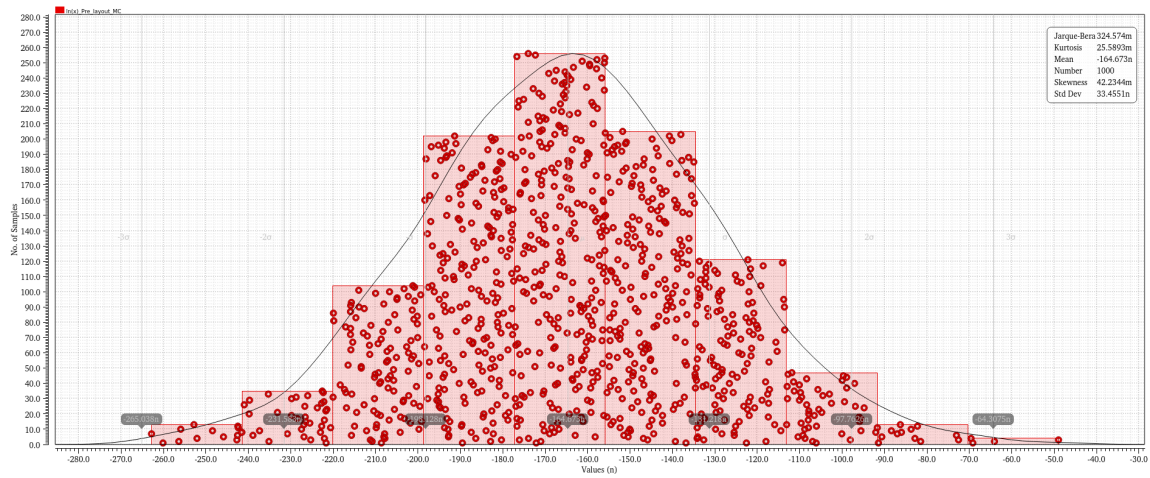


Figure 3.49: Histogram of the Monte Carlo simulation of the logarithmic function schematic showing the number of samples at input $x = 1 \mu A$

3.4.2 Post-layout Simulation Results

The post-layout simulation of the logarithmic circuit is carried and it matches the pre-layout simulation.

The layout of the logarithmic circuit is shown in Fig.3.50. The area of the layout is around $6000 \mu m^2$.

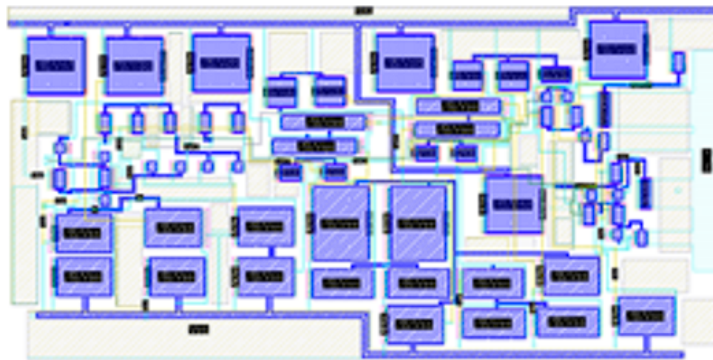


Figure 3.50: Layout of the logarithmic circuit

Fig.3.51 shows that the layout is very close to the pre-layout simulation with a slight shift.

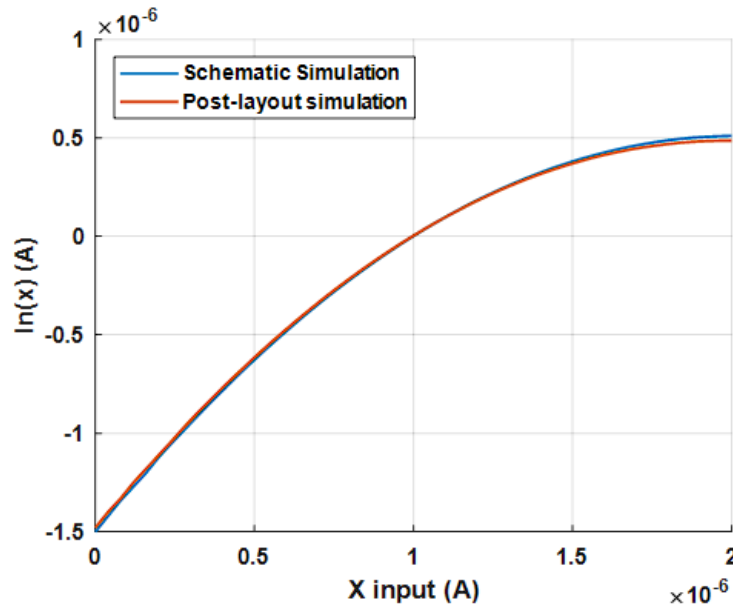


Figure 3.51: Plots of post-layout and schematic of the logarithmic function.

Similar to schematic various analysis are done to the post-layout. Temperature analysis, corner analysis, and AC analysis simulation are shown in Fig.3.52 - Fig.3.54, respectively. Fig.3.52 shows that the circuit is still almost immune to temperature. Fig.3.53 shows that the function is still the same with a very slight shift due to process. The frequency response shown in Fig.3.54 is similar to the schematic with a 3 dB cutoff frequency around 2.79 MHz. The simulations shows that the post-layout and schematic simulations are very close.

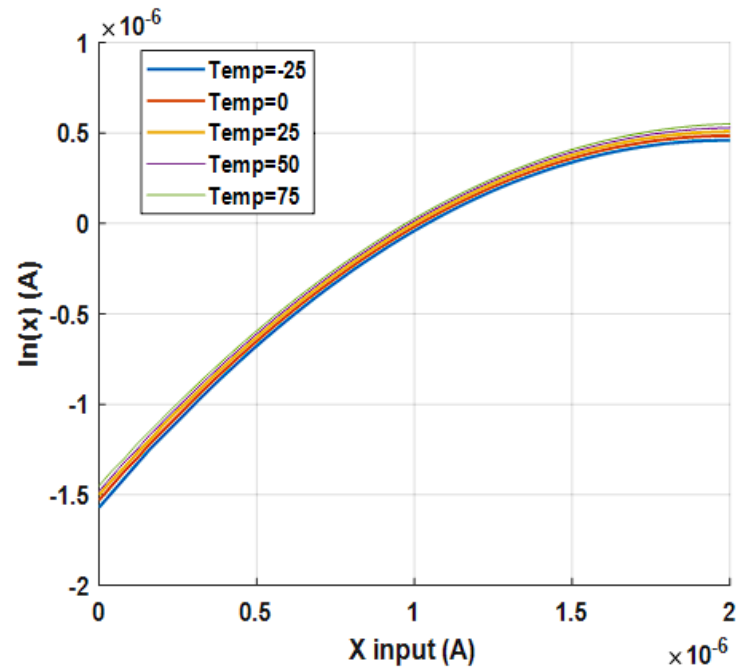


Figure 3.52: Temperature analysis of the extracted view of the logarithmic circuit

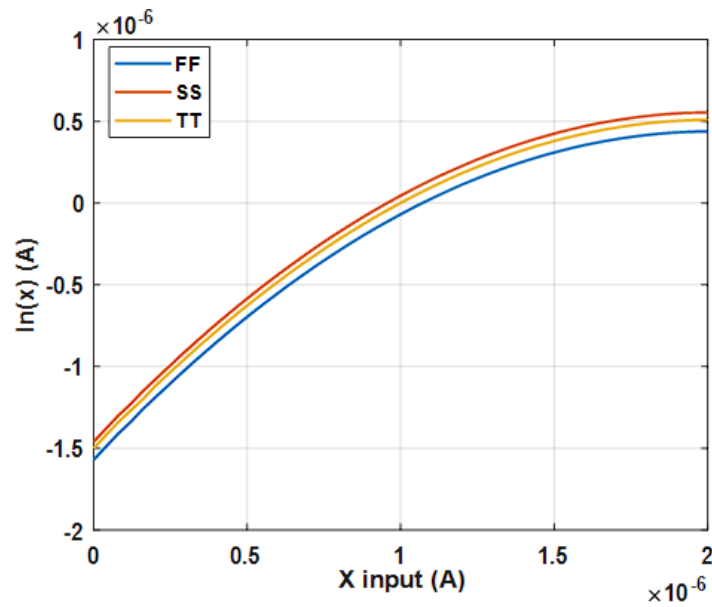


Figure 3.53: Corner analysis of the extracted view of the logarithmic circuit

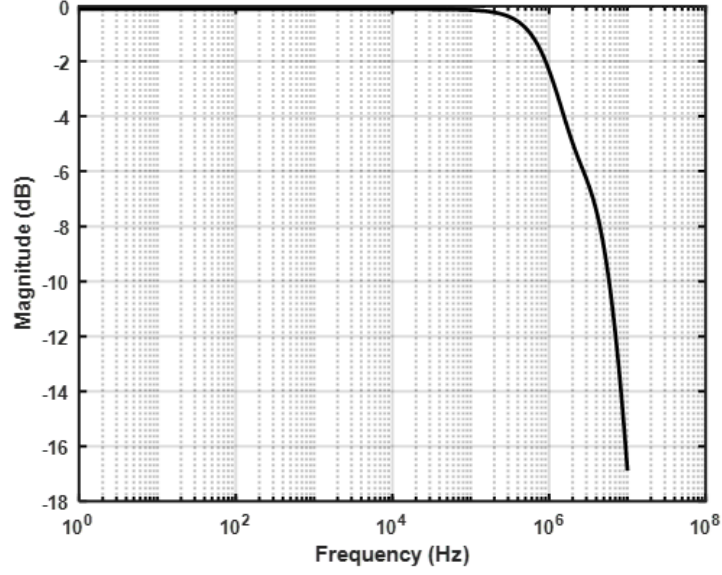


Figure 3.54: AC analysis of the extracted view of the logarithmic circuit.

Finally, to test the reliability of the post-layout of proposed logarithmic circuit approximation design, the Monte Carlo analysis is performed. The input x is taken to be in the middle of the range of the logarithmic circuit with 1000 runs of Monte Carlo analysis shown in Fig.3.55. The Monte Carlo analysis is found to be Gaussian with a mean of -164.32 nA. The standard deviation is calculated to be around $\sigma=33.04$ nA. The majority of the samples falls within to 2σ with more than 93% of the samples.

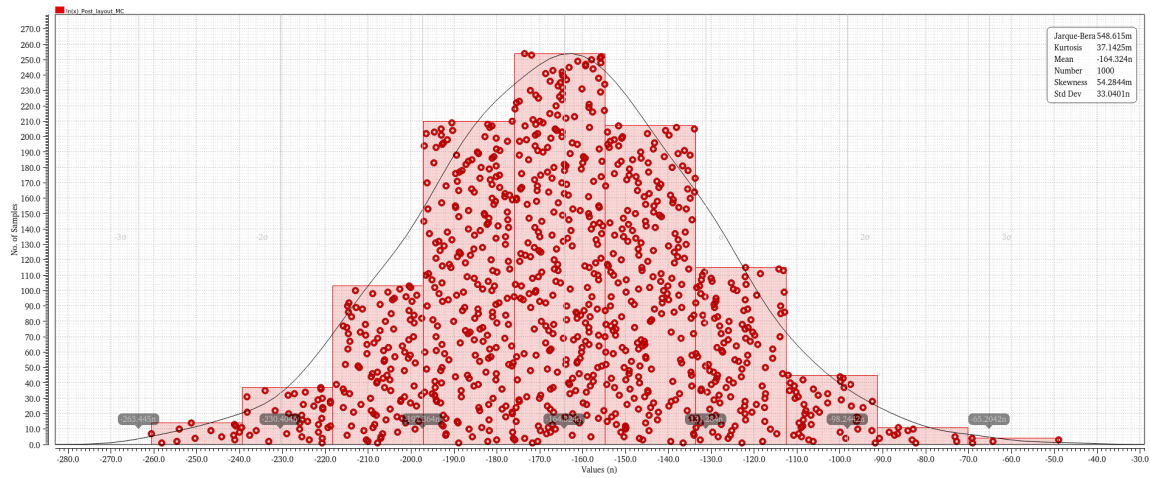


Figure 3.55: Histogram of the Monte Carlo simulation of the logarithmic function post-layout showing the number of samples at input $x= 1 \mu A$

The logarithmic circuit design was compared to earlier artwork and summarized in Table 3.5. It is evident from the table that the proposed design outperforms all other designs.

Table 3.5: Summary of logarithmic circuit comparison

Reference No.	[49]	[51]	[52]	[53]	This work
Technology (μm)	0.5	0.35	0.35	0.065	0.18
Year	2008	2009	2014	2019	2024
Supply Voltage (V)	± 2.0	3.3	± 1.65	± 0.5	± 1.25
Normalized input range	± 1	1	1	1	-1 to 2
Approximation used	$\sum_{n=0}^6 a_n x^n$	$-0.84x^2 + 4.8x - 8.4\sqrt{x} + 4.5$	$6.529\sqrt{x} - 2.51x - 3.947$	Not mentioned	$(x-1) - \frac{1}{2}(x-1)^2$
Temperature sensitive	Yes	Yes	Yes	Yes	No
Bandwidth	Not mentioned	Not mentioned	Not mentioned	Not mentioned	2.8 MHZ

3.4.3 Simulation Vs Theory

A comparison between theory and schematic is done. Plots of $\ln(x)$, approximated $\ln(x)$ and the schematic simulation are shown in Fig.3.56.

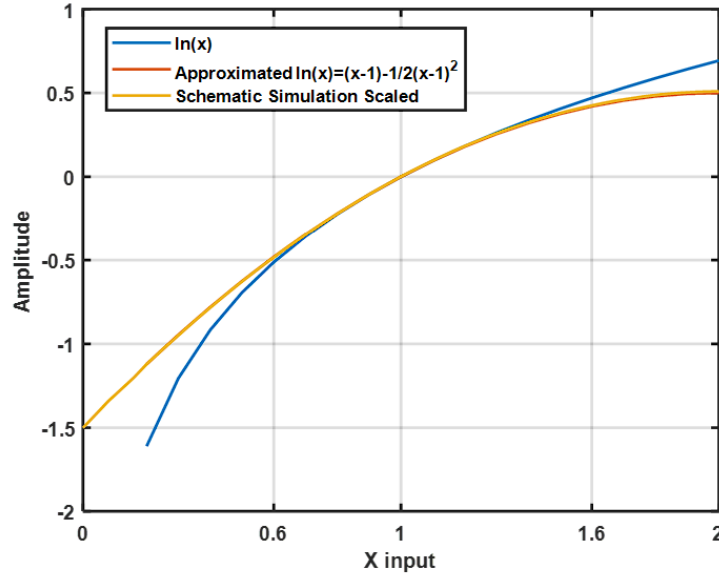


Figure 3.56: Plots of theory, approximated and schematic simulation for $\ln(x)$.

It is clear that the schematic simulation is identical to the approximation. Both simulation and approximation are close to theoretical $\ln(x)$ for values between 0.4 to 1.6. This result is expected since the approximation used (Taylor series) is valid for small values of x around the center value of the approximation ($x=1$ in this case). The logarithmic circuit can be used as $\ln(x)$ only within the values, where the Taylor series is valid.

3.5 Inverse Function

Finally, the exponential and natural log are combined to implement the inverse function. Fig.3.57 shows the block diagram of the circuit. While the Theory behind this combining is as follows in Eq(3.30):

$$Inverse(x) = e^{-ln(x)} = e^{ln(x^{-1})} = x^{-1} = \frac{1}{x} \quad (3.30)$$

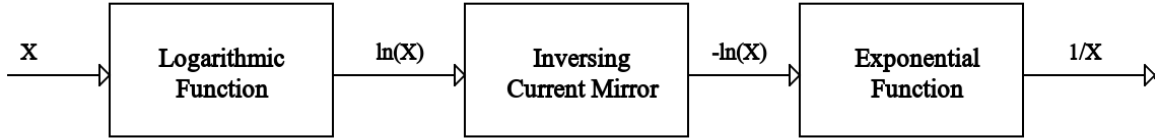


Figure 3.57: Block diagram of inverse function.

Where the first block is the proposed logarithmic function. The the logarithmic function is inverted. The third block is the proposed exponential function.

Using this approximation a realization is possible using current mirrors to correct the constant. The block diagram showing the implementation is shown in Fig.3.57. The full circuit implementation is shown in Fig.3.58 with the sizes of each transistor of logarithmic and exponential circuits used are in Tables.3.2 and 3.4, respectively.

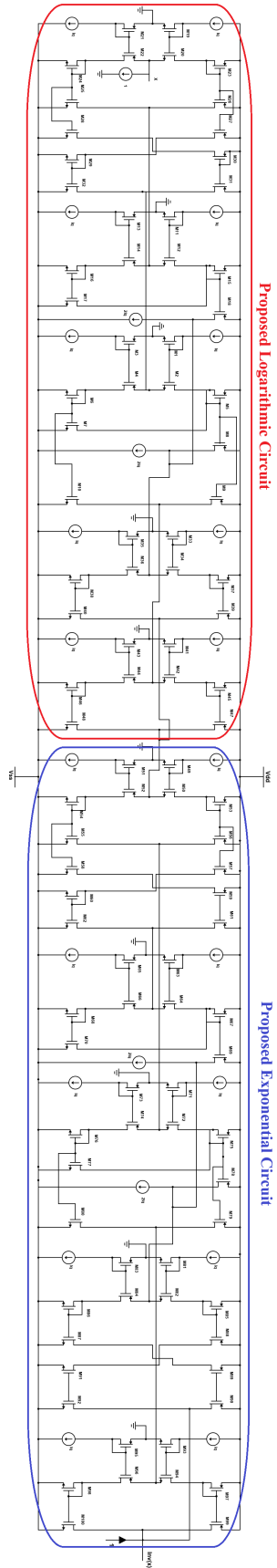


Figure 3.58: The proposed current-mode inverse function generator's circuit schematic

3.5.1 Simulation Results

The results of using the proposed basic cell are shown in Fig.3.59 and Fig.3.60. Fig.3.59 shows the values of the realization of inverse using the basic cell, while Fig.3.60 shows the value variation in the inverse due to temperature.

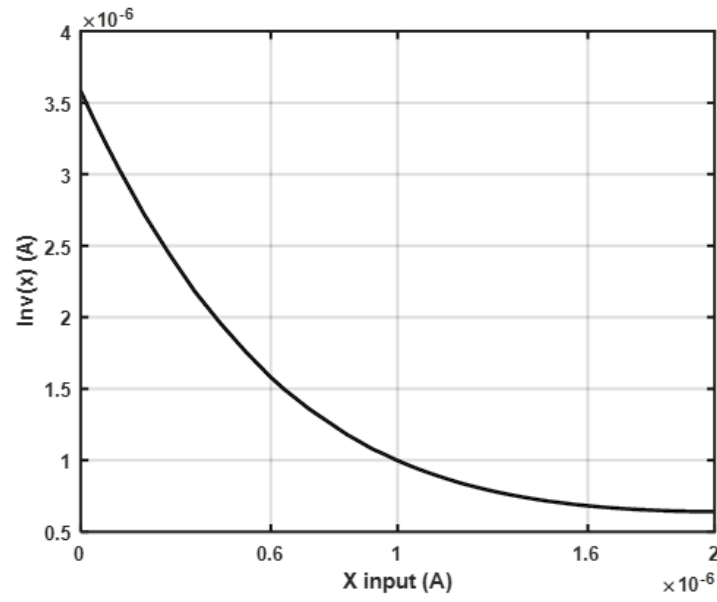


Figure 3.59: Results of realization of inverse function using proposed basic cell.

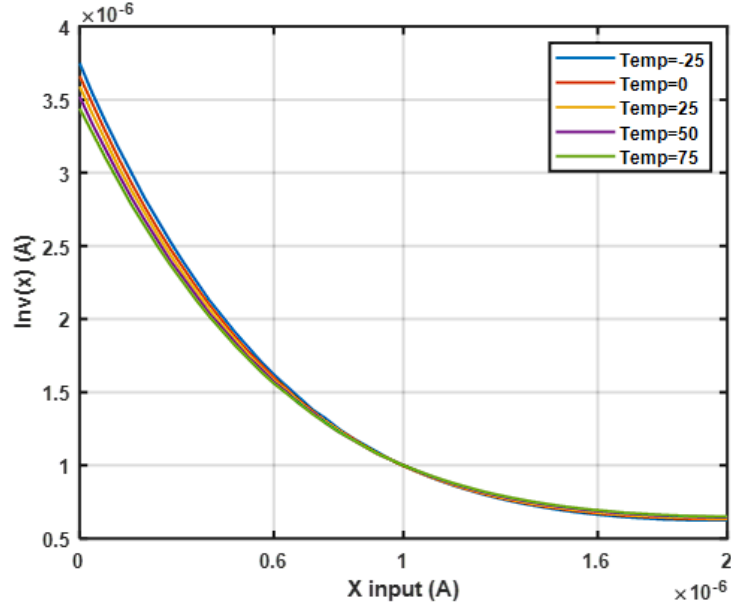


Figure 3.60: Temperature analysis of the inverse function using the proposed basic cell.

Fig.3.60 shows that the inverse circuit is almost immune to temperature variation from -25°C to 75°C . The corner analysis is done on the circuit and shown in Fig.3.61

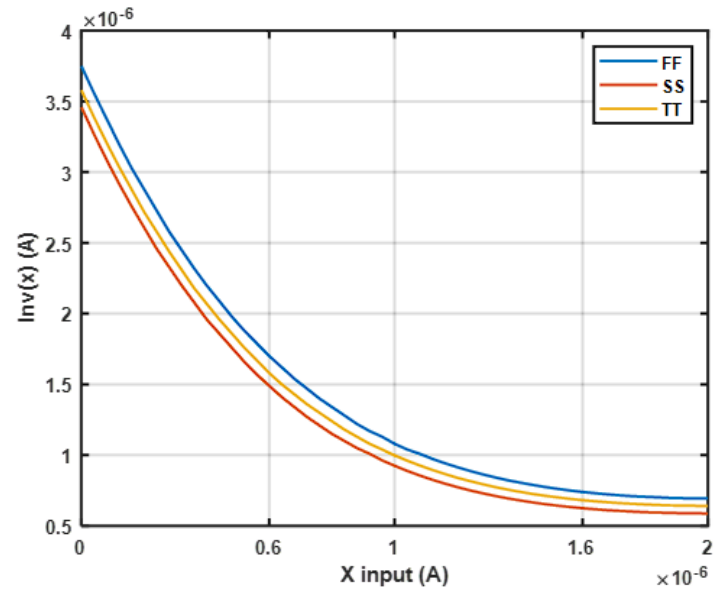


Figure 3.61: Plots for corner analysis of inverse circuit

From Fig.3.61, it is clear that the inverse circuit is behaving the same regardless of process but with a slight vertical shift.

The frequency range of the circuit is found using AC analysis simulation. Plots of the simulation is shown in Fig.3.62. The circuit 3 dB cutoff is around 1.115 MHz.

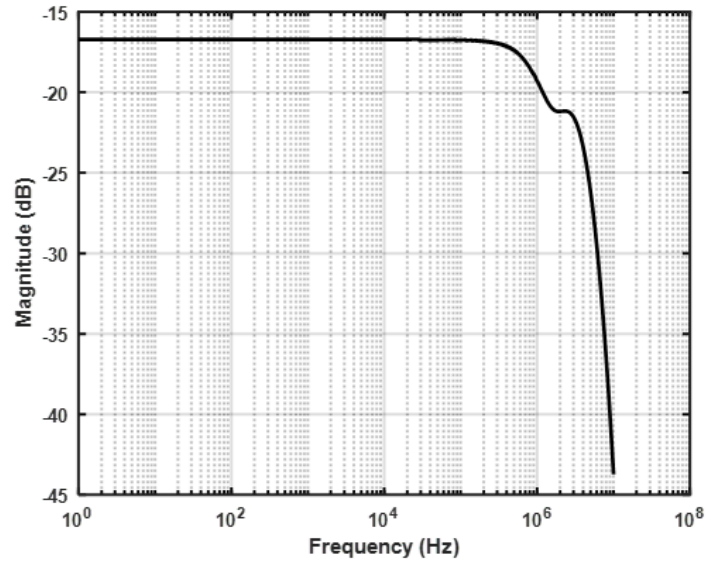


Figure 3.62: Plot of the AC analysis of the inverse circuit

Finally, to test the reliability of the proposed inverse function circuit approximation design, the Monte Carlo analysis is performed. The input x is taken to be in the middle of the range of the inverse function circuit with 1000 runs of Monte Carlo analysis shown in Fig.3.63. The Monte Carlo analysis is found to be Gaussian with a mean of $1.356 \mu\text{A}$. The standard deviation is calculated to be around $\sigma=34.58 \text{ nA}$. The majority of the samples falls within to 2σ with more than 95% of the samples.

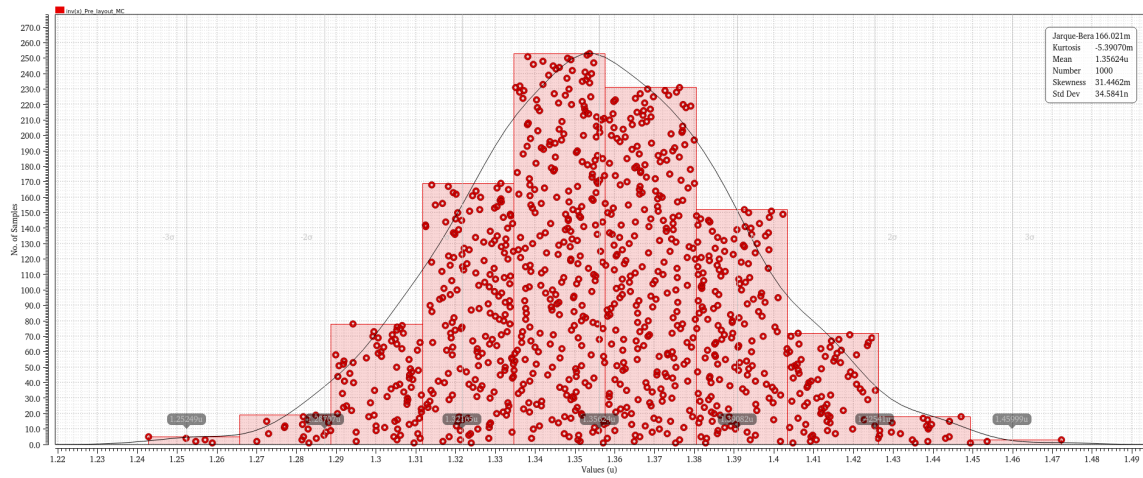


Figure 3.63: Histogram of the Monte Carlo simulation for inverse function schematic showing the number of samples at input $x = 0.9 \mu A$

3.5.2 Post-layout Simulation Results

The post-layout simulation of the inverse circuit is carried and it matches the pre-layout simulation.

The layout of the logarithmic circuit is shown in Fig.3.64. The area of the layout is around $12000 \mu m^2$.

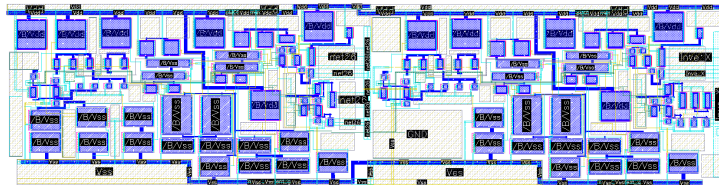


Figure 3.64: Layout of the inverse circuit

Fig.3.65 shows that the layout is very close to the pre-layout simulation with a

slight shift.

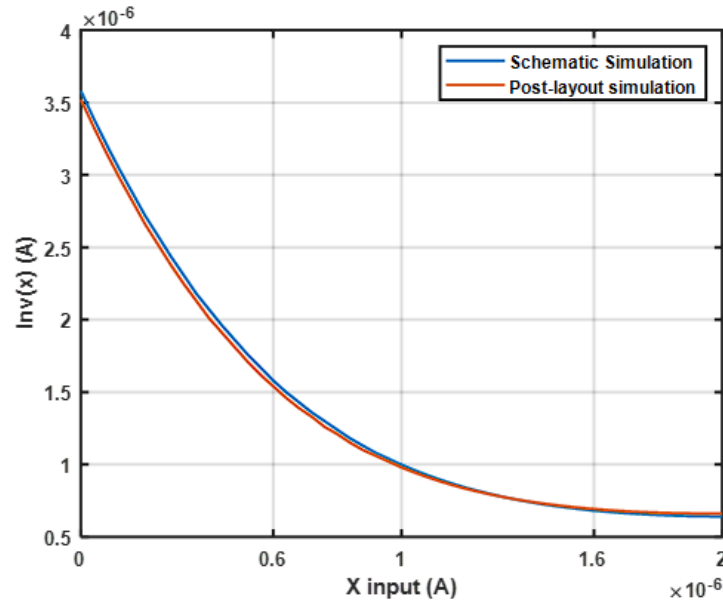


Figure 3.65: Plots of post-layout and schematic of the inverse function.

Similar to schematic various analysis are done to the post-layout. Temperature analysis, corner analysis, and AC analysis simulation are shown in Fig.3.66 - Fig.3.68, respectively. Fig.3.66 shows that the circuit is still almost immune to temperature. Fig.3.67 shows that the function is still the same with a very slight shift due to process. The frequency response shown in Fig.3.68 is similar to the schematic with a 3 dB cutoff frequency around 0.9935 MHz. The simulations shows that the post-layout and schematic simulations are very close.

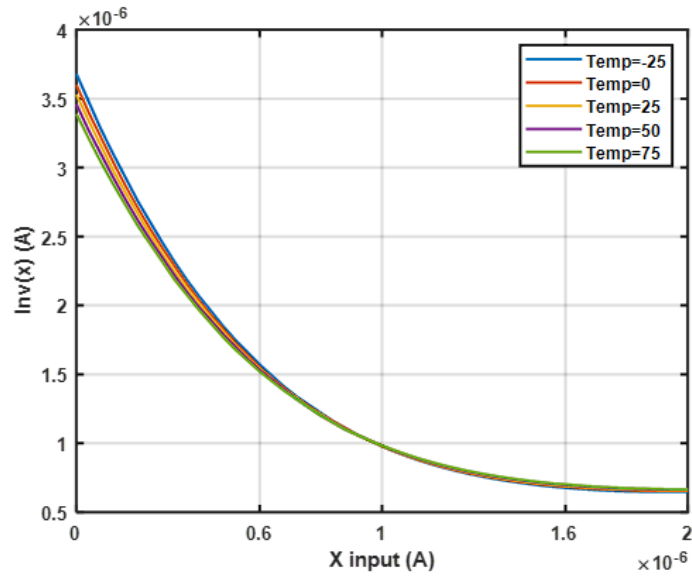


Figure 3.66: Temperature analysis of the extracted view of the inverse circuit

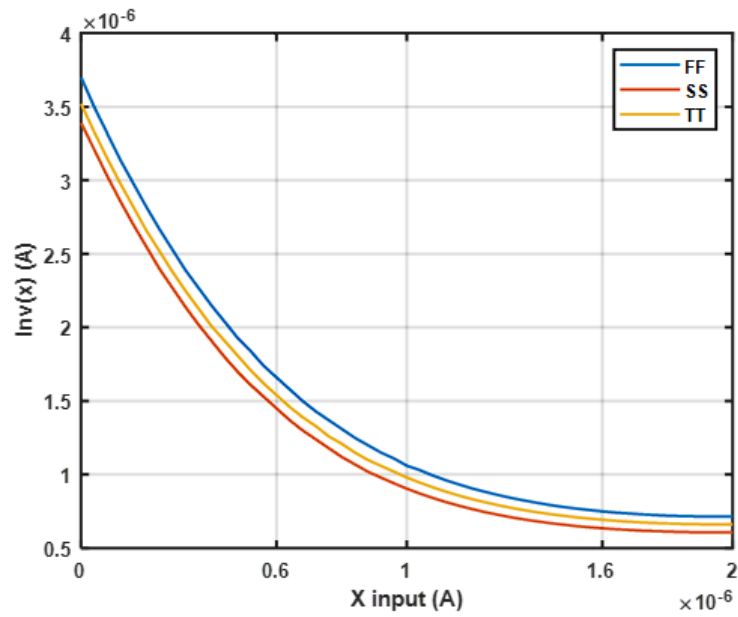


Figure 3.67: Corner analysis of the extracted view of the inverse circuit

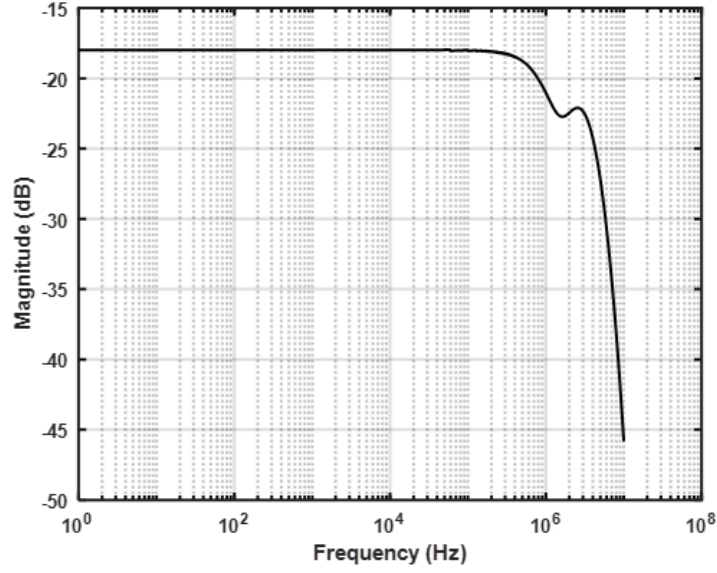


Figure 3.68: AC analysis of the extracted view of the inverse circuit.

Finally, to test the reliability of the post-layout of proposed inverse function circuit approximation design, the Monte Carlo analysis is performed. The input x is taken to be in the middle of the range of the inverse function circuit with 1000 runs of Monte Carlo analysis shown in Fig.3.69. The Monte Carlo analysis is found to be Gaussian with a mean of $1.336 \mu\text{A}$. The standard deviation is calculated to be around $\sigma=34.55$ nA. The majority of the samples falls within to 2σ with more than 95% of the samples.

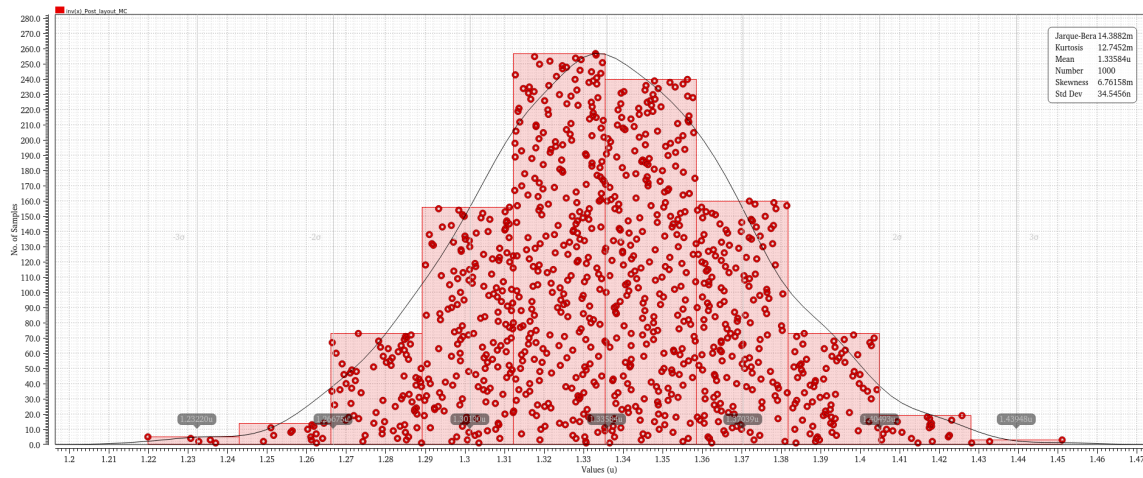


Figure 3.69: Histogram of the Monte Carlo simulation for inverse function post-layout showing the number of samples at input $x= 0.9 \mu A$

3.5.3 Simulation Vs Theory

A comparison between theory and schematic is done. Plots of $\text{inverse}(x)$, approximated $\text{inverse}(x)$ and the schematic simulation are shown in Fig.3.70.

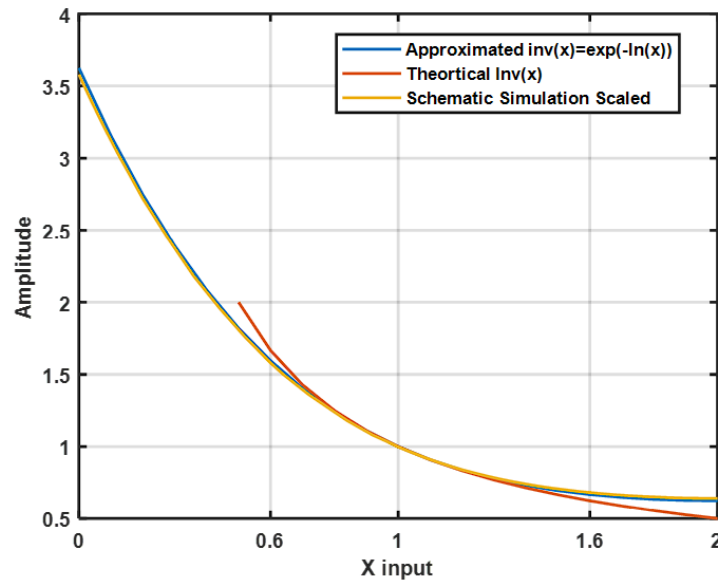


Figure 3.70: Plots of theory, approximated and schematic simulation for $\text{inv}(x)$.

It is clear that the schematic simulation is identical to the approximation. Both simulation and approximation are close to theoretical $\text{inv}(x)$ for values between 0.4 to 1.4. This result is expected since the approximation used (Taylor series for logarithmic and exponential) is valid within the ranges mentioned in the exponential and logarithmic sections. The inverse circuit can be used as $\text{inv}(x)$ only within the values, where the approximation is valid.

3.6 CTC with Inverse Function

The proposed $\text{inv}(x)$ function is used as seen in Fig.3.71 to build a CTC that is linear and PVT independent. The inverse function in conjunction with a current mirror is used to derive the current in transistor M1 in Fig.1.2.

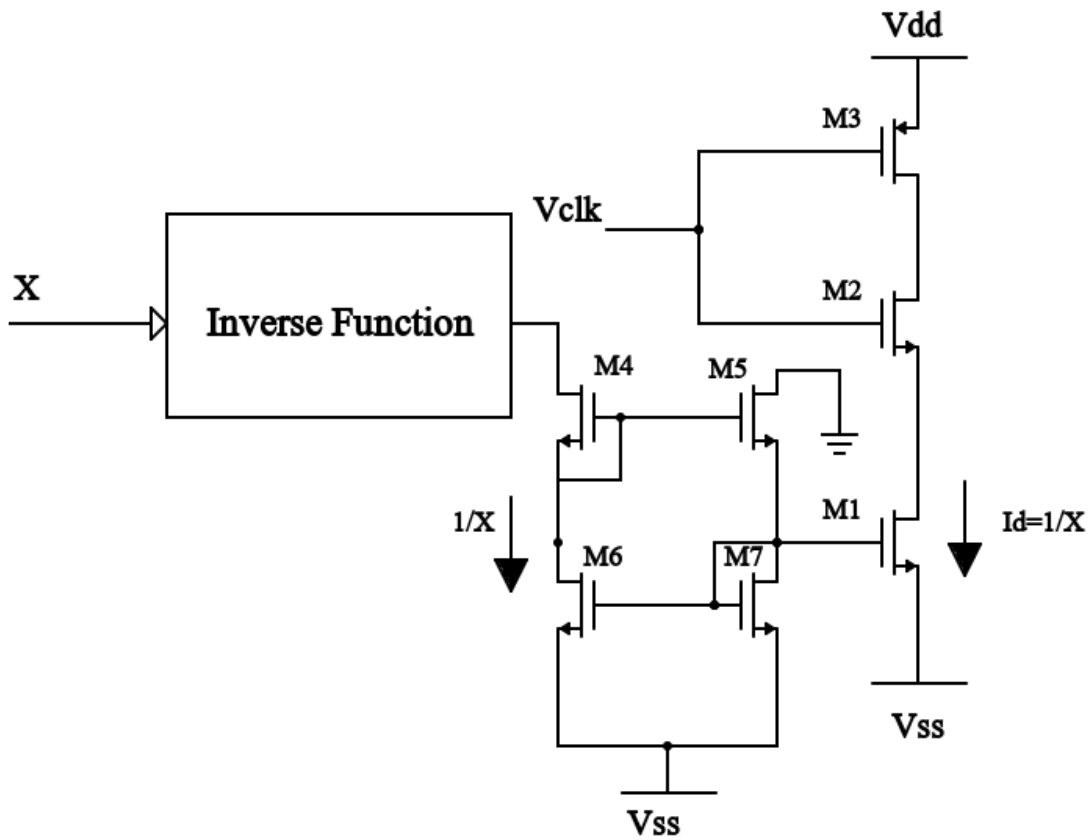


Figure 3.71: Block diagram of the current to time conveter.

This leads to the relation shown in Eq.3.31 and Eq.3.32 to be as follows:

$$inv(x) = \frac{1}{x} \quad (3.31)$$

$$dt = C \frac{dv}{inv(x)} = C \frac{dv}{\frac{1}{x}} = CXdv \quad (3.32)$$

The relation between the time delay and the input signal (current) is linear, allowing the CTC to have a linear delay conversion. The waveforms of using this method are shown in Fig.3.72, while the delay vs input x is shown in Fig.3.73

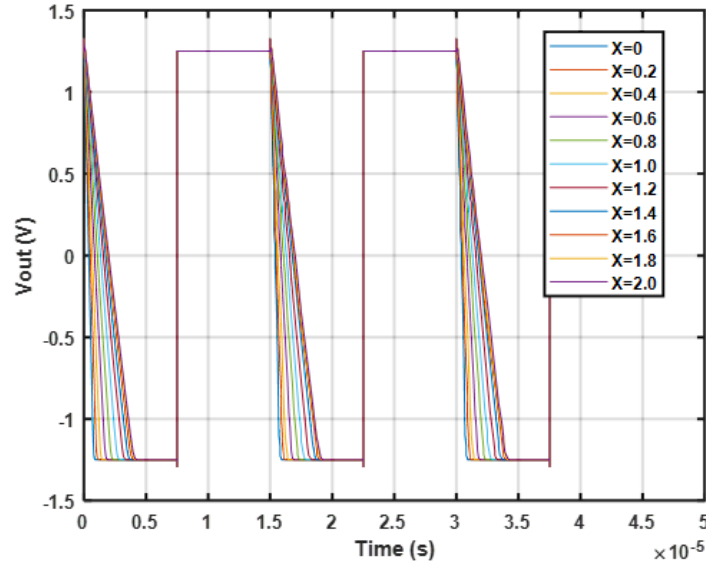


Figure 3.72: Plots of the output as a function of time for the proposed CTC .

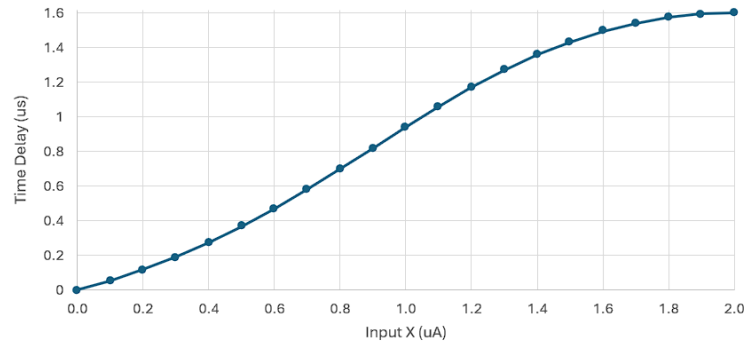


Figure 3.73: Plot of the delay as a function of the input current.

From Fig.3.73 The linear region is from $x = 0.4$ to $x = 1.4$, which is the region where the values of $\text{inv}(x)$ are correct. Fig.3.74 shows the delay within the range of X where the $\text{inv}(x)$ is valid

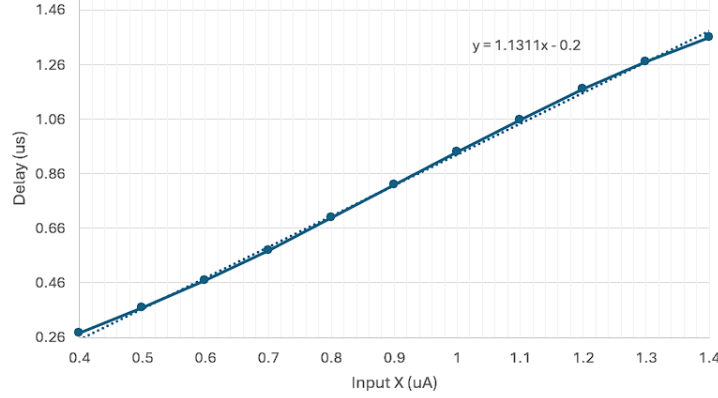


Figure 3.74: Delay of CTC using valid input for $\text{inv}(x)$.

This simulation results confirms that using $\text{inv}(x)$ produces a linear CTC with an input range of $1.0\mu\text{A}$. Furthermore, for direct sensing the range needs to start from $x = 0$ instead of $x = 0.4$ we can shift the values and use $\text{inv}(x+0.4)$ instead. This is easily achievable by using the shifting discussed in $\text{inv}(x)$ and $\ln(x)$ previously. This allows the CTC to have a $1.0\mu\text{A}$ input range that starts from 0 A . The full range of this CTC can be $1.6\mu\text{A}$ by utilizing shift and simple scaler to achieve range from $x = -0.6$ up to $x = 1.4$. The CTC achieve high linearity with a maximum linearity error of 1.8%.

The CTC temperature analysis and corner analysis are shown in Fig.3.75 and Fig.3.76., respectively. Both figures are simulated at $x = 0.4\mu\text{A}$ which will give the highest error. The error due to temperature is less than 0.5%. While the error due to

process variation is around 3%.

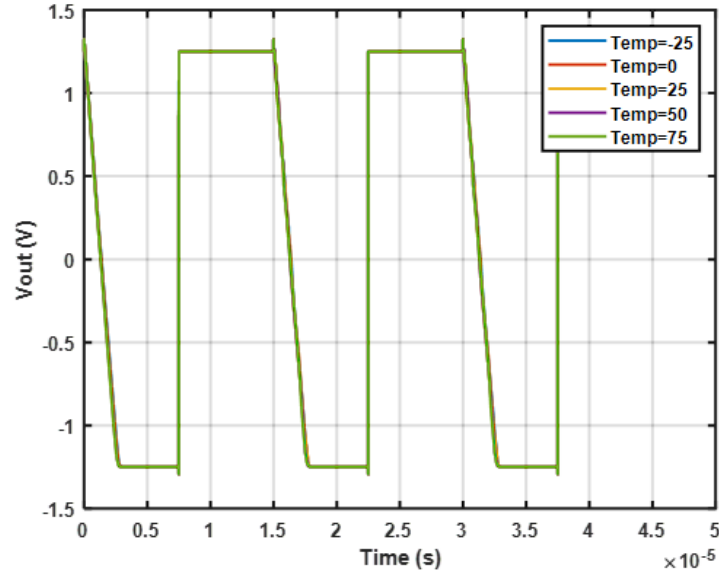


Figure 3.75: Plots of temperature analysis on the delay at $x = 0.5uA$

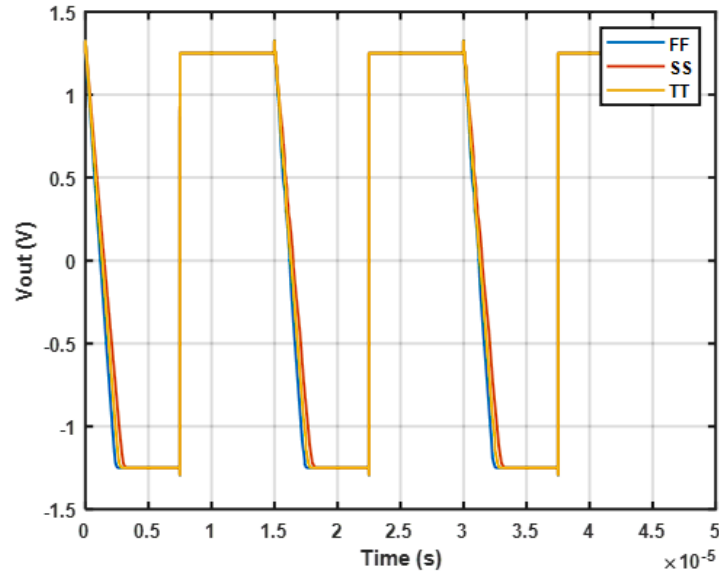


Figure 3.76: Plots of the corner analysis at $x = 0.5uA$

Finally, to test the reliability of the proposed CTC circuit design, the Monte Carlo analysis is performed. The input x is taken to be in the middle of the range of the

CTC circuit with 1000 runs of Monte Carlo analysis shown in Fig.???. The Monte Carlo analysis is found to be Gaussian with a mean of 293.87 mV . The standard deviation is calculated to be around $\sigma=10.73 \text{ mV}$. The majority of the samples falls within to 2σ with more than 90% of the samples.

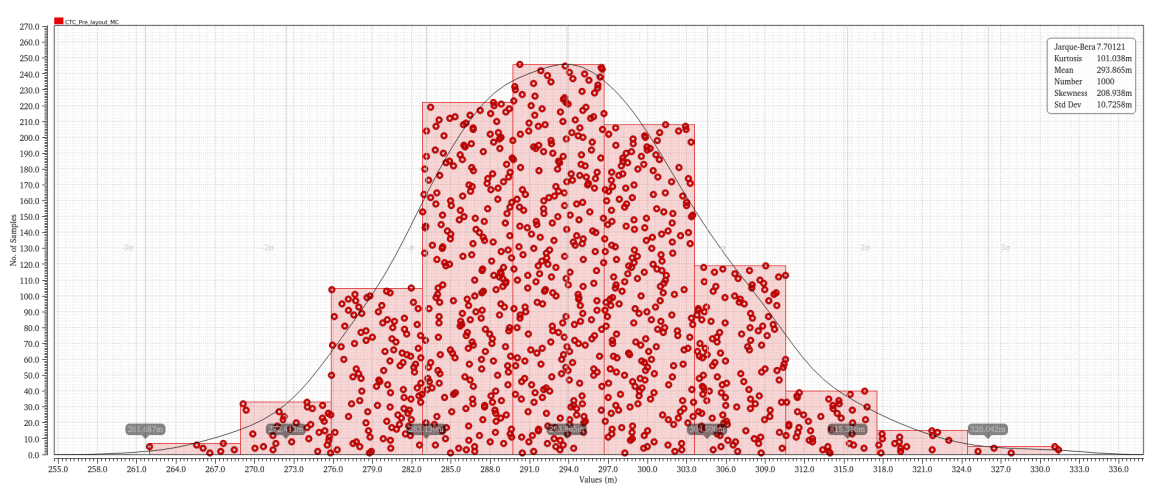


Figure 3.77: Histogram of the Monte Carlo simulation for CTC schematic showing the number of samples at input $x= 0.9 \mu\text{A}$

3.6.1 Post-layout Simulation Results

The post-layout simulation of the CTC circuit is carried and it matches the pre-layout simulation.

The layout of the CTC circuit is shown in Fig.3.78. The area of the layout is around $12000\mu\text{m}^2$.

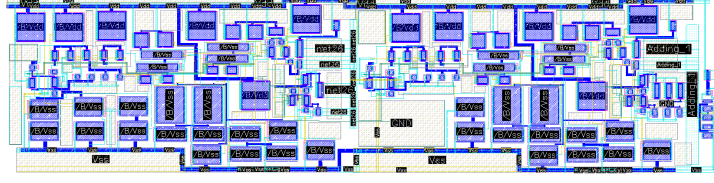


Figure 3.78: Layout of the proposed CTC.

Fig.3.79 shows that the layout is very close to the pre-layout simulation with a slight shift.

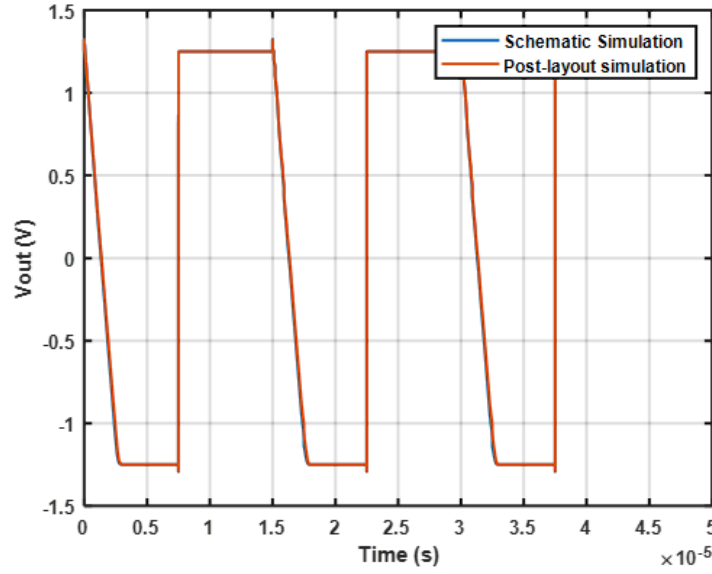


Figure 3.79: Plots of the output voltage for pre- and post-layout simulation for the CTC .

Similar to schematic various analysis are done to the post-layout. Temperature analysis and corner analysis simulation are shown in Fig.3.80 and Fig.3.81, respectively. Fig.3.80 shows that the circuit is immune to temperature. Fig.3.81 shows that

the function is still the same with a very slight shift due to process.

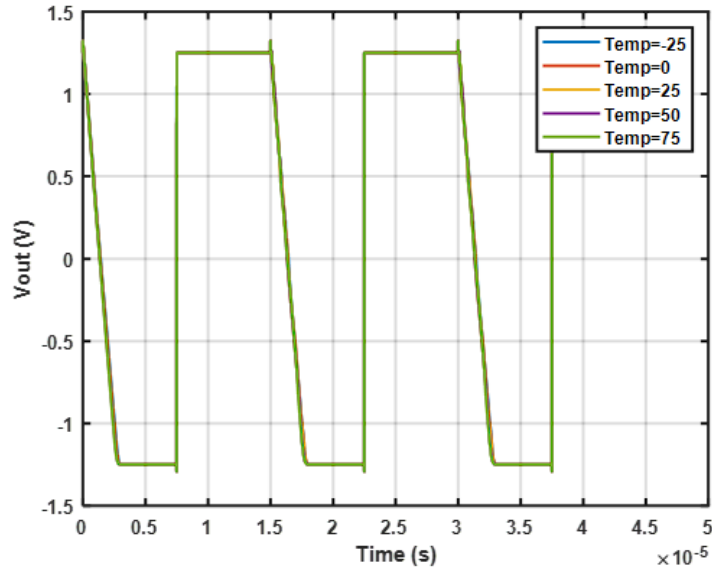


Figure 3.80: Temperature analysis of the extracted view of the CTC circuit

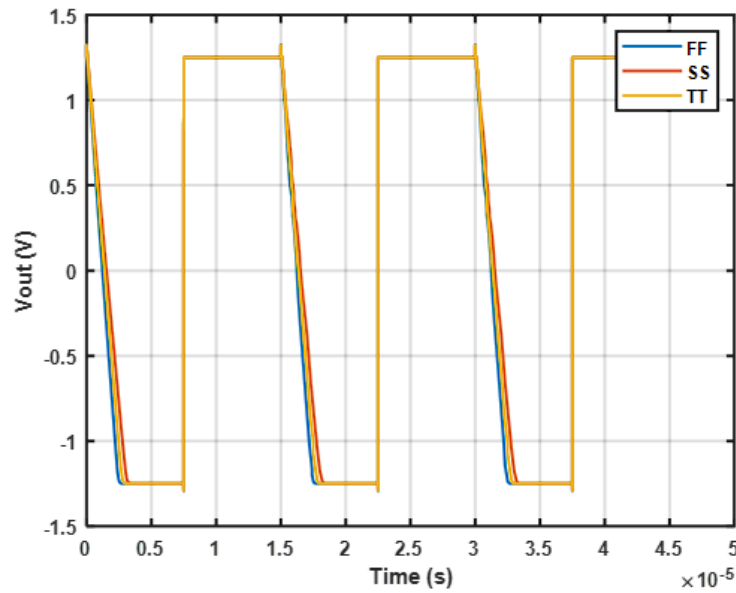


Figure 3.81: Corner analysis of the extracted view of the CTC circuit

The frequency of operation of this CTC is the same as the frequency of operation for the inv(x) of 1.115 MHz. The delay of the post-layout is almost identical to

pre-layout simulation due all of other results being identical to pre-layout simulation.

Finally, to test the reliability of the post-layout of proposed CTC circuit design, the Monte Carlo analysis is performed. The input x is taken to be in the middle of the range of the CTC circuit with 1000 runs of Monte Carlo analysis shown in Fig.3.82. The Monte Carlo analysis is found to be Gaussian with a mean of 295.82 mV . The standard deviation is calculated to be around $\sigma=10.78 mV$. The majority of the samples falls within to 2σ with more than 90% of the samples.

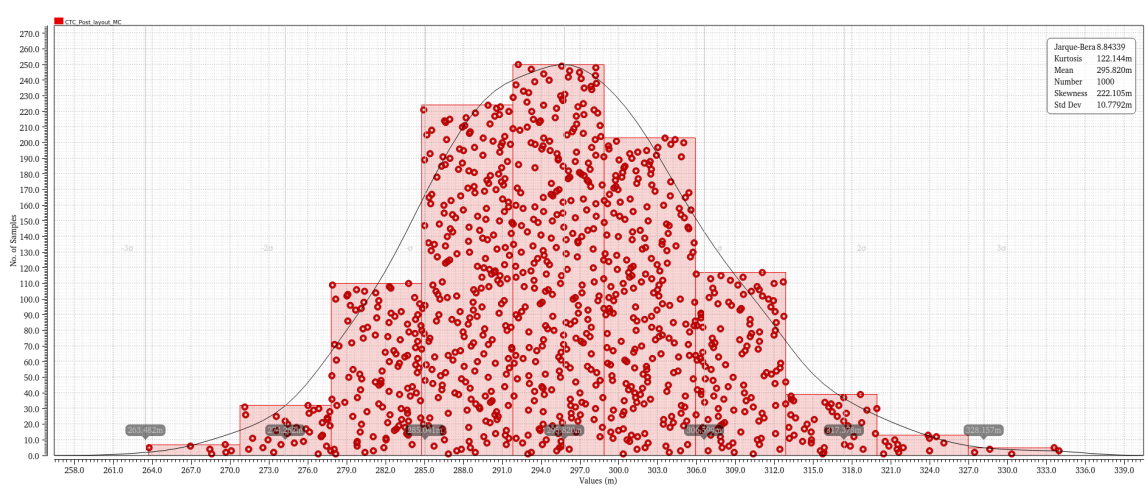


Figure 3.82: Histogram of the Monte Carlo simulation for CTC post-layout showing the number of samples at input $x= 0.9 \mu A$

Table 3.6: Comparison between different CTCs

	[22]	[23]	[24]	[25]	[26]	[27]	[30]	This Work
Year	2018	2009	2024	2020	2022	2019	2024	2024
Technology	600 nm	Not Reported	180 nm	Not Reported	65nm	350 nm	40 nm	180 nm
Supply Voltage (V)	1.0	Not Reported	1.8	1	1	3	1.1	1.25
Operation Region	Weak Inversion	Not Applicable	Weak Inversion	Strong Inversion	Subthreshold	Strong Inversion	Strong Inversion	Strong Inversion
Input Range (μA)	Not Applicable	0.7	0.03	900	0.2 V	200	Not Reported	1.6
Input Values (μA)	Not Applicable	0.3 to 1.0	0.001-0.03	100-1000	0.2 V - 0.4 V	-100 - 100	Not Reported	-0.4 - 1.4
Area (mm^2)	Not Reported	Not Reported	0.0012	Not Reported	0.038	Not Reported	Not Reported	0.012
Operating Frequency (MHz)	Not Reported	Not Reported	Not Reported	0.001	1	25	Not Reported	1.115
Passive Components	2	8 Inductors	0	0	0	1	1	0
Maximum Linearity Error	2.7%	non-linear	Not Reported	3%	non-linear	2.1%	around 0.7%	1.8%
Maximum Temperature Error	Used as temperature sensor (highly dependant)	none (operates at 1 Kelvin)	Mentiond high Error	Mentiond high Error	around 15%	Not Reported	Not Reported	0.5%
Maximum Process Variation Error	Not Reported	Not Applicable	Mentiond high Error	Not Reported	Not Reported	Not Reported	around 30%	3%
Conversion Rate (s/A)	Not Reported	0.0000000000125	1.8	0.00386	Not Reported	0.125	Not Reported	1

The proposed is design compared with previous arts and summarized in Table 3.6. It evident that the proposed CTC has the best performance in terms linearity, good input range while being insensitive to PVT variations.

CHAPTER 4

CONCLUSION

Digital signal processing is an important field. It faces the issue of acquiring the analog data provided by sensors and converting it into digital. T-ADC provides reliable, low power and fast conversion but its core block VTC or CTC suffers from linearity and PVT variations. A new developed CTC that utilizes the inverse function circuit using MOS in strong inversion. The thesis started by proposing a new implementation of inverse function circuit using proposed exponential and logarithmic functions. The proposed exponential and logarithmic function are implemented using MOS in strong inversion by utilizing Taylor series approximations. The functionality of all proposed designs were confirmed using post-layout simulation in CADENCE Virtuoso in $0.18\mu\text{m}$ TSMC CMOS process technology. The simulation results of the proposed CTC shows that the design is highly linear, compact and PVT insensitive. The CTC maximum linearity error is less than 1.8% with a full input range of $1.6\mu\text{A}$ and the frequency of operation reaches up to 1.115MHz. The developed circuit will serve as a fundamental building block in many signal processing applications.

4.1 Future Work and Recommendations

The next work can focus on increasing the frequency of operation. Even though the current work has high speed operation compared to previous work, the speed of some applications reach up to GHz range. Also, the work can focus on more efficient implementation that conserve power and area, while keeping the linearity and PVT insensitivity the same. Finally, the input range has to increase further to be used with the temperature sensors in the market that can reach output of around $10\ \mu\text{A}$.

REFERENCES

- [1] G. W. Roberts and M. Ali-Bakhshian, “A brief introduction to time-to-digital and digital-to-time converters,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 3, pp. 153–157, 2010.
- [2] S. Jia, L. Weng, W. Wang, and Y. Wang, “A highly linear 5gs/s voltage-to-time converter for time-based analog-to-digital converters,” pp. 714–717, 2017.
- [3] H. Mostafa and Y. I. Ismail, “Highly-linear voltage-to-time converter (vtc) circuit for time-based analog-to-digital converters (t-adcs),” in *2013 IEEE 20th international conference on electronics, circuits, and systems (ICECS)*. IEEE, 2013, pp. 149–152.
- [4] A. R. Macpherson, K. A. Townsend, and J. W. Haslett, “A 5gs/s voltage-to-time converter in 90nm cmos,” in *2009 European Microwave Integrated Circuits Conference (EuMIC)*, 2009, pp. 254–257.
- [5] H. Pekau, A. Yousif, and J. Haslett, “A cmos integrated linear voltage-to-pulse-delay-time converter for time based analog-to-digital converters,” in *2006 IEEE International Symposium on Circuits and Systems*, 2006, pp. 4 pp.–2376.

- [6] A. H. Hassan, H. Mostafa, T. Ismail, and S. R. I. Gabran, “An ultra-low power voltage-to-time converter (vtc) circuit for low power and low speed applications,” pp. 178–182, 2016.
- [7] A. Elgreatly, A. Dessouki, H. Mostafa, R. Abdalla, and E.-s. El-Rabaie, “A novel highly linear voltage-to-time converter (vtc) circuit for time-based analog-to-digital converters (adc) using body biasing,” *Electronics*, vol. 9, no. 12, 2020. [Online]. Available: <https://www.mdpi.com/2079-9292/9/12/2033>
- [8] C. Puglisi, E. Ghaderi, S. Bansal, G. Larue, and S. Gupta, “A 2vpk-pk,diff input range 1gs/s voltage-to-time converter with tunable distortion compensation,” in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–4.
- [9] Q. Chen, C. C. Boon, and Y. Liang, “A 0.6 v 4 gs/s -56.4 db thd voltage-to-time converter in 28 nm cmos,” *IEEE Access*, vol. 10, pp. 88 558–88 566, 2022.
- [10] Y. Zhao, F. Ye, and J. Ren, “A 500-ms/s 9-bit time-domain adc using a nonbinary successive approximation tdc,” in *2022 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2022, pp. 209–212.
- [11] L. Cuskelly, D. Bhaskar, and L. Belostotski, “A high-linearity 10-ghz-erbw 3-to-7-gs/s voltage-to-time converter with built-in s/h,” in *2023 IEEE 23rd Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2023, pp. 62–65.

- [12] O. Aiello, P. Crovetto, and M. Alioto, “Fully synthesizable low-area analogue-to-digital converters with minimal design effort based on the dyadic digital pulse modulation,” *IEEE Access*, vol. 8, pp. 70 890–70 899, 2020.
- [13] Y. Tu, R. Xu, D. Ye, L. Lyu, and C.-J. R. Shi, “A 400 mhz, 8-bit, 1.75-ps resolution pipelined-two-step time-to-digital converter with dynamic time amplification,” pp. 1–4, 2020.
- [14] I.-M. Yi, N. Miura, and H. Nosaka, “A 4-gs/s 11.3-mw 7-bit time-based adc with folding voltage-to-time converter and pipelined tdc in 65-nm cmos,” *IEEE Journal of Solid-State Circuits*, vol. 56, no. 2, pp. 465–475, 2021.
- [15] A. Karimlou and M. Yavari, “A time-based analogue-to-digital converter for ecg applications,” pp. 154–158, 2021.
- [16] Z. Chen, X. Zhang, Y. Ma, X. Liang, X. Du, and P. Wan, “A 1.9-ps $8\times$ phase interpolation tdc for time-based analog-to-digital converter with capacitance compensation self-calibration,” *IEICE Electronics Express*, vol. 20, no. 3, pp. 20 220 515–20 220 515, 2023.
- [17] Q. Chen, C. C. Boon, Q. Liu, and Y. Liang, “A single-channel voltage-scalable 8-gs/s 8-b >37.5 -db snr time-domain adc with asynchronous pipeline successive approximation in 28-nm cmos,” *IEEE Journal of Solid-State Circuits*, vol. 58, no. 6, pp. 1610–1622, 2023.
- [18] D. Ogata, R. Kamiya, Y. Toyoshima, and K. Ohhata, “A high-time-resolution time-to-digital converter using coupled ring oscillator with phase averaging,” in

- 2022 *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2022, pp. 195–198.
- [19] J. Wei, C. Zhang, and M. Liu, “A 11-bit 1-gs/s 14.9mw hybrid voltage-time pipelined adc with gain error calibration,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 799–803, 2022.
- [20] K.-J. Moon, D.-R. Oh, M. Choi, and S.-T. Ryu, “A 28-nm cmos 12-bit 250-ms/s voltage-current-time domain 3-stage pipelined adc,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 2843–2847, 2020.
- [21] D. Damljanovic, “A simple current-to-time converter,” *IEEE Transactions on Instrumentation and Measurement*, vol. IM-34, no. 1, pp. 87–88, 1985.
- [22] A. Setiabudi, H. Tamura, and K. Tanno, “Cmos temperature sensor with programmable temperature range for biomedical applications,” *Int. J. Electr. Comput. Eng*, vol. 8, no. 2, pp. 946–953, 2018.
- [23] S. Nakamura, H. Numabe, A. Bozbey, and A. Fujimaki, “Current resolution of a single-flux-quantum readout circuit based on current-to-time conversion toward a flux qubit system,” *IEEE transactions on applied superconductivity*, vol. 19, no. 3, pp. 973–976, 2009.
- [24] M. Al-Absi, A. Al-Khulaifi, and Y. Mahnashi, “A new highly linear current-to-time converter for direct sensing applications,” *Arabian Journal for Science and Engineering*, pp. 1–7, 2024.

- [25] N. Yadav, Y. Kim, M. Alashi, and K. K. Choi, “Sensitive, linear, robust current-to-time converter circuit for vehicle automation application,” *Electronics*, vol. 9, no. 3, p. 490, 2020.
- [26] M. Islam and S. Harada, “On-chip leakage current variation measurement using external-reference-free current-to-time conversion for densely placed mosfets,” *Japanese Journal of Applied Physics*, vol. 61, no. SC, p. SC1056, 2022.
- [27] S. Vlassis, O. Felouris-Panetas, G. Souliotis, and F. Plessas, “Linear current-to-time converter,” in *2019 14th International Conference on Design Technology of Integrated Systems In Nanoscale Era (DTIS)*, 2019, pp. 1–5.
- [28] A. Roldán, C. Reig, J. Roldán, A. Cano-Abellán, S. Cardoso, and P. P. Freitas, “Quasi-static magnetoresistive sensor modeling for current-time conversion circuit applications,” in *Proceedings of the 8th Spanish Conference on Electron Devices, CDE’2011*, 2011, pp. 1–4.
- [29] M. Ahmed and T. Musah, “Time-based optical receiver featuring a linear current-to-time conversion with equalization,” in *2023 IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2023, pp. 713–717.
- [30] B.-K. An, X. Zhang, A. T. Do, and T. Tae-Hyong Kim, “Time-based sensing with linear current-to-time conversion for multi-level resistive memory,” in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024, pp. 1–5.
- [31] A. Oki, M. Kim, G. Gorman, and J. Camou, “High-performance gaas heterojunction bipolar transistor logarithmic if amplifier,” in *IEEE 1988 Microwave*

- and *Millimeter-Wave Monolithic Circuits Symposium. Digest of Papers.*, 1988, pp. 41–45.
- [32] R. Wolffenbuttel, “Digitally programmable accurate current sources for logarithmic control of the amplification or attenuation in a gain cell,” *IEEE Journal of Solid-State Circuits*, vol. 23, no. 3, pp. 767–773, 1988.
- [33] P. Chadwick, “Advances in logarithmic amplifiers,” in *1989 Fifth International Conference on Radio Receivers and Associated Systems*, 1990, pp. 51–58.
- [34] K. Kimura, “Circuit design techniques for very low-voltage analog functional blocks using triple-tail cells,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, no. 11, pp. 873–885, 1995.
- [35] —, “Some circuit design techniques for low-voltage analog functional elements using squaring circuits,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 43, no. 7, pp. 559–576, 1996.
- [36] F. Bergouignan, N. Ahouchi, R. Grisel, G. Caille, and J. Caranana, “Designs of a logarithmic and exponential amplifiers using current conveyors,” in *Proceedings of Third International Conference on Electronics, Circuits, and Systems*, vol. 1, 1996, pp. 61–64 vol.1.
- [37] M. T. Abuelmaatti and O. O. Faris, “A current-mode logarithmic function circuit,” *Active and passive electronic components*, vol. 27, no. 3, pp. 183–187, 2004.

- [38] E. Gertel, D. Johnson, and M. Kumar, “2-18 ghz logarithmic amplification componentry,” in *IEEE International Digest on Microwave Symposium*, 1990, pp. 1093–1096 vol.3.
- [39] K. Koli and K. Halonen, “Temperature compensated logarithmic peak detector,” *Analog Integrated Circuits and signal processing*, vol. 9, pp. 131–140, 1996.
- [40] —, “A 2.5 v temperature compensated cmos logarithmic amplifier,” in *Proceedings of CICC 97 - Custom Integrated Circuits Conference*, 1997, pp. 79–82.
- [41] Y. Acharya and P. Vyavahare, “A low-current logarithmic led electrometer,” *IEEE Transactions on Instrumentation and Measurement*, vol. 49, no. 1, pp. 5–9, 2000.
- [42] B. Wilson and M. Al-Gahtani, “Improved logarithmic converter based on a transconductance feedback amplifier,” in *ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)*, vol. 1, 2001, pp. 651–654 vol. 1.
- [43] M. Hayes, “A nonlinear optical preamplifier for sensing applications,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 49, no. 1, pp. 1–9, 2002.
- [44] M. Smith, “A 0.5 to 4 ghz true logarithmic amplifier utilizing monolithic gaas mesfet technology,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 12, pp. 1986–1990, 1988.

- [45] G. Acciari, F. Giannini, and E. Limiti, "Theory and performance of parabolic true logarithmic amplifier," *IEE Proceedings-Circuits, Devices and Systems*, vol. 144, no. 4, pp. 223–228, 1997.
- [46] K. Kimura, "A cmos logarithmic if amplifier with unbalanced source-coupled pairs," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 1, pp. 78–83, 1993.
- [47] M. Abuelma'Atti and M. Alabsi, "A cmos analog cell and its applications in analog signal processing," *International journal of electronics*, vol. 93, no. 04, pp. 251–267, 2006.
- [48] M. A. AL-Absi and K. M. Altamimi, "A current-mode controllable logarithmic function circuit using mosfet in subthreshold," *Complexity*, vol. 6, p. 7, 2012.
- [49] M. A. ABSI and K. A. TAMIMI, "A new cmos logarithmic current generator," *Turkish Journal of Electrical Engineering and Computer Sciences*, vol. 24, no. 5, pp. 4517–4524, 2016.
- [50] M. T. Abuelma'atti and N. M. Al-Yahia, "An improved universal cmos current-mode analogue function synthesiser," *International journal of electronics*, vol. 95, no. 11, pp. 1127–1148, 2008.
- [51] A. Naderi, H. Mojarrad, H. Ghasemzadeh, A. Khoei, and K. Hadidi, "Circuit implementation of programmable high-resolution rational-powered membership functions in standard cmos technology," in *IEEE EUROCON 2009*, 2009, pp. 1236–1241.

- [52] M. T. Abuelma'atti and N. A. Tassaduq, "A new implementation for the logarithmic/exponential function generator," in *2014 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, 2014, pp. 127–132.
- [53] H. A. Yildiz, L. Kouhalvandi, and S. Ozoguz, "Cmos current-mode exponential/logarithmic function generator based on translinear loop configuration," in *2019 42nd International Conference on Telecommunications and Signal Processing (TSP)*, 2019, pp. 535–538.
- [54] F. Carrara and G. Palmisano, "High-dynamic-range vga with temperature compensation and linear-in-db gain control," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 2019 – 2024, 11 2005.
- [55] A. Motamed, C. Hwang, and M. Ismail, "A low-voltage low-power wide-range cmos variable gain amplifier," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 7, pp. 800–811, 1998.
- [56] T. Arthansiri and V. Kasemsuwan, "Current-mode pseudo-exponential-control variable-gain amplifier using fourth-order taylor's series approximation," *Electronics Letters*, vol. 42, no. 7, pp. 1–2, Mar 30 2006. [Online]. Available: <https://www.proquest.com/scholarly-journals/current-mode-pseudo-exponential-control-variable/docview/1625015090/se-2>
- [57] C. R. Popa, "Low-voltage improved accuracy cmos vga circuit," in *2022 6th European Conference on Electrical Engineering Computer Science (ELECS)*,

2022, pp. 79–82.

- [58] W. Liu and S.-K. Wei, “Cmos exponential-control variable gain amplifiers,” *IEE Proceedings-Circuits, Devices and Systems*, vol. 151, no. 2, pp. 83–86, 2004.
- [59] S. Ray and M. M. Hella, “A 10 gb/s inductorless agc amplifier with 40 db linear variable gain control in 0.13 m cmos,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 440–456, 2016.
- [60] C. Lin, Q. Zeng, and D. Shang, “An exponential function accelerator with radix-16 algorithm for spiking neural networks,” *IEICE Electronics Express*, vol. 20, no. 8, pp. 20 220 393–20 220 393, 2023.
- [61] J. Li, X. Liu, P. Wan, and Z. Chen, “Design of an exponential current generator for neural stimulation,” in *2021 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA)*, 2021, pp. 137–138.
- [62] M. Kaboli, B. Ghanavati, and M. Akhlaghi, “A new cmos pseudo approximation exponential function generator by modified particle swarm optimization algorithm,” *Integration*, vol. 56, pp. 70–76, 2017.
- [63] C.-C. Chang and S.-I. Liu, “Current-mode pseudo-exponential circuit with tunable input range,” *Electronics Letters*, vol. 36, no. 16, p. 1, 2000.
- [64] A. N. Saatlo and S. Ozoguz, “A new cmos exponential circuit with extended linear output range,” in *2011 20th European Conference on Circuit Theory and Design (ECCTD)*, 2011, pp. 893–896.

- [65] C. R. Popa, “Low-voltage cmos current-mode exponential circuit with 70 db output dynamic range,” *Microelectronics Journal*, vol. 44, no. 12, pp. 1348–1357, 2013.
- [66] K. M. Al-Tamimi and M. A. Al-Absi, “A 6.13 μ w and 96 db cmos exponential generator,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 11, pp. 2443–2447, 2014.
- [67] C.-J. Cheng, K.-J. Lin, and J.-E. Chen, “Design of a range-segmented cmos current-mode exponential circuit,” *Turkish Journal Of Electrical Engineering and Computer Sciences*, vol. 27, no. 4, pp. 2475–2487, 2019.
- [68] Q.-H. Duong, H.-N. Duong, T.-K. Nguyen, and S.-G. Lee, “All cmos current-mode exponential function generator,” in *The 6th International Conference on Advanced Communication Technology, 2004.*, vol. 1, 2004, pp. 528–531.
- [69] O. Ginstrup, “An exponential current generator,” *IEEE Transactions on Instrumentation and Measurement*, vol. 22, no. 3, pp. 222–225, 1973.
- [70] M. T. Abuelma’atti and N. M. Al-Yahia, “An improved universal cmos current-mode analog function synthesizer: Performance analysis,” in *APCCAS 2008 - 2008 IEEE Asia Pacific Conference on Circuits and Systems*, 2008, pp. 1196–1199.
- [71] R.-M. Weng and X.-R. Hsu, “Low-power exponential v-i converter using composite pmos transistors,” in *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, 2006, pp. 1473–1475.

- [72] M. Abuelma'Atti and M. Alabsi, "A cmos analog cell and its applications in analog signal processing," *International journal of electronics*, vol. 93, no. 04, pp. 251–267, 2006.
- [73] M. A. ABSI and K. A. TAMIMI, "A new cmos logarithmic current generator," *Turkish Journal of Electrical Engineering and Computer Sciences*, vol. 24, no. 5, pp. 4517–4524, 2016.
- [74] B. Ghanavati, E. Abiri, and M. Salehi, "A high-accurate exponential function generator based on a new pseudo-approximation method by tlbo optimization algorithm," *Circuits, Systems, and Signal Processing*, vol. 37, 04 2018.
- [75] P. Srivastava and R. K. Sharma, "Erratum to: A novel exponential approximation with ± 0.21 dB error for realizing an improved cmos exponential function generator," *Circuits, Systems, and Signal Processing*, vol. 36, 02 2017.
- [76] —, "A novel pseudo-taylor-exponential approximation technique for input–output range extension with reduced linearity error and its current-mode cmos implementation," *ARABIAN JOURNAL FOR SCIENCE AND ENGINEERING*, vol. 46, 04 2021.
- [77] V. Kalenteridis, S. Vlassis, and S. Siskos, "1.5-v cmos exponential current generator," *Analog Integrated Circuits and Signal Processing*, vol. 72, pp. 333–341, 08 2012.

- [78] M. T. Abuelma'atti and N. A. Tassaduq, "A new implementation for the logarithmic/exponential function generator," *Analog Integrated Circuits and Signal Processing*, vol. 83, pp. 75–84, 2015.
- [79] M.-L. Lin, A. T. Erdogan, T. Arslan, and A. Stoica, "A novel cmos exponential approximation circuit," in *2008 IEEE International SOC Conference*, 2008, pp. 301–304.
- [80] A. Naderi, A. Khoei, and K. Hadidi, "Circuit implementation of high-resolution rational-powered membership functions in standard cmos technology," *Analog Integrated Circuits and Signal Processing*, vol. 65, pp. 217–223, 11 2010.
- [81] H. A. Yildiz, L. Kouhalvandi, and S. Ozoguz, "Cmos current-mode exponential/logarithmic function generator based on translinear loop configuration," in *2019 42nd International Conference on Telecommunications and Signal Processing (TSP)*, 2019, pp. 535–538.
- [82] P. Srivastava and R. Sharma, "A novel pseudo-taylor-exponential approximation technique for input–output range extension with reduced linearity error and its current-mode cmos implementation," *Arabian Journal for Science and Engineering*, vol. 46, no. 10, pp. 9809–9830, 2021.
- [83] K. M. Al-Tamimi, M. A. Al-Absi, and M. T. Abuelma'atti, "Temperature insensitive current-mode cmos exponential function generator and its application in variable gain amplifier," *Microelectronics Journal*, vol. 45, no. 3, pp. 345–354, 2014.

- [84] M. A. Al-Absi and I. A. As-Sabban, “A new highly accurate cmos current-mode four-quadrant multiplier,” *Arabian Journal for Science and Engineering*, vol. 40, pp. 551–558, 2015.
- [85] E. Seevinck and R. Wiegink, “Generalized translinear circuit principle,” *IEEE Journal of Solid-State Circuits*, vol. 26, no. 8, pp. 1098–1102, 1991.
- [86] D. Neaman, *Semiconductor Physics and Devices*, Irwin, 2021.

VITAE

- Name: Mazen Mohamed Aboubakreleddik Abouelezz
- Nationality: Egyptian
- Date of Birth: 15/03/1997
- Email: AbouelezzMazen@gmail.com
- Permanent Address: 27th building, Abou bakr el-sedeek street, El Mansoura, Dakahlia, 7661247, Egypt
- Academic Background: Master of Science in Electrical Engineering, King Fahd University of Petroleum and Minerals. Bachelors of science in Electrical Engineering, King Fahd University of Petroleum and Minerals.
- Papers Publication:

Mazen Abouelezz and Muneer AL Absi, “Realization of PVT Independent Current-Mode CMOS Exponential Circuit”, IEEE ICM2024, Accepted.

Mazen Abouelezz and Muneer AL Absi, “Realization of PVT Independent Current-Mode CMOS Exponential Circuit”, IJCTA, Accepted.

Mazen Abouelezz and Muneer AL Absi, “Realization of PVT Independent Current-Mode CMOS Logarithmic Circuit”, AJSE, Under Review.

Mazen Abouelezz and Muneer AL Absi, “Realization of a Current-mode and PVT Independent Inverse Circuit”, to be submitted.

Mazen Abouelezz and Muneer AL Absi, “Realization of PVT Independent Current to Time Converter”, to be submitted.

- Filed Patents:

Mazen Abouelezz and Muneer AL Absi, “Realization of Current-Mode and PVT Independent CMOS Logarithmic Circuit ”, KFUPM Reference #: 2024-301, Filed.

Mazen Abouelezz and Muneer AL Absi, “Realization Of Exponential Circuit Using CMOS In Strong Inversion”, KFUPM Reference #: 2024-356, Filed.