Scan Test Cost And Power Reduction Through Systematic Scan Reconfiguration

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Summary

This paper presents segmented addressable scan (SAS), a test architecture that addresses test data volume, test application time, test power consumption, and tester channel requirements using a hardware overhead of a few gates per scan chain. Using SAS, this paper also presents systematic scan reconfiguration, a test data compression algorithm that is applied to achieve 10times to 40 times compression ratios without requiring any information from the automatic-test-pattern-generation tool about the unspecified bits. The architecture and the algorithm were applied to both single stuck as well as transition fault test sets