

**RECONFIGURABLE MEM-ELEMENT USING
CURRENT AMPLIFIERS**

BY

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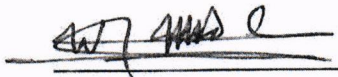
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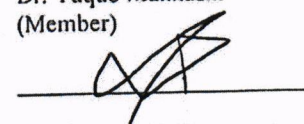
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ABSTRACT

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This thesis suggests a novel current amplifier (CA) based reconfigurable mem-element. Since mem-elements exhibit a state dependent on the history of signal (i.e., memory), they are expected to enable new unconventional applications. Although there is a plethora of mem-element emulators using different active devices, there are still areas that require improvements. Especially in the tunability and reconfigurability of the circuit. CAs have the potential advantages of offering both simplified circuit realizations and wide bandwidth. A mem-element using only CAs and a multiplier is developed in this work. Starting from the mathematical foundation of the linear model of a mem-element, this thesis provides a systematic approach to the design of a novel reconfigurable mem-element based on CAs. The designed CA has a gain-bandwidth product (GBW) of 95 MHz while consuming $234 \mu W$. The proposed mem-elements are capable of operating up to 1 MHz while consuming less than $4 mW$. In comparison with prior works, our proposed emulator achieves comparable power consumption while maintaining MHz range operation. In addition, it can be easily reconfigured to operate as any of the available mem-elements.

This thesis is organized as follows. Chapter 1 provides an overview of the history and the mathematical basis of memristors. Furthermore, it briefly discusses the most prominent research directions pertaining to memristors. Chapter 2 contains a comprehensive literature review of different types of mem-element emulator, highlighting the schemes and techniques popular in the

literature. In chapter 3, the proposed work is disclosed along with the mathematical basis that eventually lead to the realization of a CA and a reconfigurable mem-element. Chapter 4 discusses the transistor-level design details followed in order to achieve the desired performance. In chapter 5, simulation and experimental results are included to show the effectiveness and verify the operation of the proposed emulator. Lastly, chapter 6 concludes the thesis by summarizing the main highlights of the work and mentioning a few research directions that can be undertaken by future researchers.

ملخص الرسالة

الاسم الكامل: ابراهيم الخليفة

عنوان الرسالة: العناصر الكهربائية ذات الذاكرة القابلة لإعادة التشكيل باستخدام مضخمات التيار الكهربائي

التخصص: الهندسة الكهربائية

تاريخ الدرجة العلمية: ذو القعدة 1444 هـ

تقترح هذه الأطروحة دائرة محاكية للعناصر الكهربائية ذات الذاكرة باستخدام المضخمات الكهربائية. بما أن العناصر ذات الذاكرة لديها حالة تعتمد على القيم السابقة للإشارة خلالها، من المتوقع أنها سوف تمهد الطريق لتطبيقات جديدة. مع أنه هنالك الكثير من الدوائر المحاكية للعناصر ذات الذاكرة، فإنه لا يزال هنالك مجالاً للتحسين. خصوصاً من ناحية إعادة التشكيل والبرمجة. مضخمات التيار الكهربائي تمتلك إيجابيات متوقعة مثل التردد العالي وسهولة تصميم الدوائر. تم تصميم دائرة محاكية للعناصر الكهربائية ذات الذاكرة باستخدام مضخمات التيار الكهربائي في هذا العمل. بدأ من الخلفية الرياضية، تم تصميم الدوائر بشكل ممنهج. المضخم الكهربائي يمتلك $GBW = 95 \text{ MHz}$ ، بينما يستهلك $234 \mu W$ من الطاقة. الدوائر المحاكية للعناصر الكهربائية ذات الذاكرة المقترحة لديها المقدرة على العمل إلى 1 MHz بينما تستهلك أقل من 4 mW . مقارنة بالأعمال السابقة، الدوائر المحاكية للعناصر الكهربائية ذات الذاكرة المقترحة تظهر استهلاك طاقة مقارب بينما تعمل إلى نطاق MHz . بالإضافة، أنها قابلة لإعادة التشكيل بحيث تعمل كأى من العناصر الكهربائية ذات الذاكرة.

هذه الرسالة مرتبة كالآتي. الفصل الأول يقدم نظرة عامة عن المقاومة ذات الذاكرة والخلفية الرياضية. بالإضافة، فإنها تذكر بضع من الاتجاهات البحثية المشهورة في هذا المجال. الفصل الثاني يقدم مراجعة شاملة للأعمال السابقة، ويركز على ذكر أشهر الطرق لتصميم العناصر ذات الذاكرة. الفصل الثالث يقدم دائرة مضخم التيار الكهربائي المقترحة ودائرة محاكية للعناصر الكهربائية ذات الذاكرة قابلة لإعادة التشكيل. الفصل الرابع يذكر تفاصيل التصميم على مستوى الترانزستور المتبعة من أجل الحصول على المستوى المقصود. في الفصل الخامس، نتائج محاكاة وتجربة عملية ملحقه من أجل إثبات عملية وصحة العمل المقترح. أخيراً، الفصل السادس يختتم هذه الرسالة عبر تلخيص العمل وذكر بعض المواضيع التي يمكن للباحثين القادمين العمل على تحسينها.

CHAPTER 1 INTRODUCTION

1.1 Historical Background

In 1971, Chua published a research paper [1] predicting the existence of a fourth fundamental passive electrical component; the other three being resistors, capacitors, and inductors. Since the new component was basically a resistor with memory, it was named a memristor (its reciprocal is called a memductor). However, this finding did not spark a strong research effort into memristors. Many researchers began taking interest after the 2008 Hewlett-Packard (HP) publication [2] announcing that they have fabricated the first memristor and experimentally validated its operation. Many research directions in memristors which gained popularity since then could be identified. First, the study of the feasibility of emulating the neural networks in the brain using memristors. This is because the memristor has many similarities with the neurons; therefore, it has been envisioned to be the enabler of neuromorphic computing [3]. Second, the design of memories based on memristive crossbar arrays since they are promising in terms of lower power consumption and higher integration density [4]. Third, many works focus on the development of memristors at the device-physics level [5]–[7]. This is necessary for the memristor to be economically feasible. As of today, the fabrication of memristors is complex and expensive. In fact, very few companies offer memristors. One example of such companies is Knowm Inc. [8]. The inaccessibility of memristors have motivated the fourth research direction which is memristor-emulating circuits using CMOS process since it is widely available and affordable. On the way to this achievement, discrete components based emulators have been proposed. However, they are only meant as breadboard-level verification of the proposed emulators.

Memristors find applications in many fields for both analog and digital circuits. Although a memristor could be used as a variable/programmable resistor, a resistor with switches or a switched-capacitor based resistor already provide this functionality. An analog application in which the memristor find a unique role is in chaotic oscillators [9]–[11]. These oscillators exhibit behaviors that are very difficult to predict and highly dependent on the initial conditions of the circuit. Thus, they are used for encryption [12]. For digital circuits, memristors have provided means by which high-density with low power consumption memories could be achieved [13].

1.2 Mathematical Background

The concept of a passive component with memory has also been extended to include capacitors with memory (memcapacitors) and inductors with memory (meminductors); therefore, recent research work has been directed towards realizing universal emulators which can be configured to realize any of the three mem-elements. To see how a passive element achieves a behavior exhibiting memory, one can start from the following relations of the resistor, capacitor, and inductor, respectively:

$$R = \frac{dv}{di} \quad (1)$$

$$C = \frac{dq}{dv} \quad (2)$$

$$L = \frac{d\phi}{di} \quad (3)$$

where $i = \frac{dq}{dt}$ and $v = \frac{d\phi}{dt}$ relate the charge with the current, and the flux with the voltage, respectively. One can understand from (1)-(3) why a memristor is called the fourth fundamental passive element; it is the only relation left among V , I , q , and ϕ . It can be seen from (1)-(3) that the expression of the passive component is linear. The generalization of these relations to nonlinear expressions leads to the definition of three mem-elements:

$$M_R = R(i) = \frac{dv}{di} \quad (4)$$

$$M_C = C(v) = \frac{dq}{dv} \quad (5)$$

$$M_L = L(i) = \frac{d\phi}{di} \quad (6)$$

The model of the mem-element can be described by various functions which were proposed in literature such as linear, quadratic, and piecewise-linear functions. A designer of a mem-element emulator has to start by choosing one of these models and proceed systematically to realize it. For example, the linear model is in general given by:

$$M_G = \frac{1}{M_R} = \frac{lin}{v_{in}} = A + B \int_0^t V_{in} dt \quad (7)$$

$$M_C = \frac{q_{in}}{v_{in}} = \frac{\int_0^t I_{in} dt}{v_{in}} = C + D \int_0^t V_{in} dt \quad (8)$$

$$M_L^{-1} = \frac{1}{M_L} = \frac{lin}{\phi_{in}} = \frac{I_{in}}{\int_0^t v_{in} dt} = E + F \int_0^t \phi_{in} dt \quad (9)$$

where A , B , C , D , E , and F are constants dependent of the specific design of the emulator. Two important aspects of a mem-element. First, the memory behavior is captured by the integration term. Assuming that the input voltage is a series of positive pulses, then the mem-element value will increase accordingly. On the other hand, when the input voltage is a series of negative pulses, the mem-element value will decrease. As a result, the value of the mem-element could be controlled by a combination of positive and negative input pulses. Second, the plot of the constituent variables results in a number-eight-shaped pinched hysteresis loop (PHL) in their plane, as shown in Figure 1. For instance, a number-eight-shaped PHL in the I-V plane will be obtained for M_G (q-V for M_C and I- ϕ for M_L^{-1}). This loop serves as the single most important characteristic to verify that an emulator acts as a mem-element.

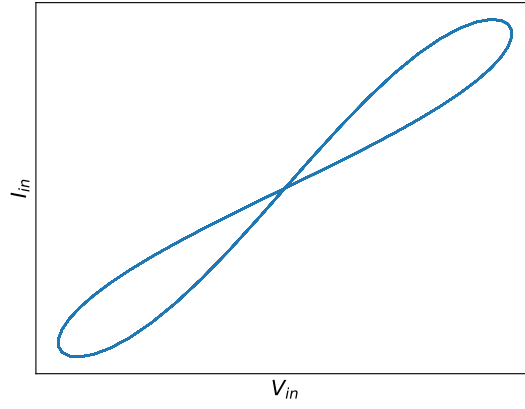


Figure 1. PHL.

In this research project, we intend to design a novel reconfigurable mem-element emulator using current amplifiers. The proposed design will be compared with the available solutions to highlight its projected advantages in terms of power consumption, maximum frequency of operation, tunability, and reconfigurability.

CHAPTER 2 LITERATURE REVIEW

In this chapter, recent mem-elements designed in CMOS and verified through simulation will be reviewed. Throughout the review, features unique to each design will be emphasized.

In [14], the author proposed a novel memristor consisting of seven transistors and a capacitor. The seven MOS transistors can be thought of as two G_m cells; the first is based on a differential pair with active load, and the second one is an inverter. This emulator is grounded and has an outstanding operation range of 50 MHz. The multiplication was achieved by injecting AC current through the biasing transistor in the first G_m cell as shown in Figure 2.

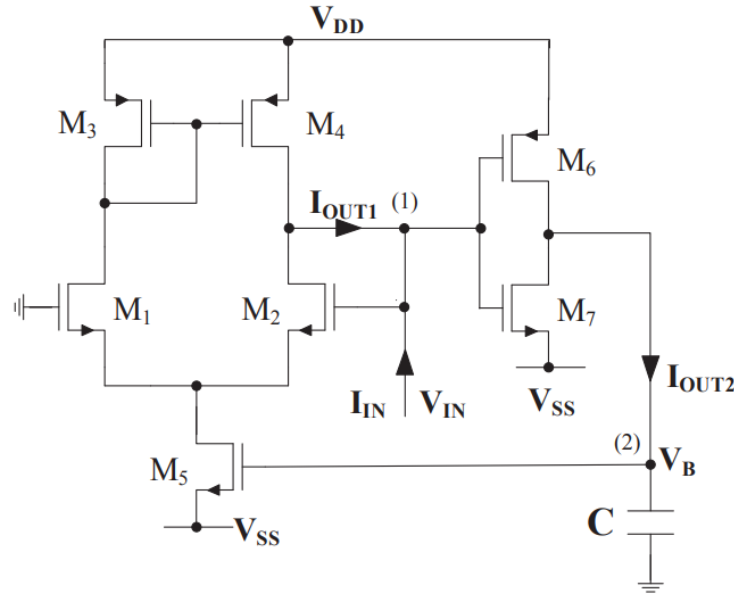


Figure 2. Memristor proposed in [14].

In [15], a simple floating memristor consisting of three MOSFETs, a constant current bias source, and a capacitor was proposed (see Figure 3). The concept of operation is based on a feedback circuit which controls a triode MOS such that it exhibits memristive behaviour. It achieves an operation range of 13 MHz with a power consumption of 6.7 nW. In addition, three

applications making use of the memristor were presented: a Schmitt trigger, a modulation scheme, and an associative learning circuit.

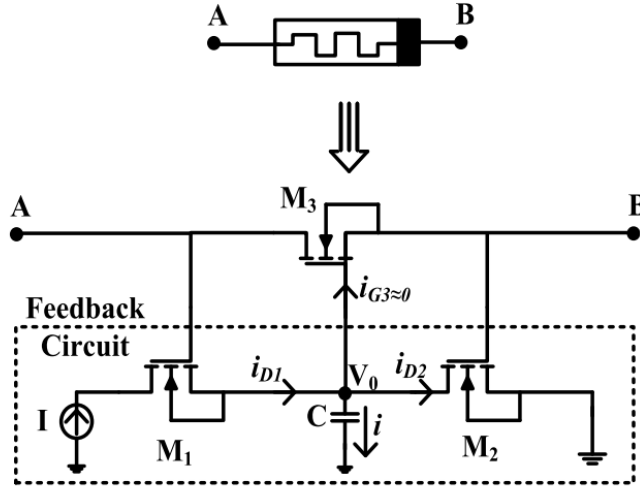


Figure 3. Memristor proposed in [15].

In [16], a grounded memristor using an OTA, a CCII, a resistor, and a capacitor was proposed, as shown in Figure 4. With respect to the grounded aspect of the proposed emulator, the authors mentioned that it is often observed that a grounded emulator has a superior frequency performance compared to the floating type. The circuit achieves an operation range of 26.3 MHz in simulations using 180 nm CMOS process with 9.6 mW power consumption.

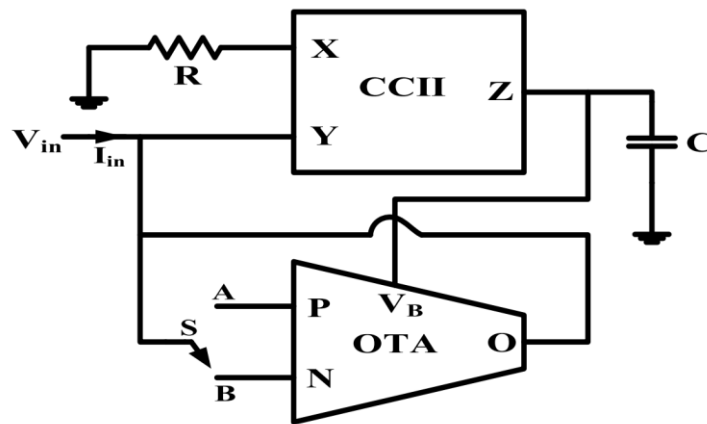


Figure 4. Memristor proposed in [16]

In [17], a MOS-only floating memristor was proposed, as shown in Figure 5. It consists of four transistors, one of them active as a MOS capacitor. The authors reported that a MOS capacitor was used in order to improve high frequency performance. Simulation results in 90 nm CMOS GPDK show a frequency performance of 50 MHz with a power consumption of $2.6 \mu\text{W}$. Without using an external current source, this design achieves a time dependent drain-source resistance which is used to obtain a memristor. Binary frequency-shift keying and logic gates were taken as applications in which the memristor was used.

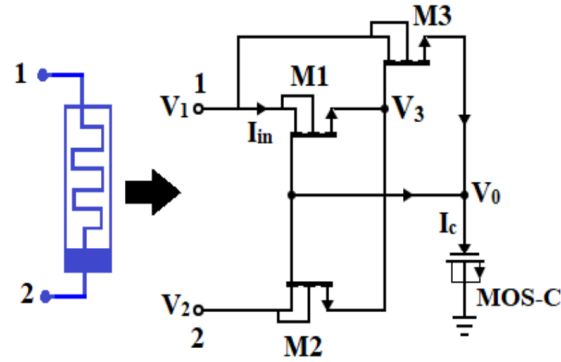


Figure 5. Memristor proposed in [17]

In [18], a 1.2 MHz memcapacitor emulator was proposed. The emulator consists of an OTA, a VDTA, and a buffer as shown in Figure 6. A power dissipation of 2.7 mW was reported. An adaptive learning circuit was presented as an application. Since an amoeba has memory, a circuit using a resistor, inductor, and a memcapacitor is used to model its behavior. The proposed memcapacitor was used in this model to verify its effectiveness.

In [19], to achieve high speed, a dynamic threshold voltage MOS (DTMOS) based memristor emulator was proposed, as shown in Figure 7. It achieves a performance of 3 MHz at a power consumption of $8.24 \mu\text{W}$. Through body biasing, the memristor is predicted to exhibit higher operation frequencies due to lower V_{th} . M1 and M2 are connected in parallel and are meant to operate in triode. The remainder of the circuit converts this resistance into a time varying

resistance. A chaotic oscillator and a high pass filter were used as examples showing the effectiveness of the proposed memristor.

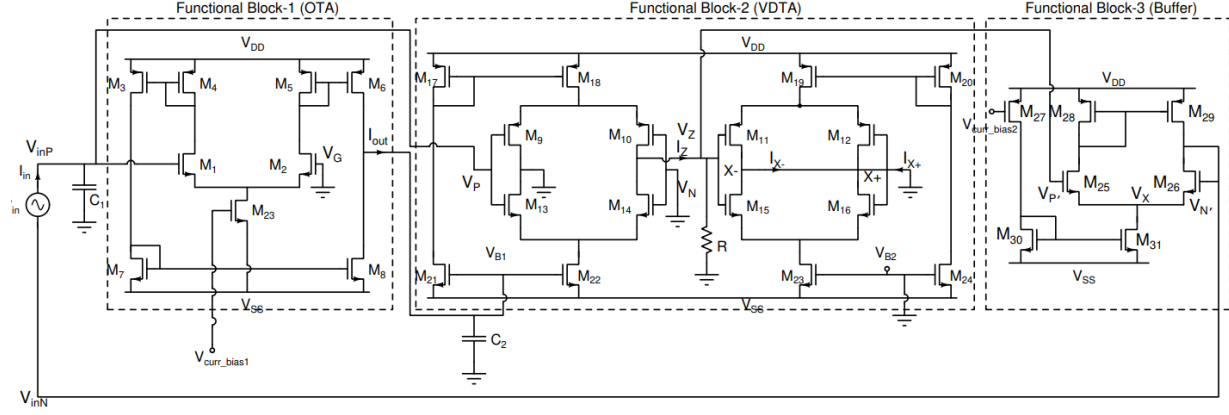


Figure 6. Memcapacitor proposed in [18].

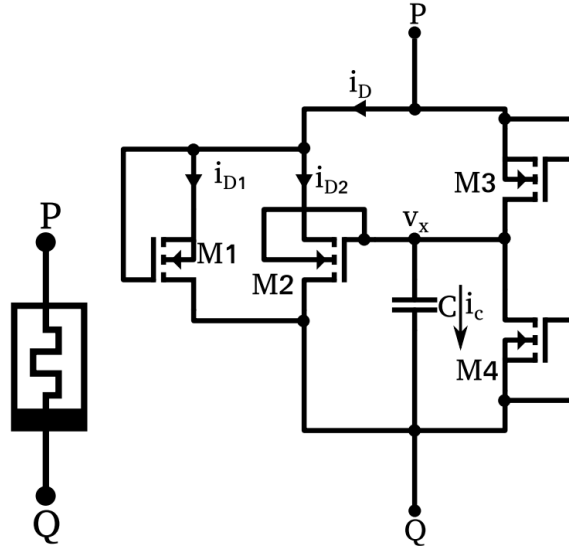


Figure 7. Memristor proposed in [19].

In [20], an electronically tunable floating memristor emulator was designed using current-mode blocks; namely, OTA and VDTA. The floating capability was achieved by using a G_m with double (differential) outputs. The design is capable of both incremental and decremental modes of operations by switching the connections among a, b, c, and d nodes. Specifically, incremental configuration uses a-c and b-d, whereas decremental uses a-d and b-c. Since the memristance

expression depends on technology parameters, process corner simulation show that the PHL is highly affected by process variations. The memristor operates up to 5 MHz. Circuit is shown in Figure 8.

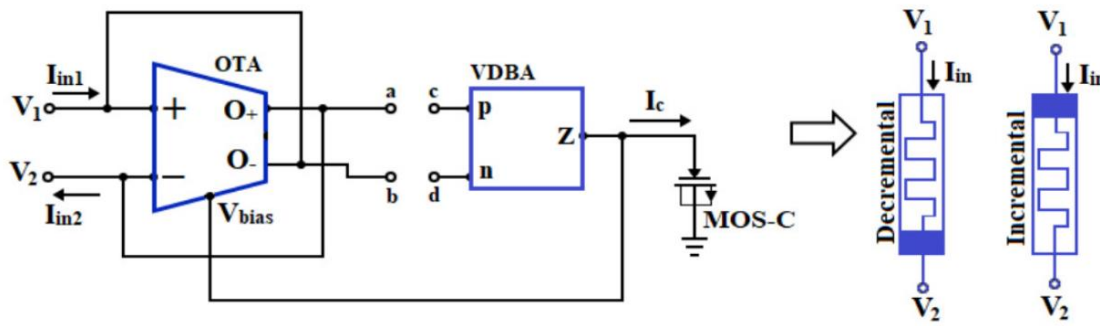


Figure 8. Memristor proposed in [20].

In [21], a current follower transconductance amplifier (CFTA) based memristor was proposed. A CFTA combines a current follower with a G_m cell. Contrary to previous design, this paper used Monte Carlo simulations to test the robustness of the circuit against process variations. It should be noted that process corner simulations is a stricter test than Monte Carlo simulations; however, Monte Carlo simulations are closer to reality since devices in close proximity are expected to experience similar process variations. The circuit, shown in Figure 9, is capable of operating up to 9 MHz.

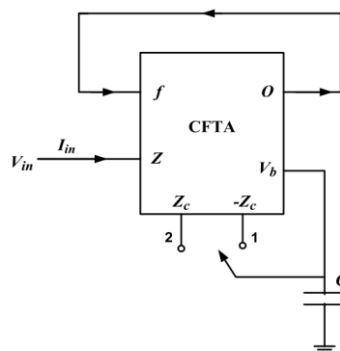


Figure 9. Memristor proposed in [21].

In [22], a VDTA based floating meminductor was proposed. Shown in Figure 10, this emulator operates up to 1 MHz. It can be seen that contrary to memristor emulators previously reviewed, this emulator contains two capacitors. This is expected since double integration of the input voltage is needed to realize a meminductor. A switch is included to accommodate both incremental and decremental modes of operation. An adaptive neuromorphic circuit exemplified by a model of amoeba was given as an application.

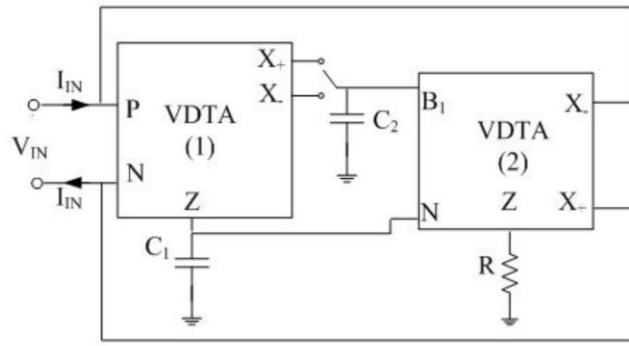


Figure 10. Meminductor proposed in [22].

Table 1 provides a summary of the aforementioned works. They can be divided into two main categories. First, mem-elements designed using transistors as the main active device [14], [15], [17], [19], [23] These designs are amenable to high frequency operation, low power dissipation, and small area consumption. However, in these designs the analytical analysis relies on approximate square-law MOS models, make frequent approximations, and realize a mem-element expression which depends on process parameters. The second category uses various active blocks such as G_m cells, VDTAs, CFTAs, among others, to realize mem-elements [16], [18], [20]–[22]. Generally, these designs have higher power and area requirements, while providing comparable frequency performance to transistor-based designs. Furthermore, they usually make less approximations in analytical derivation; therefore, they achieve more accurate mem-element expressions. Both approaches follow the linear model of the memristor due to its simplicity.

Table 1. Summary of prior CMOS mem-element emulators simulation results.

Ref.	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[22]
Technology	0.18 μm	0.18 μm	0.18 μm	90 nm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
Mem-element Type	M_R	M_R	M_R	M_R	M_C	M_R	M_R	M_R	M_L
Maximum Frequency	50 MHz	13 MHz	26.3 MHz	50 MHz	1.2 MHz	3 MHz	5 MHz	9 MHz	1 MHz
Active Devices	MOS	MOS	CCII, OTA	MOS	OTA, VDTA, Buffer	MOS	OTA, VDBA	CFTA	VDTA
Connection	Grounded	Floating	Grounded	Floating	Floating	Floating	Floating	Grounded	Floating
Power Consumption	-	6.7 nW	9.567 mW	2.6 μW	2.7 mW	8.2 μW	-	-	-
Voltage Supply	± 0.9 V	-	± 1.2 V	1.3 V	± 0.9 V	-	± 0.9 V	± 1.2 V	± 0.9 V
Verification	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.	Sim.

Several potential short comings of the previous works could be identified. First, the proposed designs are not reconfigurable. Second, no tuning mechanism was highlighted in order to combat fabrication nonidealities and to control the size of the PHL. In this paper, we propose a novel reconfigurable mem-element using CAs. Further, we show how the size of PHL can be controlled simply by changing the value of resistors.

CHAPTER 3 PROPOSED WORK

3.1 Introduction to Current Amplifier

A CA could be realized as either an open-loop amplifier or a negative feedback amplifier. The difference between the two being the gain (A_i) of the amplifier. If A_i is designed to be finite, for example by utilizing the gain of a current mirror, then it is usually used in an open-loop configuration. In contrast, an ideal negative feedback CA has $A_i \rightarrow \infty$. This paper proposes the use of the latter type; therefore, the remaining discussions refer solely to the second type.

Another point of interest is how to define the input and output terminals of the CA. The definition that will be followed in this work can be obtained through adjoint networks [24], from which it can be shown that a CA has one input terminal and two differential output terminals adhering to the following input-output relation

$$I_{out}^+ = -I_{out}^- = A_i I_{in} \text{ where } A_i \rightarrow \infty. \quad (10)$$

Figure 11 presents the CA symbol. The small signal model is shown in Figure 12. CA small signal model. Using this model, the effect of negative feedback on BW, R_{in} , and R_{out} can be derived. Assuming the gain A_i has a dominant pole w_o , it can be shown that the transfer function is given

by $\frac{I_{out}}{I_{in}} = \frac{\frac{A_i}{1+A_i\beta}}{1+\frac{s}{(1+A_i\beta)w_o}}$; thus, $BW_{CL} = (1 + A_i\beta)w_o$. It can also be shown that $R_{inCL} = \frac{R_{in}}{1+A_i\beta}$,

$R_{outCL} = R_{out}(1 + A_i\beta)$. This is an expected result since a CA employs shunt-series feedback.

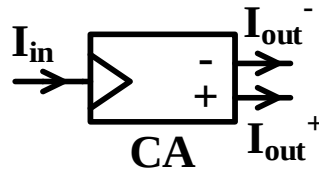


Figure 11. CA symbol.

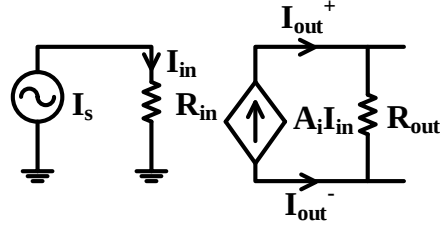


Figure 12. CA small signal model.

Many opamp circuits can be realized using the CA. Figure 13 shows a CA in a closed loop with two generalized impedances. Using this circuit, Table 2 shows how to implement a buffer, integrator, differentiator, inverting amplifier, and non-inverting amplifier. Along with a multiplier, these functions are all that is needed to realize a memristor.

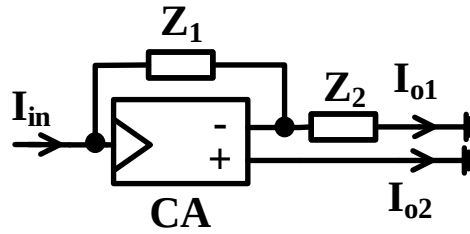


Figure 13. A generalized CA circuit.

3.2 CMOS Implementation of Current Amplifier

A transistor level implementation of CA has to meet the following requirements. First, since the input and output are current signals, the input impedance has to be small, whereas the output impedance has to be large. Second, to use negative feedback effectively, the circuit has to provide large gain. Third, the voltage at the input terminal has to be forced to ground potential for both AC and DC operations. If the third requirement is not met, systematic errors will be introduced in the circuit. In order to arrive systematically at the proposed circuit that meets these requirements, simple circuits that meet some of these requirements will be explored.

To meet the first requirement, a CG amplifier, shown in Figure 14, could be used. It has low R_{in} and high R_{out} ; however, this circuit has three problems. First, its gain is unity. Second, its

Table 2. Implementation of different mathematical relations using Figure 13.

Function	Z_1	Z_2	I_o
Buffer	short	open	$I_{o2} = I_{in}$
Integrator	$\frac{1}{sC}$	R	$I_{o1} = -\frac{I_{in}}{sRC}$
Differentiator	R	$\frac{1}{sC}$	$I_{o1} = -sRC I_{in}$
Inverting Amplifier	R_1	R_2	$I_{o1} = -\frac{R_1}{R_2} I_{in}$
Non-Inverting Amplifier	R_1	R_2	$I_{o2} = \left(1 + \frac{R_1}{R_2}\right) I_{in}$

input voltage is not at ground potential. Third, its DC output voltage is not well defined. The first issue can be resolved by adding another gain stage. Since differential outputs are needed, a differential pair comes to mind. Shown in Figure 15, the resulting circuit has a gain of $g_m r_o$ which can be designed to provide gain on the order of 100. To achieve higher gain, a cascode at the input can be used.

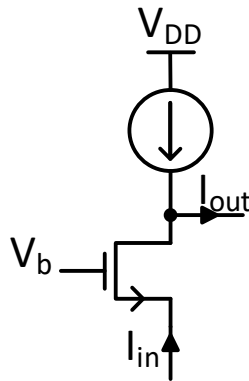


Figure 14. CG-based CA amplifier.

The second issue can be resolved by using local negative feedback as shown in Figure 16. Due to the finite loop gain, the negative terminal will not be at ground potential exactly. Instead, it will be at a potential equal to $\frac{V_{GS}}{loop\ gain}$. Another benefit of this configuration is that the input impedance will be lowered by the loop gain. This arises since the input transistor sees a small signal gate-source potential given by $v_{gs} = (1 + loop\ gain)V_{in}$; thus, the transconductance experienced will be $g_{mCL} = g_m(1 + loop\ gain)$. Finally, $R_{in} = \frac{1}{g_{mCL}} = \frac{1}{g_m(1+loop\ gain)}$. This result can also be derived by applying a test voltage source and measuring the resulting current.

The third issue arises two times in Figure 16. Once at the drain of the input transistor, and a second time at the output nodes of the differential pair. The former case will be discussed later, and the following discussion will refer to the drain terminal of the differential pair. One is tempted to resolve the third issue by employing common-mode feedback (CMFB) in the circuit in Figure 16; however, that would not work since in a CA configured as a buffer the output and input terminals are shorted, resulting in two negative feedback loops trying to force their own voltage level. Therefore, a better solution is to ensure at all times that the output terminals are connected to a known voltage. This is naturally achieved by connecting the output terminal to the input terminal (e.g., buffer), or by connecting the output terminal to the input terminal of another CA (i.e., next stage). If one of the output terminals is not needed (e.g., integrator) it must be grounded.

A fourth issue is ensuring that the differential pair gate terminals are biased at the same DC level, since otherwise a DC offset would arise in both outputs. This can be solved by exploiting symmetry as shown in Figure 17. In other words, the same mechanism that generates the DC level of the left transistor in the differential pair, is replicated for the right transistor.

Returning to the undefined DC level at the drain of the input transistor, it can be defined by imposing symmetry a second time as shown in Figure 18. This figure shows the final and complete

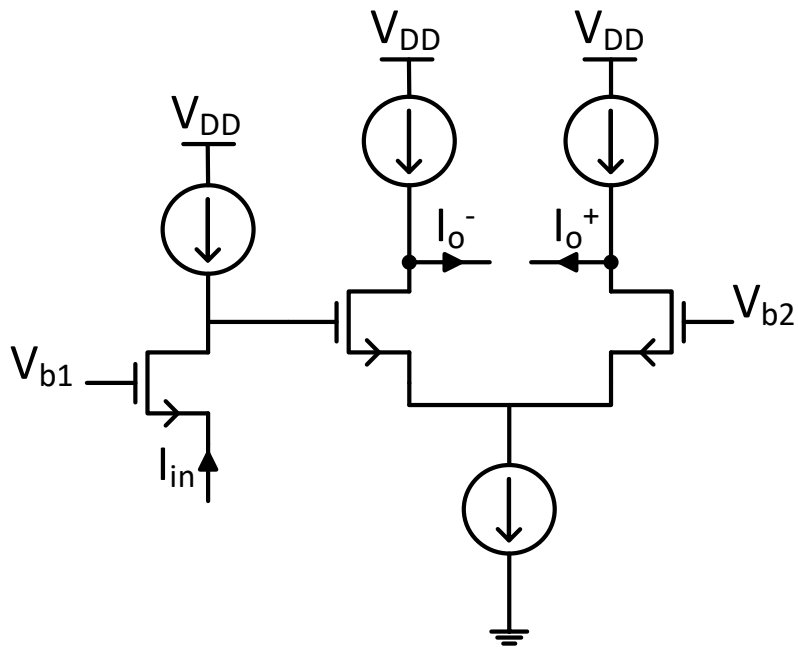


Figure 15. A CG CA amplifier with a differential pair output stage.

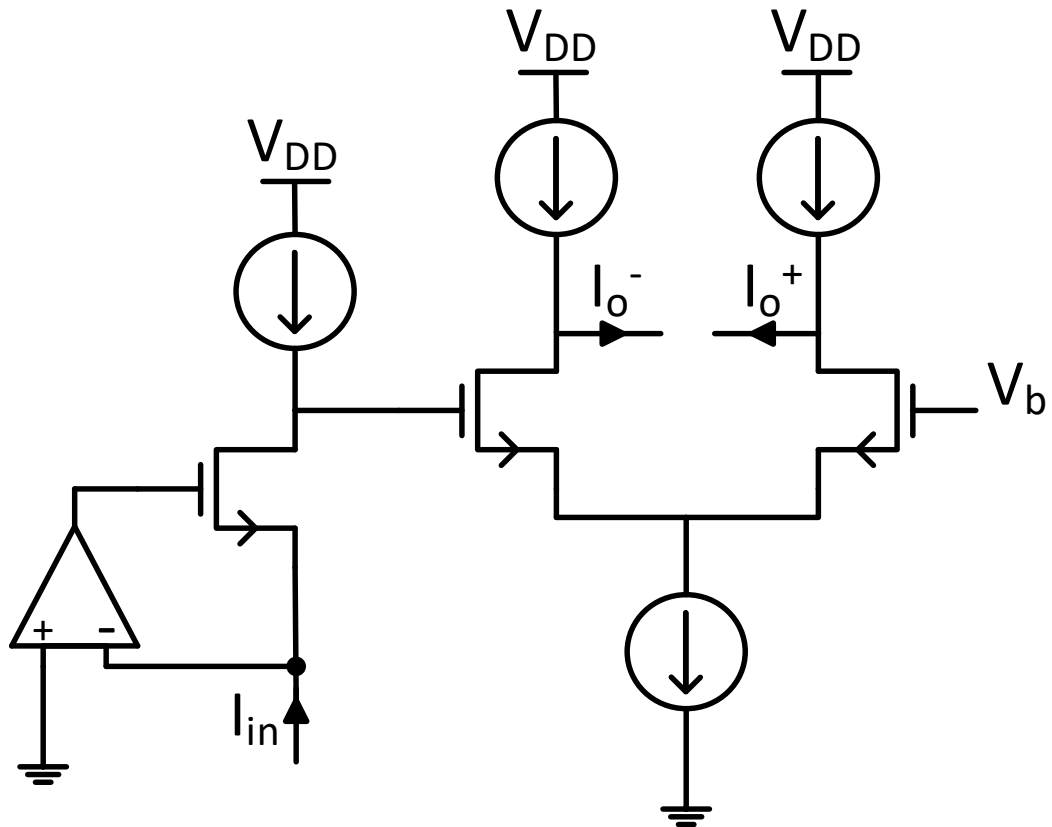


Figure 16. Negative feedback use to force input terminal to ground potential.

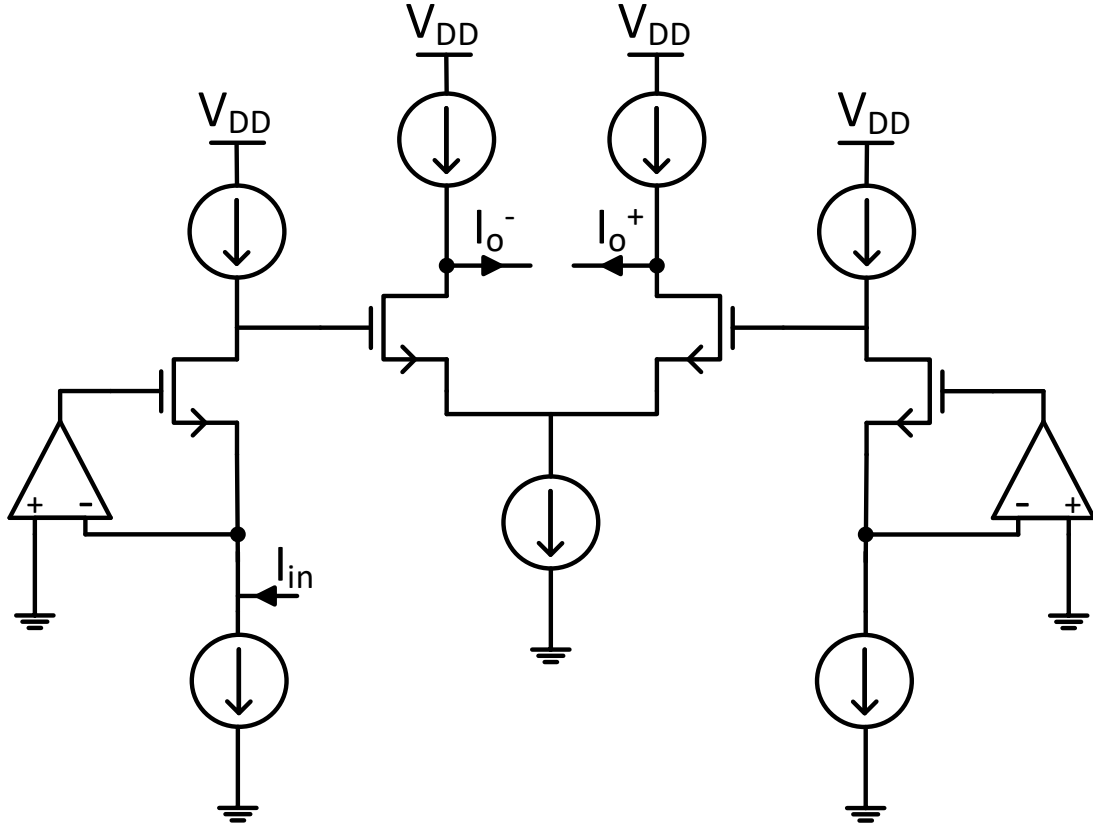


Figure 17. A scheme to force the DC level of the input differential pair to be equal.

circuit which incorporates all the previously discussed ideas. M1-M4 and I_b are used to generate a reference bias current for the circuit. V_{b2} and V_{b3} are bias voltages that can be generated using simple circuitry. M5-M9 constitute the input CG amplifier and its biasing circuitry. The signal is then copied to M14 resulting in a voltage at the drain of M15 given by $v_{d15} = g_m r_o^2 I_{in}$. To define the DC level at the drain of M15 (V_{d15}), M10-M13 are added. Since M10 cannot be biased through M5, otherwise $v_{d15} = 0$, M34-M38 are added to bias M10 at the same DC voltage that biases M14. Since M10-M13 and M14-M17 see the same bias conditions, then $V_{d15} = V_{d12} = V_{DD} - V_{sg13}$. M26-M29 and M30-M33 are added to bias M21 at the same gate voltage as M20. The final output current is given by $I_{op} = -I_{on} = g_m^2 r_o^2 I_{in}$. Since many poles exist in this circuit, dominant pole compensation was used by adding C_c at the drain of M15, which is the only high impedance

node in this circuit. This results in a pole given by $\omega_o = \frac{1}{g_{m1}r_o^2C_c}$. Therefore, the gain bandwidth product is given by $GBW = \frac{g_m}{C_c}$.

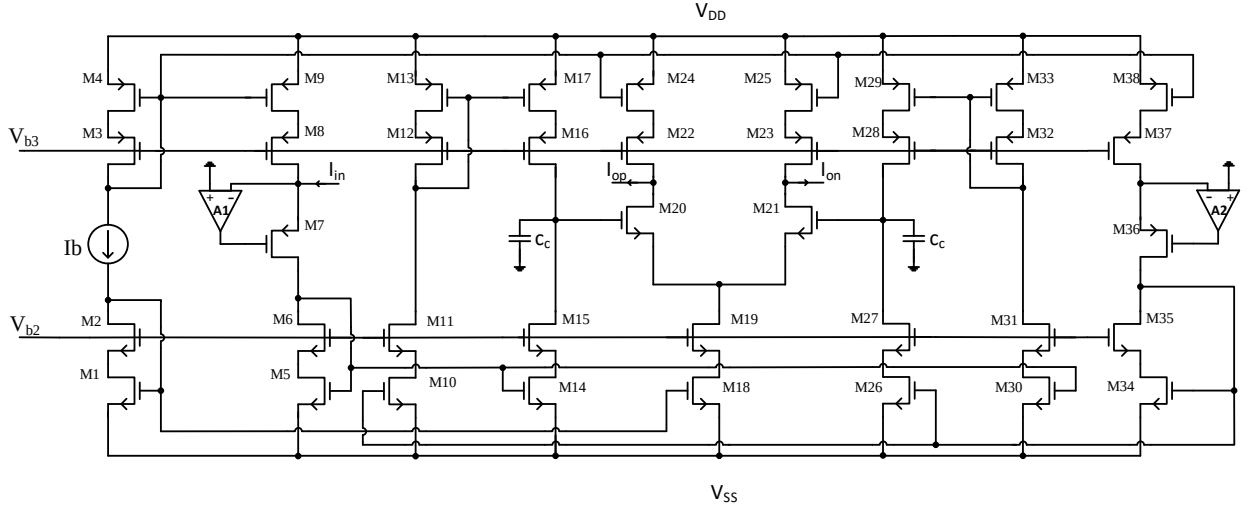


Figure 18. Proposed CA CMOS implementation.

3.3 Multiplier Implementation

To construct any mem-element, it is best to start by choosing a model. Most papers have chosen the linear model given by (7)-(9) due to its simple circuit realization. To demonstrate the thought process behind building any mem-element, a memristor whose model is given by (7) will be taken as an example. It can be seen from (7) that the model is for the memductance, which is the reciprocal of the memristor. Although in principle either one could be realized, the control variable will be different. For a memristor, an input current pulse is required to vary the resistance; therefore, it is called a charge-controlled memristor. On the other hand, a memductance requires voltage pulses to vary its conductance; therefore, it is called a flux-controlled memductance. A flux-controlled memductance was chosen for two reasons. First, the circuit realization is simpler. Second, in practice it is easier to apply a voltage signal rather than a current signal for measurements.

Rewriting (7) as

$$I_{in} = AV_{in} + BV_{in} \int_0^t V_{in} dt, \quad (11)$$

It can be observed that three fundamental operations, addition, integration, and multiplication are needed. Addition is easily achieved in the current domain since charge entering a node is conserved. Integration can be realized using the circuit in Figure 13 as explained in Table 2. To realize the multiplication operation, a non-linear circuit has to be introduced. To avoid using a mixture of active devices, a transistor-level approach was chosen. The non-linearity can be obtained from the characteristics of a MOS transistor operating in saturation. Assuming a classic square-law model

$$I_{DS} = \frac{1}{2} \beta \frac{W}{L} (V_{GS} - V_{th})^2 \quad (12)$$

where β is the transconductance factor, $\frac{W}{L}$ is the aspect ratio, V_{GS} is the gate-source voltage, and V_{th} is the threshold voltage. If it is desired to multiply two signals v_x and v_y , an ideal multiplier should generate an output equal to $A_{mul} v_x v_y$ where A_{mul} is the gain of the multiplier. To achieve this using (12), the following signals: $v_x + v_y$, $v_x - v_y$, $-(v_x - v_y)$, and $-(v_x + v_y)$ need to be generated. Then, applying each of these signals to four separate MOS transistors, the following expressions are obtained

$$I_{DS1} = \frac{1}{2} \beta \frac{W}{L} (V_{DC}^2 + 2V_{DC}(v_x + v_y) + v_x^2 + v_y^2 + 2v_x v_y) \quad (13)$$

$$I_{DS2} = \frac{1}{2} \beta \frac{W}{L} (V_{DC}^2 + 2V_{DC}(v_x - v_y) + v_x^2 + v_y^2 - 2v_x v_y) \quad (14)$$

$$I_{DS3} = \frac{1}{2} \beta \frac{W}{L} (V_{DC}^2 - 2V_{DC}(v_x - v_y) + v_x^2 + v_y^2 - 2v_x v_y) \quad (15)$$

$$I_{DS4} = \frac{1}{2} \beta \frac{W}{L} (V_{DC}^2 - 2V_{DC}(v_x + v_y) + v_x^2 + v_y^2 + 2v_x v_y) \quad (16)$$

$$I_o = I_{DS1} - I_{DS2} + (I_{DS4} - I_{DS3}) = \frac{1}{4} \beta \frac{W}{L} v_x v_y \quad (17)$$

where $V_{DC} = V_{GS} - V_{th}$.

From (17) it can be seen that to obtain the pure multiplication result, two subtractions and two additions are needed, this can be easily achieved using CAs since the signals are now in current domain. Note that also at the input of the multiplier, several additions and subtractions are needed. This is also easily achieved since the signals arriving at the input of the multiplier are in current domain. To convert them into voltage signals, a grounded resistor is connected to the gate of each transistor. Note that the bias is applied to source terminal and is designed to be equal to V_{DD} (or V_{SS}); therefore, there is no need to for bias-generating circuits. The last operation required in (7) is addition which is easily achieved since the output of the multiplier is in the current domain. The complete implementation of the multiplier is shown in Figure 19.

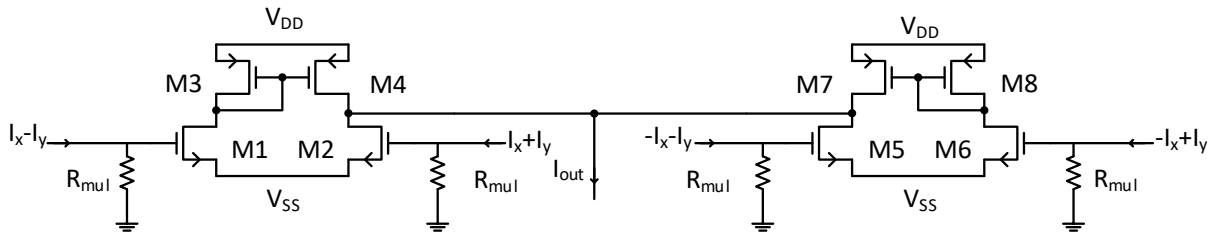


Figure 19. CMOS multiplier.

3.4 Mem-Element Implementation Using CA

Using the previously discussed circuits a reconfigurable mem-element could be implemented. In order to arrive at the final reconfigurable mem-element, we start by the simple case of a floating memristor as shown in Figure 20. CA1 converts the input voltage into current. CA3 is used to realize an integrator with a pole at $\frac{1}{R_{int}C_{int}}$. R_{sat} is used to reduce the integrator's gain at DC. Since the integrator's output can only be used once, CA4 is used as a buffer to generate multiple copies. These copies are generated by using multiple differential pair output stages with their gate terminals shorted as discussed in [25]. This is achieved at the cost of power consumption and slightly reduced GBW. Another method [26] that can be used in some configurations to generate

multiple copies is to add a resistor in parallel with Z_2 in Figure 13. Although this method does not consume additional power, it requires increasing the value of Z_2 to maintain the original function of the circuit unchanged. As a result, this method becomes impractical when large resistor values are required. Ignoring R_{sat} for simplicity, it can be shown that the input current and input conductance are given by

$$I_{in} = \frac{V_{in}}{R} + \frac{V_{in} A_{mul}}{RR_{int} C_{int}} \int \frac{V_{in}}{R} dt \quad (18)$$

$$G_{in} = \frac{I_{in}}{V_{in}} = M_G = \frac{1}{R} + \frac{A_{mul}}{RR_{int} C_{int}} \int \frac{V_{in}}{R} dt. \quad (19)$$

As a second step, a memcapacitor is implemented. By rewriting (8) as

$$I_{in} = \frac{d}{dt} (CV_{in} + DV_{in} \int_0^t V_{in} dt) \quad (20)$$

We notice that I_{in} is the same as the memristor case, with the only difference being differentiation. Thus, by adding two differentiators to the memristor, a memcapacitor is obtained as shown in Figure 22. R_n is added to reduce the gain of the differentiator at high frequencies. Ignoring R_n for simplicity, it can be shown that the integral of the input current and charge-voltage relation are given by

$$\int I_{in} dt = q_{in} = \frac{R_{diff} C_{diff} V_{in}}{R} + \frac{V_{in} R_{diff} C_{diff} A_{mul}}{RR_{int} C_{int}} \int \frac{V_{in}}{R} dt \quad (21)$$

$$\frac{q_{in}}{V_{in}} = M_C = \frac{R_{diff} C_{diff}}{R} + \frac{R_{diff} C_{diff} A_{mul}}{RR_{int} C_{int}} \int \frac{V_{in}}{R} dt. \quad (22)$$

As it turns out, the implementation of the meminductor requires more modifications to the memristor. First, rewriting (9) as

$$I_{in} = E \int_0^t V_{in} dt + F \int_0^t V_{in} dt \int_0^t (\int_0^t V_{in} dt) dt. \quad (23)$$

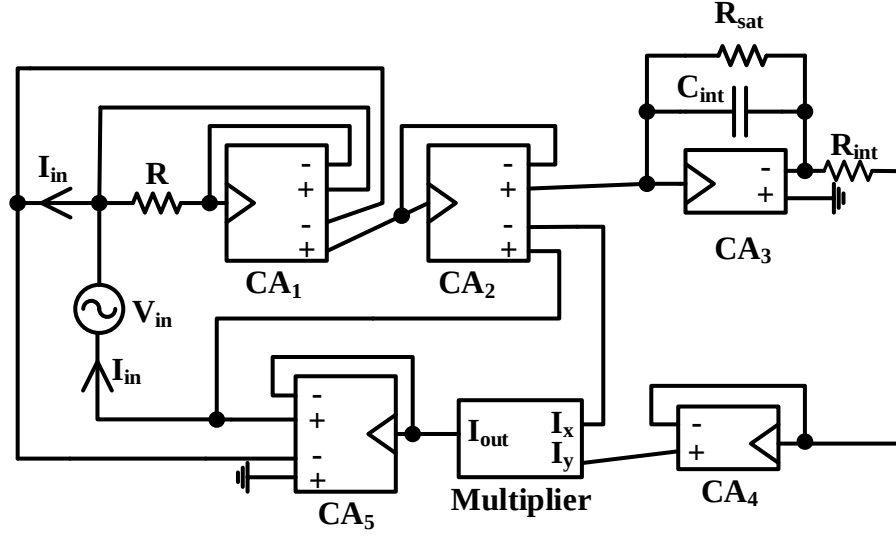


Figure 20. Proposed memristor.

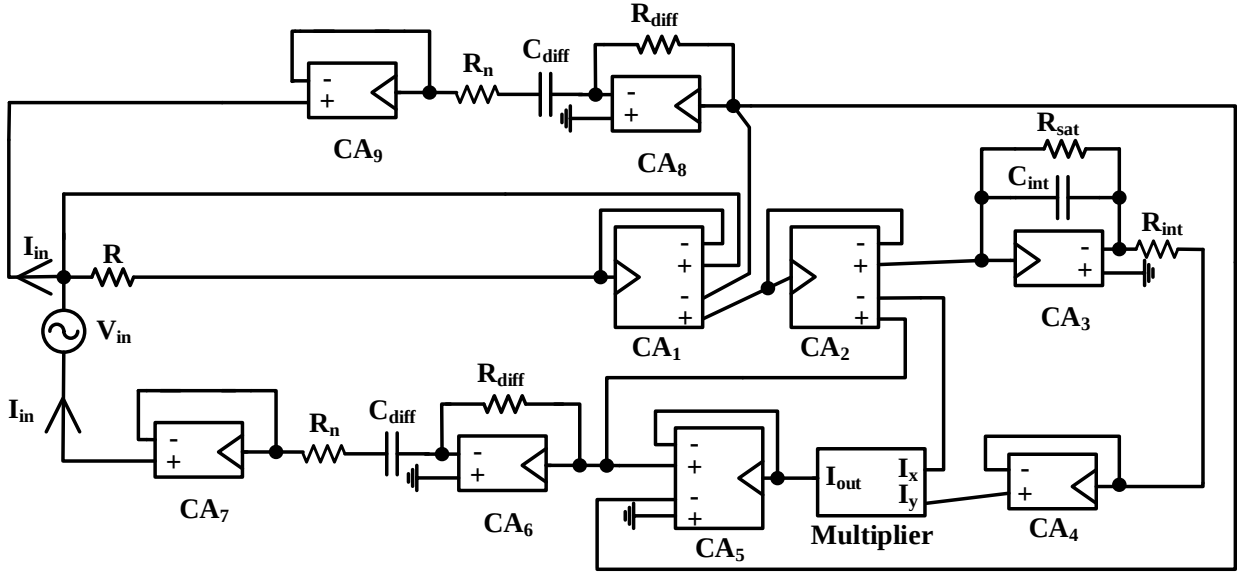


Figure 21. Proposed memcapacitor.

We notice that two integrations are needed. In addition, the inputs to the multiplier must be the integral of V_{in} and the double integral of V_{in} . Implementing these changes and making appropriate modification to the memristor results in the circuit shown in Figure 22. It can be shown that the input current and the current-flux relation are given by

$$I_{in} = \frac{\int V_{in} dt}{RR_{int}C_{int}} + \frac{A_{mul}}{R_{int}^3 C_{int}^3} \int \frac{V_{in}}{R} dt \int \left(\int \frac{V_{in}}{R} dt \right) dt \quad (24)$$

$$\frac{I_{in}}{\phi_{in}} = M_L^{-1} = \frac{1}{RR_{int}C_{int}} + \frac{A_{mul}}{R^2R_{int}^3C_{int}^3} \int \phi_{in} dt. \quad (25)$$

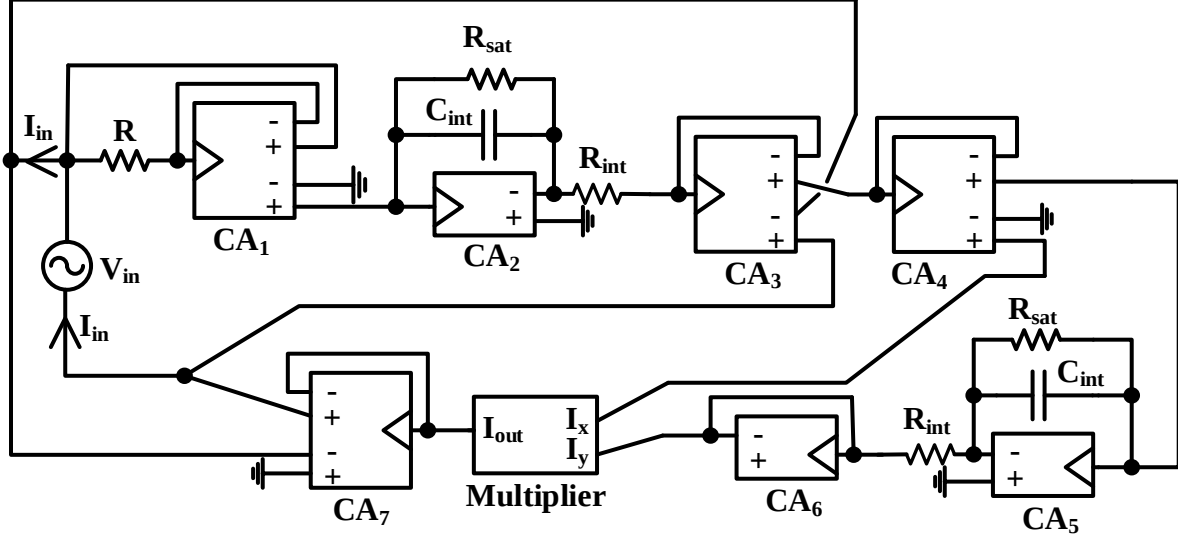


Figure 22. Proposed meminductor.

The final circuit that can implement any of the three mem-elements by reconfiguring the circuit can be developed as follows. It is noted that the main difference between memristor and memcapacitor implementation is a differentiation. On the other hand, the key difference between a memristor and a meminductor is an additional integrator. Therefore, by modifying the memristor to include an additional differentiator and integrator, a reconfigurable mem-element could be achieved as shown in Figure 23.

The operation of the reconfigurable mem-element can be explained as follows. At three junctures (blue, red, and green) in this circuit, a choice has to be made as to which mem-element is desired. Then, the appropriate switches must be closed. The need for the blue and green switches was already explained. The red switches are added since the linear term in a memristor and memcapacitor is the same (i.e., V_{in}), while it is different for a meminductor (i.e., $\int V_{in} dt$) as can be seen from (7)-(9). The operation of the reconfigurable mem-element is summarized in Table 3.

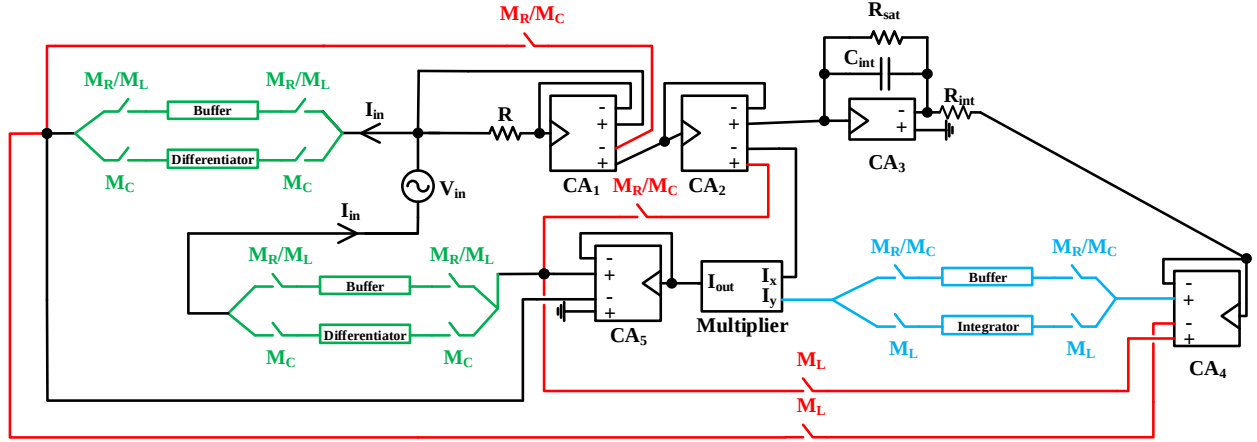


Figure 23. Proposed reconfigurable mem-element.

Table 3. Operation of reconfigurable mem-element.

Mem-element Type	Blue Switches		Red Switches		Green Switches	
	MR/MC	ML	MR/MC	ML	MR/ML	MC
Memristor	Closed	Open	Closed	Open	Closed	Open
Memcapacitor	Closed	Open	Closed	Open	Open	Closed
Meminductor	Open	Closed	Open	Closed	Closed	Open

CHAPTER 4 DESIGN DETAILS in TSMC 180 nm CMOS TECHNOLOGY

This chapter will walk the reader through the design methodology followed to determine W , L , and I_d for each transistor. Furthermore, it will discuss how to design a mem-element to obtain the desired operating frequency and size of the PHL. The proposed circuits were designed in 180 nm TSMC CMOS process in Cadence simulation environment.

4.1 Current Amplifier Design

There are several parameters pertaining to mem-elements that will govern CA design. First, since CA will be used in closed loop configurations, its gain must be at least 60 dB to obtain errors on the order of 0.1%. Second, if the target is a maximum operation frequency (f_{max}) for the mem-elements, then a rule of thumb is to satisfy the following inequality $GBW \geq 100f_{max}$. In our design, we choose $f_{max} = 1 \text{ MHz}$ as a balance between speed and power consumption. This implies $GBW = 100 \text{ MHz}$. All previously mentioned requirements should be achieved with minimal power dissipation and silicon area.

After establishing the design targets, we can proceed with transistor level design of the CA shown in Figure 18. We start by choosing the inversion level through g_m/I_d . To accommodate $\pm 0.9 \text{ V}$ supply, minimize power consumption, and achieve moderate speed, we choose $\frac{g_m}{I_d} = 15 \text{ V}^{-1}$ which is roughly at the center of moderate inversion. The choice of L is dictated by a compromise between speed and gain. The unity current gain transition frequency ($f_T = \frac{g_m}{2\pi C_{gg}}$) is a figure of merit that tells the designer how high C_{gg} must be to accommodate a desired g_m . A rule of thumb is to choose f_T such that it satisfies $f_T \geq 10GBW$. Whereas f_T is inversely proportional to L , the gain is proportional to L . It should be noted that the use of cascodes in our

design significantly improves the gain. In addition to the aforementioned issues, a small L reduces area. Therefore, $L = 360 \text{ nm}$ is chosen. The choice of I_d is dictated by speed, power consumption and reasonable W . While the former two are obvious, the latter is further explained as follows. Given a certain g_m/I_D and L , the current density $\left(\frac{I_d}{W}\right)^*$ is fixed. Then, for a given I_d , W is found through $W = \frac{I_d}{\left(\frac{I_d}{W}\right)^*}$. Therefore, the use of low bias current results in very small W approaching the minimum width set by foundry layout rules. In our design, $\left(\frac{I_d}{W}\right)_N^* = 3.082 \frac{\text{A}}{\text{m}}$, $\left(\frac{I_d}{W}\right)_P^* = 0.944 \frac{\text{A}}{\text{m}}$. Since a choice of $I_d = 1 \mu\text{A}$, results in W_N less than $1 \mu\text{m}$, we choose $I_d = 10 \mu\text{A}$, obtaining $W_N = 3.24 \mu\text{m}$, and $W_P = 10.6 \mu\text{m}$.

The remaining variables that are needed to complete the design of Figure 18 are the cascode transistor gate bias voltages V_{b2} and V_{b3} . We start by finding the range of possible values. This is given by the following inequalities

$$V_{SS} + V_{GS2} + V_{dsat1} < V_{b2} < V_{DD} + V_{th2} - V_{GS4} - V_{I_b} \quad (26)$$

$$V_{SS} + V_{GS1} + V_{I_b} + V_{th3} < V_{b3} < V_{DD} - V_{dsat4} - V_{GS3} \quad (27)$$

where V_{I_b} is the voltage drop across the current source I_b . In our design, we have $V_{DD} = -V_{SS} = 0.9 \text{ V}$, $V_{GS1} = V_{GS2} = 0.545 \text{ V}$, $V_{SG3} = V_{SG4} = 0.524 \text{ V}$, $V_{I_b} = 0.731 \text{ V}$, $V_{th2} = 0.532 \text{ V}$, $V_{th3} = -0.518 \text{ V}$, $V_{dsat1} = 86 \text{ mV}$, and $|V_{dsat4}| = 86 \text{ mV}$. Substituting in (26) and (27) we get $-0.269 \text{ V} < V_{b2} < 0.177 \text{ V}$, and $-0.142 \text{ V} < V_{b3} < 0.29 \text{ V}$. It is worth noting, however, that these inequalities neglected the body effect present in M2, and channel length modulation present in both M2 and M3. In addition, although V_{th} might have been useful in long channel transistor design, its definition becomes less useful in design when we think of the MOSFET's inversion regions as a continuum. Therefore, parameter sweeps in the calculated ranges were performed in

simulation in order to choose V_{b2} and V_{b3} that would bias the transistors closest to the desired operating point. Note that we expect V_{b3} to be closer to the upper limit, while V_{b2} is expected to be closer to the lower limit. It is found that $V_{b3} = -V_{b2} = 200 \text{ mV}$ meets the outlined requirements.

The compensation capacitor (C_c) value was calculated from $GBW = \frac{g_m}{2\pi C_c}$ to be $C_c = 239 \text{ fF}$.

Table 4. Summary of CA design.

Transistors	$\frac{g_m}{I_d}$	W	L	I_d
M1, M2, M5, M6, M10, M11, M14, M15, M20, M21, M26, M27, M30, M31, M34, M35	15 V^{-1}	$3.06 \mu\text{m}$	$0.36 \mu\text{m}$	$10 \mu\text{A}$
M3, M4, M7-M9, M12, M13, M16, M17, M22- M25, M28, M29, M32, M33, M36-M38	15 V^{-1}	$10.6 \mu\text{m}$	$0.36 \mu\text{m}$	$10 \mu\text{A}$
M18, M19	15 V^{-1}	$6.12 \mu\text{m}$	$0.36 \mu\text{m}$	$20 \mu\text{A}$

The amplifiers A1 and A2 in Figure 18 are identical and were implemented using a telescopic cascode topology as shown in Figure 24. PMOS input stage was chosen since it results in a compatible range for $V_{out} = V_{GS7} = V_{GS36} = -0.524 \text{ V}$.

4.2 Multiplier Design

The inversion level of the transistors constituting the multiplier is already set since $V_{GS} = V_{DD} = 0.9 \text{ V}$ is chosen to make the output DC level of the multiplier compatible with the DC level at the input of CA. Thus, the transistors are all biased in strong inversion with very large current densities. We choose a high L since this will result in a lower I_d/W and

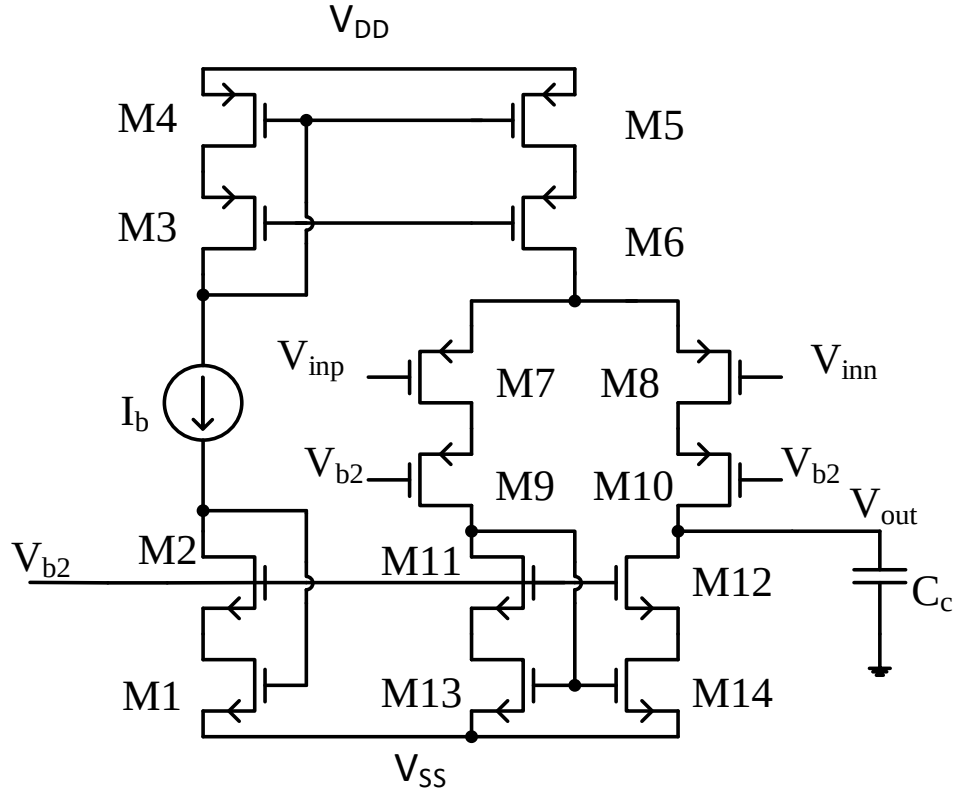


Figure 24. Telescopic cascode amplifier.

higher r_o . In our generated data, the highest L is 900 nm . Choosing $L = 900 \text{ nm}$, we then choose I_d to achieve a reasonable W . With reference to Figure 19, the design is summarized in Table 5.

One could ask why was not (17) to design the multiplier to achieve a desired gain. The answer is that (17) assumes a square-law model. It is known that the square-law model is ineffective in predicting the nonlinearity of the device since it implies infinite linearity in fully differential circuits. Instead, inspired by g_m/I_d methodology, we generated an output amplitude vs input amplitude table for the multiplier (shown in Table 6). Using Table 6, the gain of the multiplier ($A_{mul} = \frac{I_{out}}{I_x I_y}$) at a given input can be found. Thus, the mem-element design can take into consideration the multiplier's input-dependent gain.

4.3 Mem-Element Design

Any mem-element can be designed to achieve a PHL at a chosen operating frequency.

Following the methodology presented in [27], we start by assuming a sinusoidal input

Table 5. Summary of multiplier design.

Transistors	$\frac{g_m}{I_d}$	W	L	I_d
M1, M2, M5, M6	4.4 V^{-1}	$0.821 \mu\text{m}$	$0.9 \mu\text{m}$	$20 \mu\text{A}$
M3, M4, M7, M8	4.2 V^{-1}	$2.86 \mu\text{m}$	$0.9 \mu\text{m}$	$20 \mu\text{A}$

Table 6. Multiplier gain look-up table ($f_{in} = 1 \text{ MHz}$, $R_{mul} = 10 \text{ K}\Omega$).

$I_x = I_y = I_{in} (\mu\text{A})$	$I_{out} (\mu\text{A})$
1	0.033
2	0.13
3	0.277
4	0.493
5	0.765
6	1.113
7	1.5
8	2
9	2.5
10	3.1

$V_{in} = A_{in} \sin(w_o t)$, where A_{in} is the amplitude, and $w_o = 2\pi f_o$. Substituting for V_{in} in (18) we get

$$I_{in} = \frac{A_{in} \sin(w_o t)}{R} - \frac{A_{in}^2 A_{mul}}{4\pi f_o R^2 R_{int} C_{int}} \sin(2w_o t). \quad (28)$$

We see that I_{in} is nothing but the sum of the first harmonic (f_o) and the second harmonic ($2f_o$).

Next, we define

$$k = \left| \frac{\text{amplitude of second harmonic}}{\text{amplitude of first harmonic}} \right| = \frac{A_{in}A_{mul}}{4\pi f_o R R_{int} C_{int}}. \quad (29)$$

From (29), we observe the following. When $k = 0$, the second harmonic vanishes, and the input impedance reduces to a linear resistor. Then, as k increases, the PHL becomes more prominent. At $k = 1$, the maximum PHL is achieved. For $k > 1$, the PHL behavior starts to fade. This can be explained by noting that if k is very large, then input impedance is sinusoidal. Thus, we have to ensure $0 < k < 1$ for proper operation. Furthermore, we note that $k \propto \frac{1}{f_o}$. Therefore, to operate the memristor at high frequencies, k has to be updated through the other the remaining variables in (29).

Using similar logic, the same analysis could be extended to memcapacitors and meminductors.

For memcapacitors, (21) will become

$$q_{in} = \frac{A_{in} R_{diff} C_{diff} \sin(w_o t)}{R} - \frac{A_{in}^2 A_{mul} R_{diff} C_{diff}}{4\pi f_o R^2 R_{int} C_{int}} \sin(2w_o t), \quad (30)$$

$$k = \left| \frac{\text{amplitude of second harmonic}}{\text{amplitude of first harmonic}} \right| = \frac{A_{in} A_{mul}}{4\pi f_o R R_{int} C_{int}}. \quad (31)$$

For meminductors, using $\phi_{in} = \int V_{in} dt = A'_{in} \sin(w_o t)$ where A'_{in} is in Wb (V*s), (24)

becomes

$$I_{in} = \frac{A'_{in} \sin(w_o t)}{R R_{int} C_{int}} - \frac{A_{in}'^2 A_{mul}}{4\pi f_o R^2 R_{int}^3 C_{int}^3} \sin(2w_o t), \quad (32)$$

$$k = \left| \frac{\text{amplitude of second harmonic}}{\text{amplitude of first harmonic}} \right| = \frac{A_{in}' A_{mul}}{4\pi f_o R R_{int}^2 C_{int}^2}. \quad (33)$$

Using (30)-(33), we can design the memcapacitor and meminductor to achieve the desired performance at the desired frequency.

CHAPTER 5 RESULTS AND DISCUSSION

This chapter will present the results of proposed circuits. The results are obtained from simulating the circuits in Cadence using TSMC 180 nm CMOS technology. These results are from schematic simulation; post-layout simulations were not performed. Instead, breadboard experiments were conducted to verify the concept.

5.1 Current Amplifier

In Figure 25, the magnitude response of the CA is shown. The dc gain is 64 dB, $GBW = 94.6\text{ MHz}$, and $phase\ margin = 60^\circ$. Figure 26 shows the input impedance (Z_{in}) of the CA. It can be seen that it has an inductive behavior as expected from a CG stage. Low impedance is maintained even at high frequencies thanks to the internal and global feedback networks. Figure 27 shows the output impedance (Z_{out}) frequency response. Due to parasitic capacitors, it decreases at high frequencies. However, it has a satisfactory performance at the frequencies of interest. A summary of CA performance is presented in Table 7.

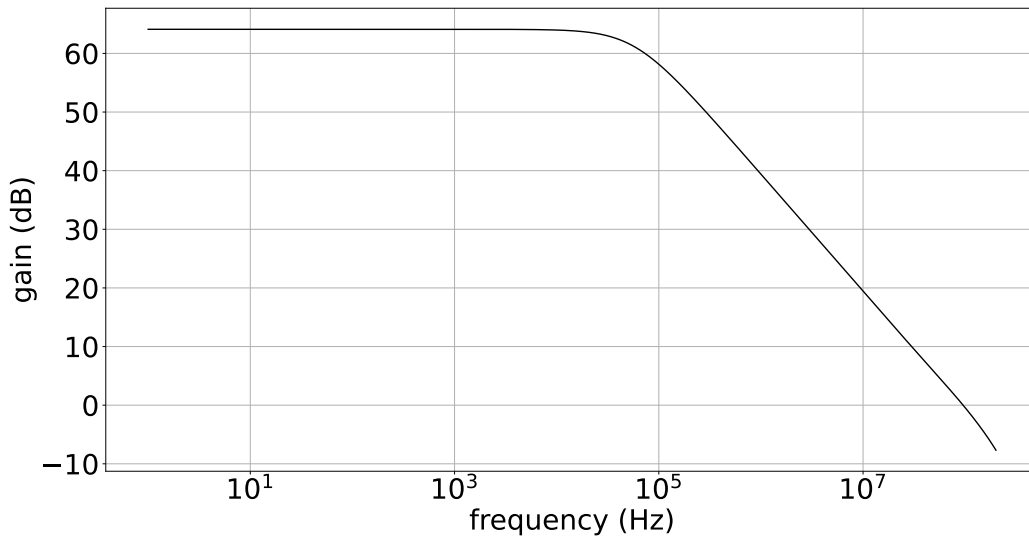


Figure 25. CA magnitude frequency response.

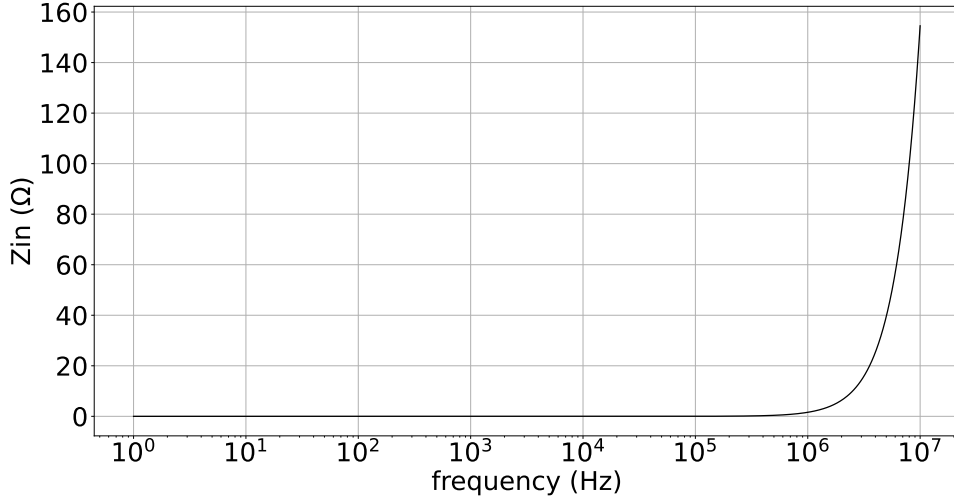


Figure 26. Input impedance frequency response.

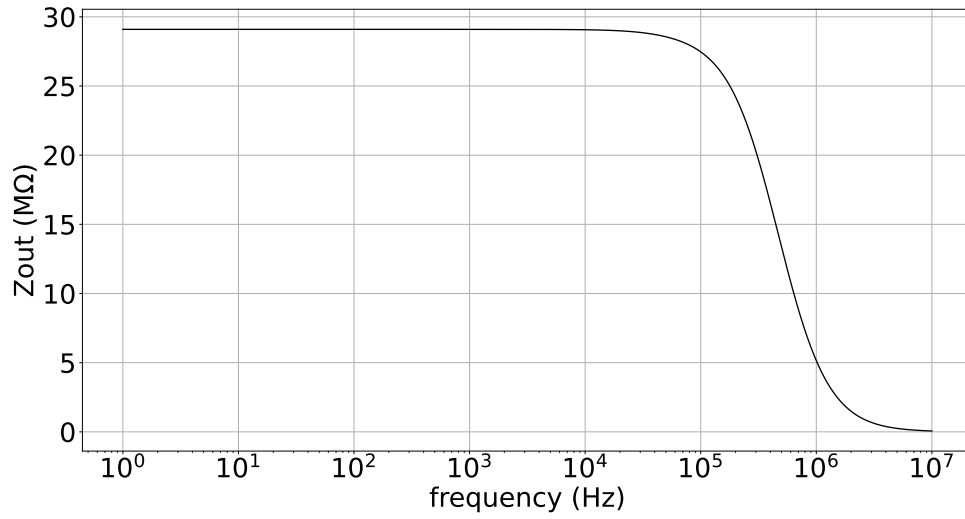


Figure 27. Output impedance frequency response.

5.2 Mem-Element

In this section, we will present the achieved PHL for the mem-element circuits at different input frequencies (f_{in}), different input voltages (V_{in}), and different gain settings. In all the simulations, $R_{mul} = 10\text{ K}\Omega$, $R_{int} = R_{diff} = 30\text{ K}\Omega$, $R_{sat} = 10R_{int}$, $R_n = 1\text{ K}\Omega$, and $C_{int} = C_{diff} = 5.3\text{ pF}$. R is used to control gain. For a gain of unity $R = R_{mul}$.

Table 7. CA performance summary.

Supply	$\pm 0.9 V$
CMOS Technology	180 nm
Gain	64 dB
GBW	94.6 MHz
Phase Margin	60°
$R_{in,CL}$ @ 1 MHz	1.6 Ω
$R_{out,CL}$ @ 1 MHz	5 M Ω
Input offset voltage	51 μV
Power Dissipation	234 μW
Area*	631.2 μm^2

*: Area estimated using WL (μm^2) for transistors, and capacitance density ($\frac{fF}{\mu m^2}$) from PDK for capacitors.

Note that R_{sat} can be implemented using a MOS operating in triode. A method to make the PHL larger is to add gain to second harmonic. This can be done by making the buffer after the multiplier have gain, or by making $\frac{R_{mul}}{R} > 1$.

Figure 28-Figure 31 show V_{in} and I_{in} waveforms, and the resultant plot in the I-V plane for different V_{in} and f_{in} . Figure 32-Figure 35 show V_{in} and Q_{in} waveforms, and the resultant plot in the Q-V plane for different V_{in} and f_{in} . Figure 36-Figure 39 show ϕ_{in} and I_{in} waveforms, and the resultant plot in the I- ϕ plane for different V_{in} and f_{in} . In all figures, we observe that at a given frequency, the pinched loop becomes more pronounced as V_{in} increases. This is because k increases. A summary of the performance of the proposed mem-elements is given in Table 8.

Comparing the achieved performance with the ones presented in Table 1, we observe that our design achieves comparable power consumption in comparison to [16], [18]. Furthermore, it is reconfigurable, provides simple tuning using ratios of resistors, and floating. This is achieved while maintaining MHz frequency of operation.

Table 8. Summary of proposed mem-elements performance.

Mem-element	Memristor	Memcapacitor	Meminductor
Technology	180 nm	180 nm	180 nm
Maximum Frequency	1 MHz	1 MHz	1 MHz
Active Device	CA	CA	CA
Floating Connection	Yes	Yes	Yes
Power Dissipation	2.5 mW	3.5 mW	3 mW
Supply	$\pm 0.9 V$	$\pm 0.9 V$	$\pm 0.9 V$
Model	Linear	Linear	Linear
Verification	Sim.	Sim.	Sim.
Area	5618 μm^2	12391 μm^2	9637 μm^2

*: Resistors' area estimated using sheet resistance ($\frac{\Omega}{\square}$) from PDK.

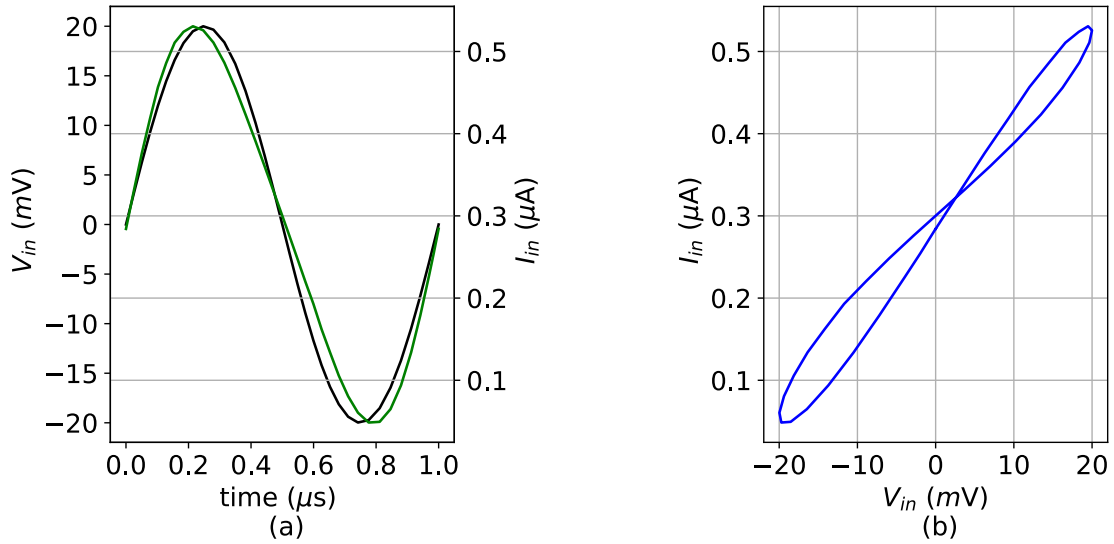


Figure 28. Memristor PHL. $V_{in} = 10 mV$, $f_{in} = 1 MHz$. (a) time domain waveforms and (b) PHL.

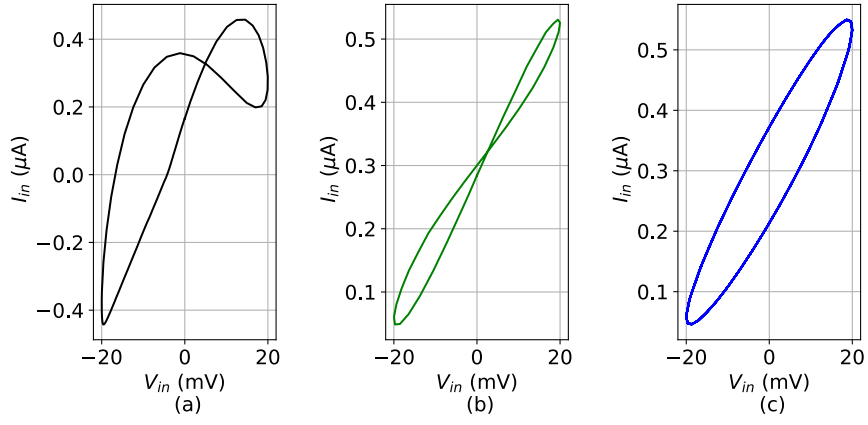


Figure 29. Memristor PHL variation with frequency. (a) 100 KHz, (b) 1 MHz, and (c) 10 MHz.

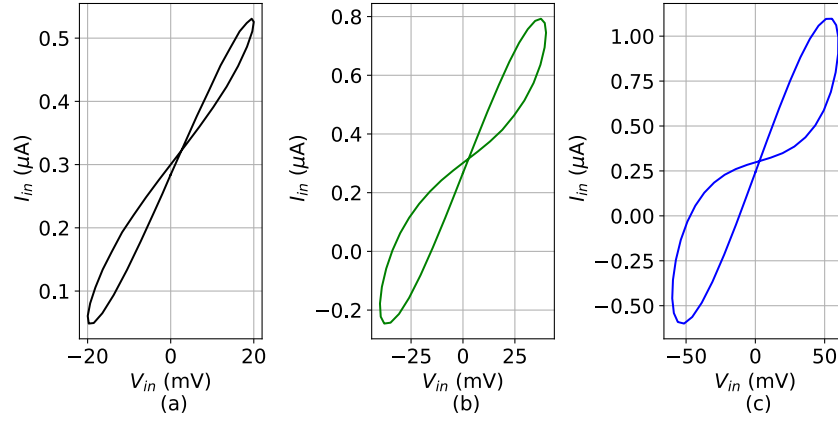


Figure 30. Memristor PHL variation with input voltage. (a) 10 mV, (b) 20 mV, and (c) 30 mV.

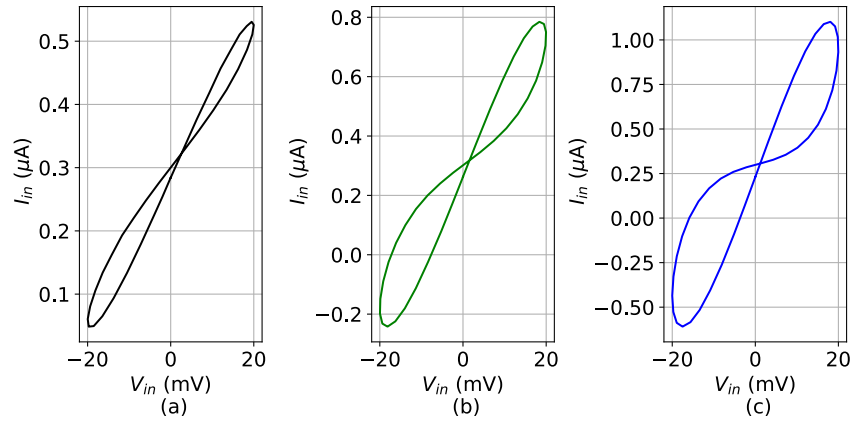


Figure 31. Memristor PHL variation with gain. (a) gain = 1, (b) 2, and (c) 3.

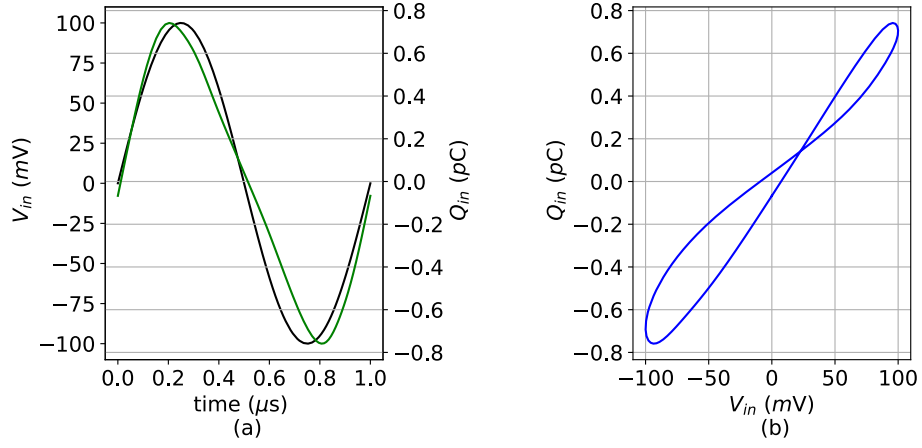


Figure 32. Memcapacitor PHL. $V_{in} = 50 \text{ mV}$, $f_{in} = 1 \text{ MHz}$. (a) time domain waveforms and (b) PHL.

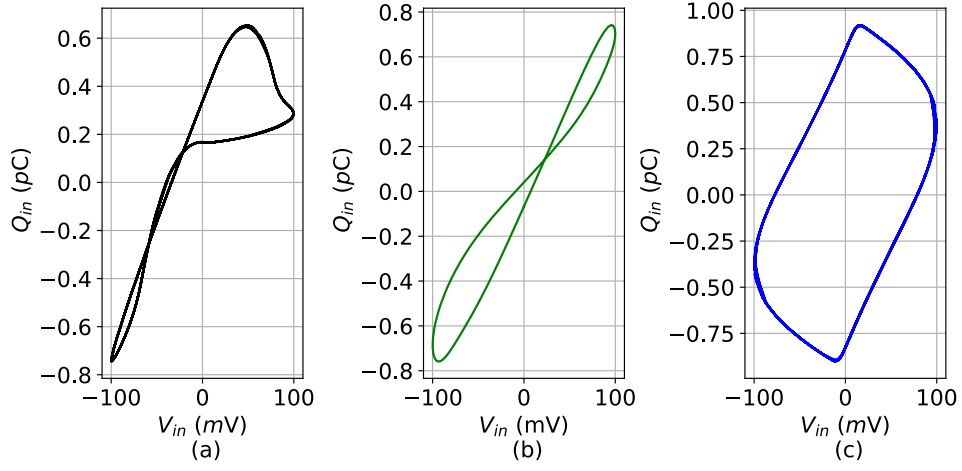


Figure 33. Memcapacitor PHL variation with frequency. (a) 100 KHz, (b) 1 MHz, and (c) 2 MHz.

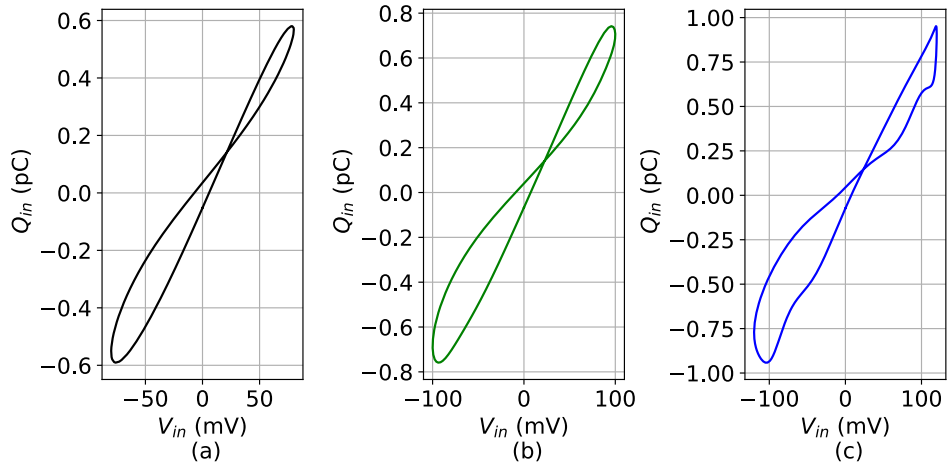


Figure 34. Memcapacitor PHL variation with input voltage. (a) 40 mV, (b) 50 mV, and (c) 60 mV.

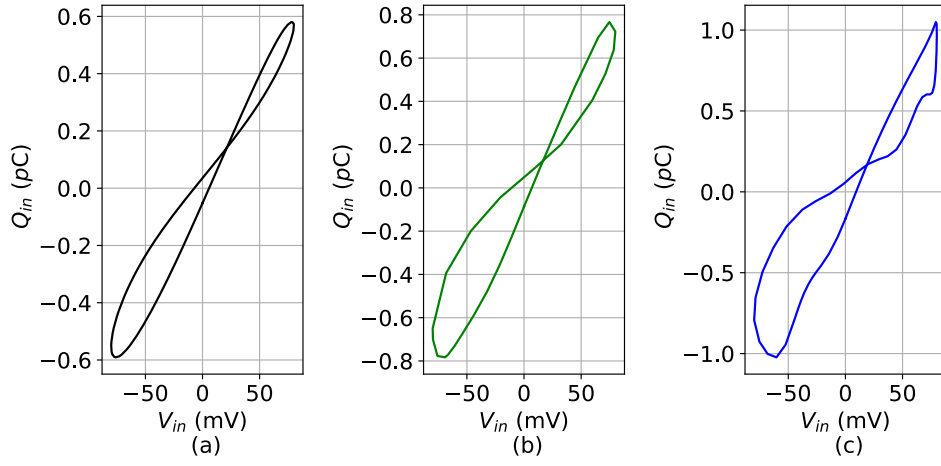


Figure 35. Memcapacitor PHL variation with gain. (a) gain = 1, (b) 2, and (c) 3.

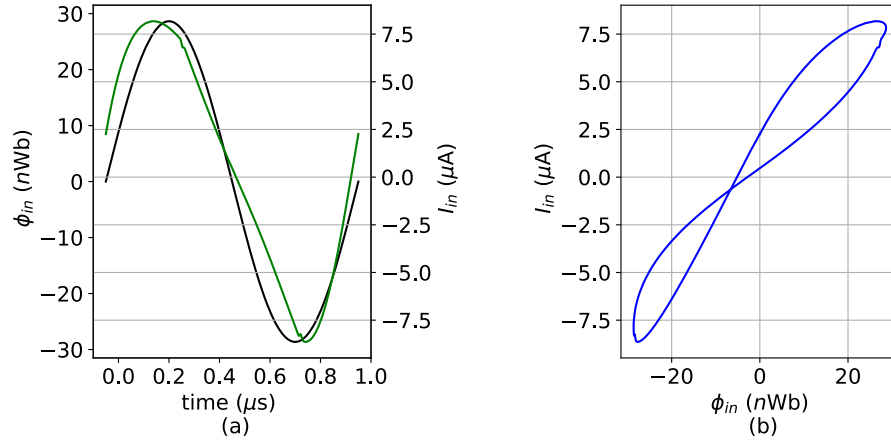


Figure 36. Meminductor PHL $V_{in} = 90$ mV, $f_{in} = 1$ MHz. (a) time domain waveforms and (b) PHL.

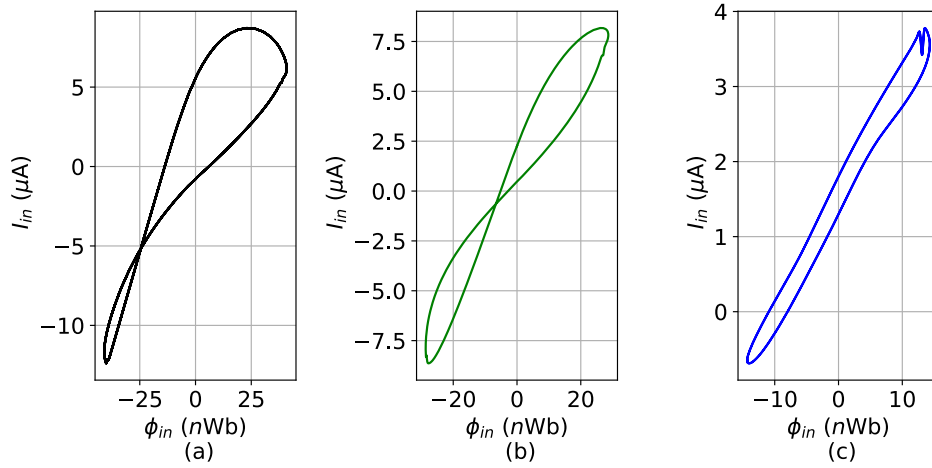


Figure 37. Meminductor PHL variation with frequency. (a) 700 KHz, (b) 1 MHz, and (c) 2 MHz.

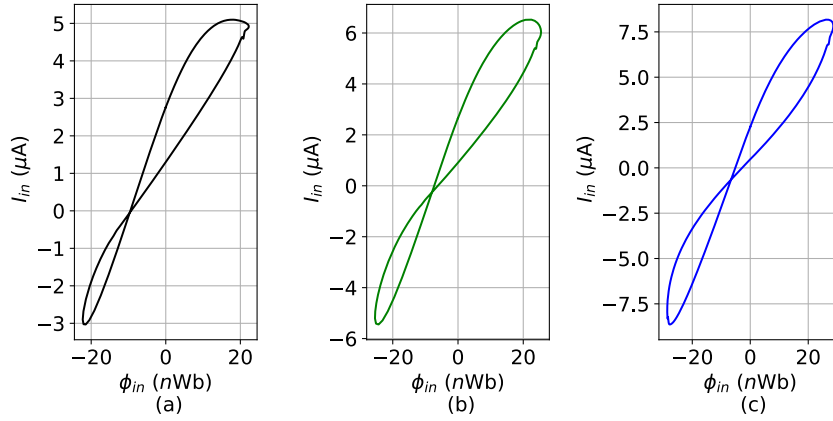


Figure 38. Meminductor PHL variation with input voltage. (a) 70 mV, (b) 80 mV, and (c) 90 mV.

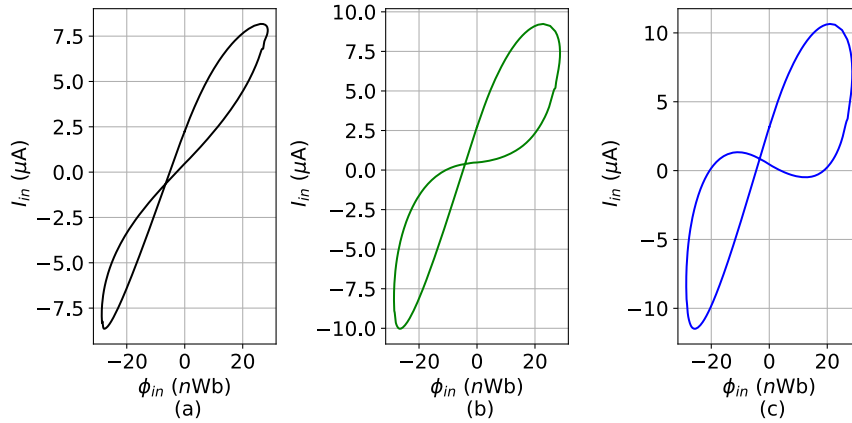


Figure 39. Meminductor PHL variation with gain. (a) gain = 1, (b) 2, and (c) 3.

5.3 Breadboard Prototype

To verify simulations, breadboard experiments were conducted. Using AD844, LM358, and CD4007UBE, a grounded memristor was constructed. AD844 was used in lieu of a CA, LM358 was used as an inverter to generate negative copies of current, and CD4007UBE was used to implement a multiplier. Two 9 V batteries were used as supplies.

Shown in Figure 40 is the breadboard implementation. Figure 41-Figure 44 show the time domain waveforms and PHL as the frequency increases. These results were obtained with a 15 nF capacitor in the integrator. To increase the frequency of operation, a 1.5 nF capacitor was used to obtain Figure 45-Figure 48. It can be seen that time domain waveforms have the same shape as in

simulation. Further, for a given pole frequency, as the frequency increases the PHL size becomes smaller. Lastly, the frequency of operation can be increased by increasing the pole frequency of the integrator.

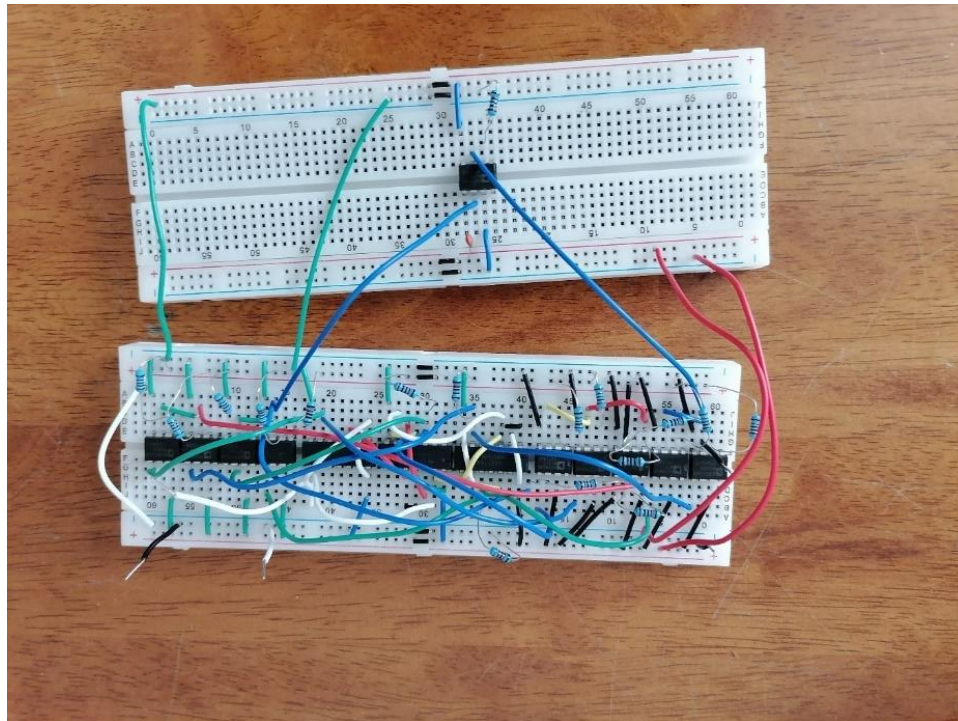


Figure 40. Breadboard implementation of a grounded memristor.

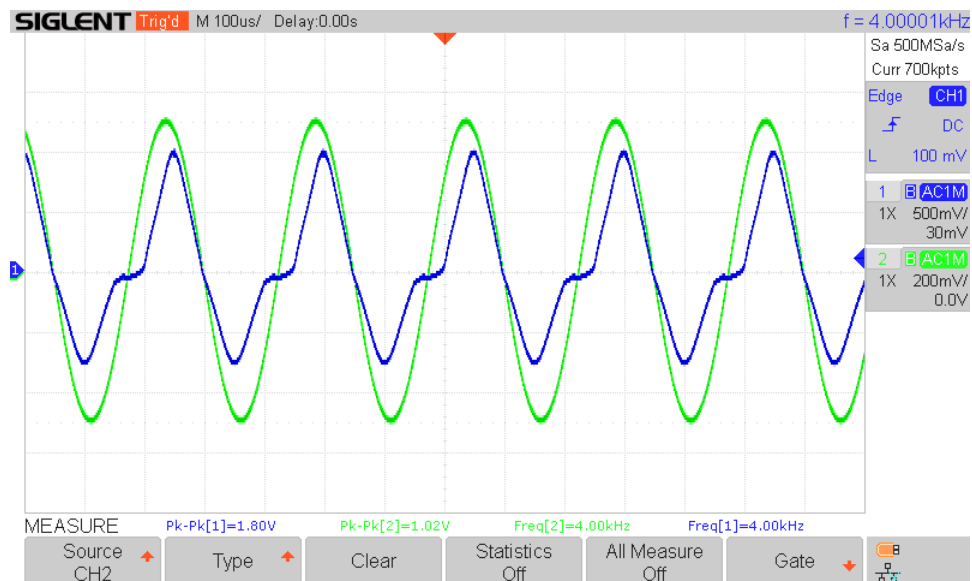


Figure 41. Measured Waveforms (4 KHz).

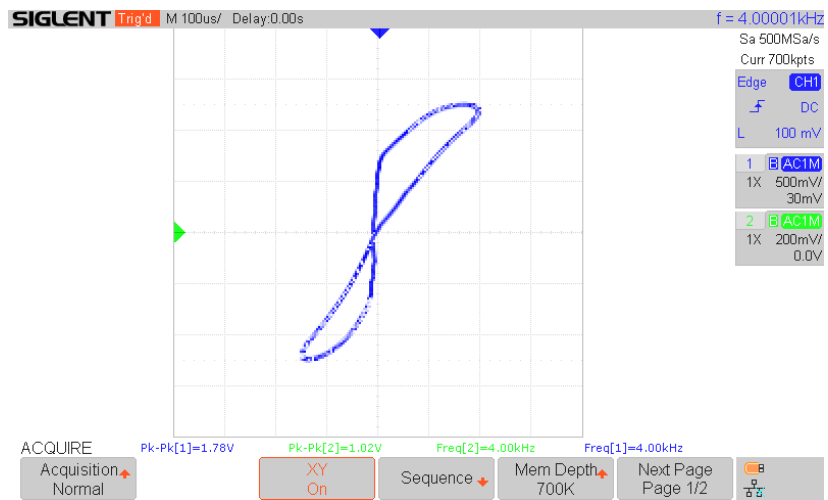


Figure 42. Measured PHL (4 KHz).

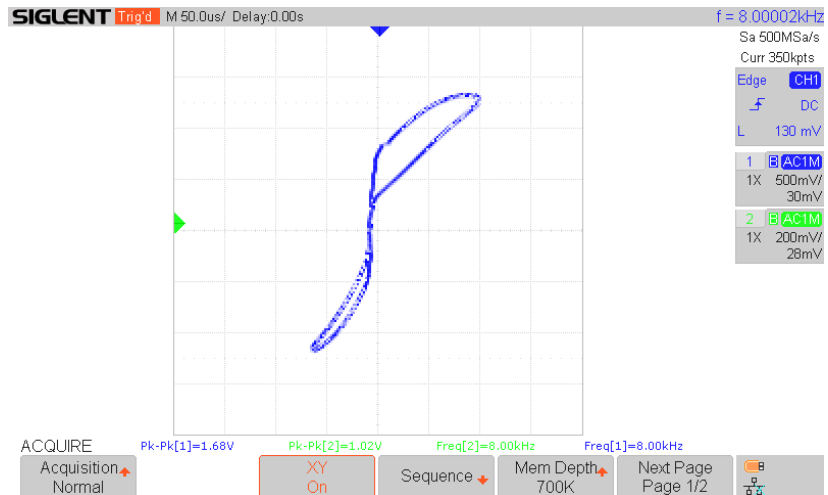


Figure 43. Measured PHL (8 KHz).

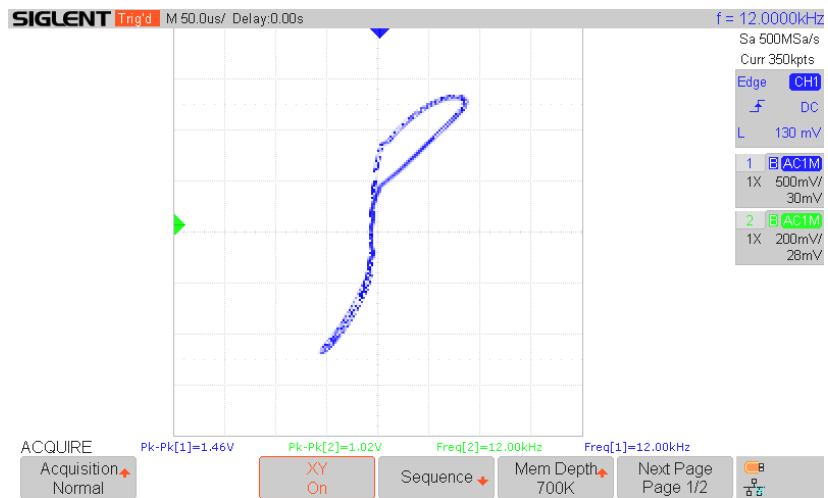


Figure 44. Measured PHL (12 KHz).

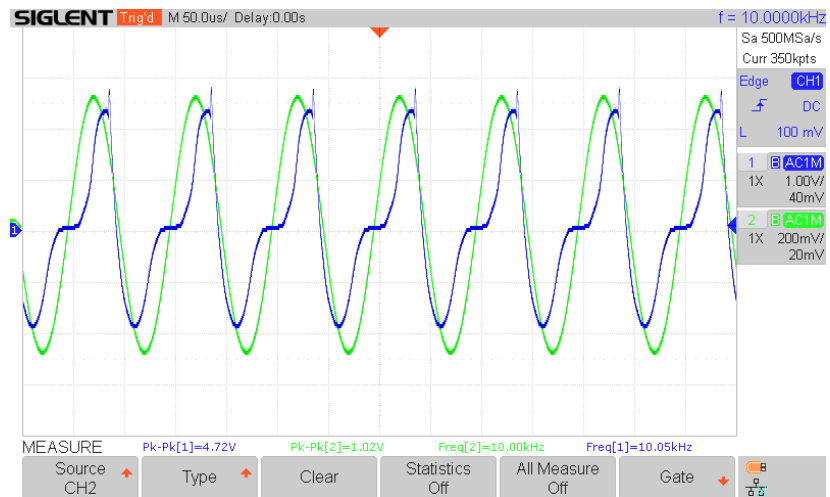


Figure 45. Measured waveforms (10 KHz).

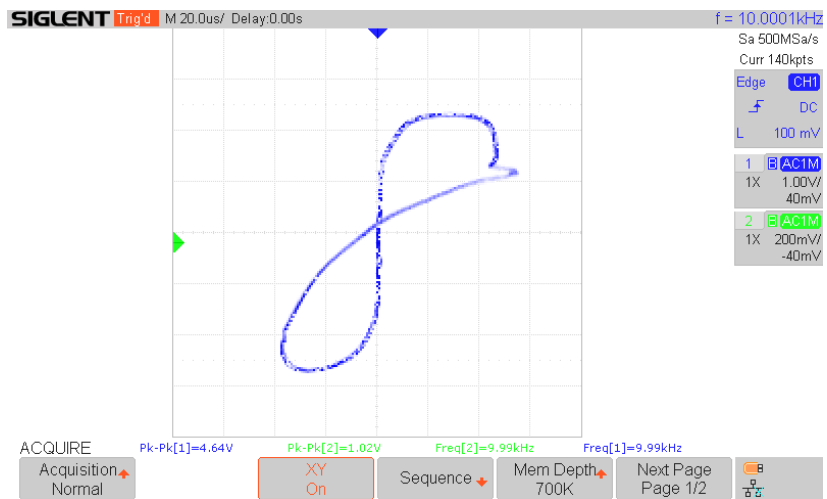


Figure 46. Measured PHL (10 KHz).

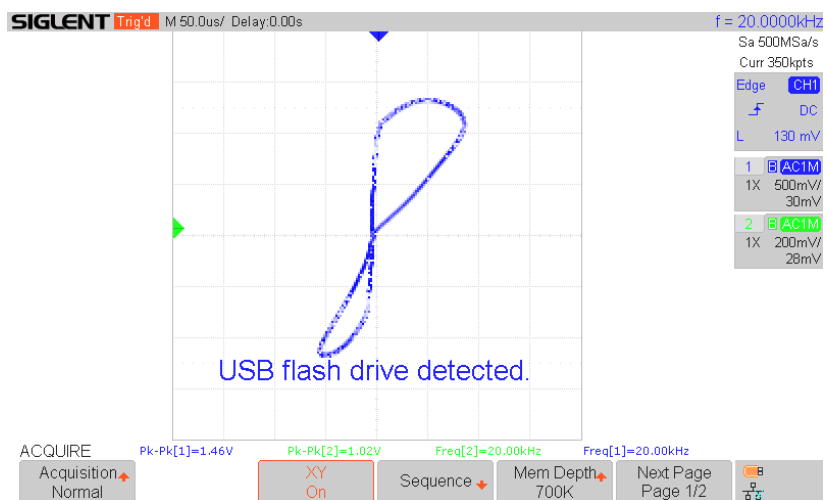


Figure 47. Measured PHL (20 KHz).

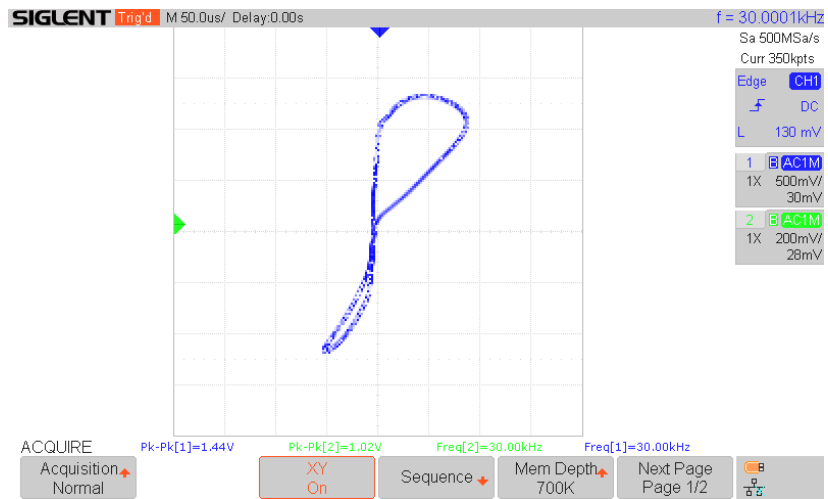


Figure 48. Measured PHL (30 KHz).

CHAPTER 6 CONCLUSION

In summary, this thesis proposed a new transistor-level high gain CA which can be used in a negative feedback configuration to realize various functions such as amplification, integration, differentiation, and buffering. This CA was used to emulate memristors, memcapacitors, and meminductors, culminating in a reconfigurable mem-element. Comprehensive simulations show the effectiveness of the proposed method and design in terms of MHz frequency operation and low power consumption in comparison with prior works. Moreover, breadboard experimental results verified the validity of the proposed design.

That being said, there are a few suggestions for future work. First, not using CMFB circuit results in an offset DC current at the output of CA. Although this offset is small, the use of integrators provides high DC gain, thus amplifying the offset. A large resistor was added to reduce the integrator's DC gain; however, this resulted in an error in the nominally 90° phase at the pole frequency. Therefore, future work can focus on finding a way to force the offset to zero through the use of CMFB or other techniques. Second, although there are established applications for memristors, applications for memcapacitors and meminductors are less explored. Third, a reconfigurable mem-element is very suitable for field programmable analog arrays (FPAAs); however, it remains to be investigated whether other applications would benefit from reconfigurability. Fourth, a scheme for controlling the reconfigurable mem-element can be studied.

References

- [1] L. Chua, "Memristor-The missing circuit element," in *IEEE Transactions on Circuit Theory*, vol. 18, no. 5, pp. 507-519, September 1971, doi: 10.1109/TCT.1971.1083337.
- [2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008, doi: 10.1038/nature06932.
- [3] Q. Xia and J. J. Yang, "Memristive crossbar arrays for brain-inspired computing," *Nature Materials*, vol. 18, no. 4. Nature Publishing Group, pp. 309–323, Apr. 01, 2019. doi: 10.1038/s41563-019-0291-x.
- [4] Z. Wang *et al.*, "Resistive switching materials for information processing," *Nature Reviews Materials*, vol. 5, no. 3. Nature Research, pp. 173–195, Mar. 01, 2020. doi: 10.1038/s41578-019-0159-3.
- [5] P. Y. Jung, D. Panda, S. Chandrasekaran, S. Rajasekaran, and T. Y. Tseng, "Enhanced Switching Properties in TaOx Memristors Using Diffusion Limiting Layer for Synaptic Learning," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 110–115, 2020, doi: 10.1109/JEDS.2020.2966799.
- [6] F. Wu *et al.*, "Memristor Based on TiOx/Al₂O₃ Bilayer as Flexible Artificial Synapse for Neuromorphic Electronics," *IEEE Trans Electron Devices*, vol. 69, no. 1, pp. 375–379, Jan. 2022, doi: 10.1109/TED.2021.3128841.
- [7] H. Chen *et al.*, "Performance Optimization of Atomic Layer Deposited HfOx Memristor by Annealing With Back-End-of-Line Compatibility," *IEEE Electron Device Letters*, vol. 43, no. 7, pp. 1141–1144, Jul. 2022, doi: 10.1109/LED.2022.3177774.

- [8] H. Cao and F. Wang, “Spreading Operation Frequency Ranges of Memristor Emulators via a New Sine-Based Method,” *IEEE Trans Very Large Scale Integr VLSI Syst*, vol. 29, no. 4, pp. 617–630, Apr. 2021, doi: 10.1109/TVLSI.2021.3056472.
- [9] B. Muthuswamy, “Implementing memristor based chaotic circuits,” *International Journal of Bifurcation and Chaos*, vol. 20, no. 5, pp. 1335–1350, 2010, doi: 10.1142/S0218127410026514.
- [10] A. Rodríguez-Vázquez and M. Delgado-Restituto, “CMOS Design of Chaotic Oscillators Using State Variables: A Monolithic Chua’s Circuit,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 40, no. 10, pp. 596–613, 1993, doi: 10.1109/82.246161.
- [11] Q. Zhao, C. Wang, and X. Zhang, “A universal emulator for memristor, memcapacitor, and meminductor and its chaotic circuit,” *Chaos*, vol. 29, no. 1, Jan. 2019, doi: 10.1063/1.5081076.
- [12] B. Dang *et al.*, “1-HEMT-1-Memristor With Hardware Encryptor for Privacy-Preserving Image Processing,” *IEEE Electron Device Letters*, vol. 43, no. 8, pp. 1223–1226, Aug. 2022, doi: 10.1109/LED.2022.3182945.
- [13] K. Prabhu *et al.*, “CHIMERA: A 0.92-TOPS, 2.2-TOPS/W Edge AI Accelerator with 2-MByte On-Chip Foundry Resistive RAM for Efficient Training and Inference,” *IEEE J Solid-State Circuits*, vol. 57, no. 4, pp. 1013–1026, Apr. 2022, doi: 10.1109/JSSC.2022.3140753.
- [14] A. Yesil, “A new grounded memristor emulator based on MOSFET-C,” *AEU - International Journal of Electronics and Communications*, vol. 91, pp. 143–149, Jul. 2018, doi: 10.1016/j.aeue.2018.05.004.

- [15] J. Vista and A. Ranjan, "A simple floating mos-memristor for high-frequency applications," *IEEE Trans Very Large Scale Integr VLSI Syst*, vol. 27, no. 5, pp. 1186–1195, May 2019, doi: 10.1109/TVLSI.2018.2890591.
- [16] N. Raj, R. K. Ranjan, and F. Khateb, "Flux-Controlled Memristor Emulator and Its Experimental Results," *IEEE Trans Very Large Scale Integr VLSI Syst*, vol. 28, no. 4, pp. 1050–1061, Apr. 2020, doi: 10.1109/TVLSI.2020.2966292.
- [17] M. Ghosh, A. Singh, S. S. Borah, J. Vista, A. Ranjan, and S. Kumar, "MOSFET-Based Memristor for High-Frequency Signal Processing," *IEEE Trans Electron Devices*, vol. 69, no. 5, pp. 2248–2255, May 2022, doi: 10.1109/TED.2022.3160940.
- [18] A. Y. R, G. S. Satyanarayan, and G. Trivedi, "A High Frequency MOS-based Floating Charge-Controlled Memcapacitor Emulator," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Mar. 2022, doi: 10.1109/TCSII.2022.3221334.
- [19] Y. R. Ananda, N. Raj, and G. Trivedi, "A MOS-DTMOS Implementation of Floating Memristor Emulator for High-Frequency Applications," *IEEE Trans Very Large Scale Integr VLSI Syst*, vol. 31, no. 3, pp. 355–368, Mar. 2023, doi: 10.1109/TVLSI.2022.3227201.
- [20] M. Ghosh, P. Mondal, S. S. Borah, and S. Kumar, "Resistorless Memristor Emulators: Floating and Grounded Using OTA and VDBA for High-Frequency Applications," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 42, no. 3, pp. 978–986, Mar. 2023, doi: 10.1109/TCAD.2022.3189837.
- [21] S. S. Prasad, P. Kumar, and R. K. Ranjan, "Resistorless Memristor Emulator Using CFTA and Its Experimental Verification," *IEEE Access*, vol. 9, pp. 64065–64075, 2021, doi: 10.1109/ACCESS.2021.3075341.

- [22] J. Vista and A. Ranjan, “High Frequency Meminductor Emulator Employing VDTA and its Application,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 39, no. 10, pp. 2020–2028, Oct. 2020, doi: 10.1109/TCAD.2019.2950376.
- [23] P. K. Ghosh, S. Z. Riam, M. S. Ahmed, and P. Sundaravadivel, “CMOS-Based Memristor Emulator Circuits for Low-Power Edge-Computing Applications,” *Electronics (Switzerland)*, vol. 12, no. 7, Apr. 2023, doi: 10.3390/electronics12071654.
- [24] Roberts, G., and Sedra, A.: ‘All current-mode frequency selective circuits’, *Electron. Lett.*, 1989, 25, pp. 759–761
- [25] H. Alzaher, “Current follower based reconfigurable integrator/differentiator circuits with passive and active components’ reuse,” *Microelectronics J*, vol. 46, no. 2, pp. 135–142, 2015, doi: 10.1016/j.mejo.2014.12.001.
- [26] Youssef, Mohamed & Soliman, A.M.. (2005). A Novel CMOS Realization of the Differential Input Balanced Output Current Operational Amplifier and its Applications. *Analog Integr Circ S*. 44. 37-53. 10.1007/s10470-005-1613-2.
- [27] C. Sanchez-Lopez, J. Mendoza-Lopez, M. A. Carrasco-Aguilar, and C. Muniz-Montero, “A floating analog memristor emulator circuit,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 5, pp. 309–313, 2014, doi: 10.1109/TCSII.2014.2312806.

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