VLSI Layout Generation Of A Programmable CRC Chip

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Summary

VLSI layout generation of a programmable CRC chip with a CRC of 16-bits is presented. The hardware of CRC generator is specified in a hardware description language (HDL). The hardware compiler and functional level simulator of HDL are used for logic synthesis. The second stage of the compilation process generates a net list of logic gates. The net list so produced is translated to RNL compatible net list by a translator program. The layout subsystem of VPNR is used to generate the VLSI layout of the programmable CRC chip from RNL netlist. The design rules and technology files of MOSIS are used. The layout is viewed in the MAGIC layout editor and simulated by irsim at the transistor-level. The CRC chip can be used in a number of applications. These include areas such as data communications for error detection and correction, digital system testing for test pattern generation and signature analysis, and mass storage devices for parallel information transfers