

# **Design And Analysis Of A High-Speed Sense Amplifier For single-Transistor Nonvolatile Memory Cells**

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## **Summary**

Using a current-sensing scheme and novel circuit techniques, the amplifier achieves sensing speeds equal to or better than those achievable by memory arrays using two transistors per cell. Other circuit techniques were used to improve the circuit-noise immunity as well as sensitivity to critical mask misalignments including the use of output latches, dummy bit lines and decoded odd/even reference-memory-cell selection. The circuit was implemented on a 32 k EPROM memory chip using 1.5  $\mu$ m N-well CMOS process

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