Speed Optimised Array Architecture For Flash EEPROMs

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Summary

The author describes a new architecture for a split-gate flash EEPROM memory array. The new array architecture provides increased speed and less susceptibility to soft writes during read operations. A unique circuit design and operation method obviates the need for applying high erase voltage in the path between the memory array and the sense amplifier. This allows all the transistors in this speed path to be fabricated as low voltage minimum channel length devices, thereby increasing their speed of operation and consequently the speed of the memory device as a whole. The new architecture, however, requires the addition of two extra rows of nonmemory cell transistors in addition to following a strict programming sequence to guard against spurious programming of unselected cells