A Geometric-Primitives-Based Compression Scheme For Testingsystems-On-A-Chip

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Summary

The increasing complexity of systems-on-a-chip with the accompanied increase in their test data size has made the need for test data reduction imperative. In this paper we introduce a novel and very efficient lossless compression technique for testing systems-on-a-chip based on geometric shapes. The technique exploits reordering of test vectors to minimize the number of shapes needed to encode the test data. The effectiveness of the technique in achieving high compression ratio is demonstrated on the largest ISCAS85 and full-scanned versions of ISCAS89 benchmark circuits. In this paper, it is assumed that an embedded core will be used to execute the decompression algorithm and decompress the test data