

# **A Parallel Tabu Search Algorithm For VLSI Standard-Cell Placement**

Suit, S.M. Youssef, H. Barada, H.R. Al-Yamani, A.;Dept. of Comput. Eng., King Fahd Univ. of Pet.Miner., Dhahran;

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King Fahd University of Petroleum & Minerals

**<http://www.kfupm.edu.sa>**

## **Summary**

VLSI standard-cell placement is an NP-hard problem to which various heuristics have been applied. In this work, tabu search placement algorithm is parallelized on a network of workstations using PVM. The objective of the algorithm is to achieve the best possible solution in terms of interconnection length, overall area of the circuit, and critical path delay (circuit speed). Two parallelization strategies are integrated: functional decomposition strategy and multi-search threads strategy. In addition, domain decomposition strategy is implemented probabilistically. The performance of each strategy is observed and analyzed

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