Interconnect-Efficient LDPC Code Design

El-Maleh, Aiman Arkasosy, Basil Al-Andalusi, M. Adnan;King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia, aimane@ccse.kfupm.edu.sa;

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King Fahd University of Petroleum & Minerals

http://www.kfupm.edu.sa

Summary

In this paper, we present a new, hardware-oriented technique for designing Low Density Parity Check (LDPC) codes. The technique targets to achieve an interconnect-efficient architecture that reduces the area and delay of the decoder implementation while maintaining good error correction performance. With a fully parallel implementation of the LDPC decoder, the proposed design assumes a constraint on the interconnect wire length which has a direct impact on the maximum signal delay and power dissipation. Furthermore, this design approach is shown to lower interconnect routing congestion, and hence reduce the chip area and maximize chip utilization.