Bit-Level Pipelined Digit Serial GF(2m) Multiplier

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Summary

A low latency digit serial multiplier for GF(2m) that can be pipelined to the bit-level is presented in this paper. Unlike existing structures, the new multiplier does not put any restriction on the type of generator polynomial used or the digit size. Furthermore, the latency of the new multiplier is significantly less than the latency of the existing bit-level pipelined digit-serial multiplier

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