A Novel Flash Erase EEPROM Memory Cell With Reversed Poly Roles

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Summary

A novel structure for a flash EEPROM memory cell is described. The structure employs the first poly as a control gate, while the second poly is used as the floating gate. Such a reversed structure allows the floating gate to overlap both the source and drain even with a merged transistor memory cell structure. Erasing can thus be performed independently at the source junction while programming is performed at the drain junction. This allows the independent optimization of each of the two junctions to satisfy the conflicting program and erase requirements. In addition, an alternative cell structure with a third poly erase electrode is made possible by the reversed poly roles