A Systolic Algorithm For VLSI Design Of A 1/N Rate Viterbi Decoder

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Summary

A novel systolic architecture for Viterbi decoding is presented. It consists of two blocks of processors. The first contains a column of processors which perform branch metric computation and decide on the survived branches. The second consists of a matrix of simpler processors which update survived paths and provide the decoded output. The systolic algorithm is modeled in AHPL to verify functional correctness. Implementation details are discussed. It is found that the proposed systolic design compares favorably with previous implementations of Viterbi decoders in terms of speed and modularity