EFFICIENT ISLANDING DETECTION METHOD FOR INVERTER-BASED DG SYSTEM

BY

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Dedicated to my father Irshad ul Haq

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All praise is due to ALLAH and peace be upon the Prophet Muhammad صلى الله عليه وسلم and his family, his companions (may ALLAH be pleased with them) and his followers.

With respect, I would like to extend my deepest gratitude to my family because without their prayers, love, positive reception, I would not have been able to achieve my desired goal in life. I will always be thankful to them for their continuous moral and emotional support and ever-needed prayers.

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LIST OF ABBREVIATIONS

ANN	:	Artificial Neural Network
ADCH	:	Analog to Digital channel
DG	:	Distributed Generation
DMS	:	Distribution Management System
DACH	:	Digital to Analog Channel
GSL	**:**	Grid Synchronization Loop
LPF	:	Low-Pass Filter
PLL	:	Phase Locked Loop
PCC	**:**	Point of Common Coupling
PJD	:	Phase Jump Detection
PI	:	Proportional Integrator
PFL	:	Positive Feedback Loop
PSIB	:	Power System Interfacing Board
PWM	:	Pulse Width Modulation
RTI	:	Real Time Inverter
RMS	:	Root Mean Square Value

RPS	:	Real Power Shift
RSG	:	Reference Signal Generator
SCADA	:	Supervisory Control and Data Acquisition
SRF	:	Synchronous Reference Frame
U/OVP	:	Under Over Voltage Protection
U/OFP	:	Under Over Frequency Protection
VCO	:	Voltage Controlled Oscillator
VSC	:	Voltage Source Converter
VAR	:	Volt-Ampere Reactive
W	:	Watt

Nomenclature

V_{DC}	:	DC link voltage
i_q	:	q component of line current
i_d	:	d component of line current
L	:	Inductance of L_{filter}
f_o	:	Rated frequency of the system
$P_s(t)$	:	Active power coming from inverter

$Q_s(t)$	:	Reactive power coming from inverter
V_{sd}	:	d component of phase voltage
V_{sq}	:	q component of phase voltage
K_p	:	Proportional gain of PI controller
K_i	:	Integral gain of PI controller
τ_i	:	Time constant
R	:	Resistance
ΔP	:	Active power from grid
Z_g	:	Grid input impedance
V_g	:	Rated value of grid voltage
Z_L	:	Load impedance
v_{pcc}	:	Instantaneous value of voltage at PCC
Z_T	:	System impedance
f_s	:	Carrier frequency

ABSTRACT

Full Name : Usama Bin Irshad

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Integration of renewable energy sources in the distribution system is widely adopted due to the various advantages of distribution generation (DG) which include environmental friendly operation without upgrading transmission and distribution (T&D) systems, having less T&D line losses. Aside from the benefits, integration of DG exposes whole power system at risk. DG is not like the traditional generation through rotating masses so its behavior is different as compared to traditional generators, especially under fault conditions. Islanding occurs when DG is supplying power to load while the main grid is disconnected. Unintentional islanding causes safety threats to people, equipment, and power system. So, detecting islanding events will make the system more protected and reliable.

This thesis proposes self-created reactive power mismatch and modified phase locked loop to detect islanding events. One of the vital outcomes of this work is to detect islanding under the weak grid and worst load conditions. When islanding occurs, adapted phase locked loop and reactive power mismatch destabilize the system by shifting the system frequency away from nominal value. The proposed technique detects islanding based on frequency variation. This scheme is applied and tested as per IEEE- 1547 standard. The simulation results show that when islanding occurs, the frequency deviates abruptly to destabilize the system. The experimental setup is developed to investigate the

proposed technique. The experimental results match with the simulation results and both validate the efficiency of the proposed method. Results are presented and discussed in detail.

ملخص الرسالة

الاسم الكامل: أسامة بن إرشاد

عنوان الرسالة: طريقة أكثر كفاءة للكشف عن عملية تجزئة النظام لأنظمة المولد الموزع المعكوسة

التخصص: الهندسة الكهربائية

تاريخ الدرجة العلمية : رَبيع الثاني/ 1438

إن دمج مصاد الطاقة المتجددة كجزأ من شبكات التوزيع الكهربية انتشر على نطاق واسع وذلك للعديد من المزايا التى يتمتع بها التوليد الموزع حيث أنها صديقة للبيئة و لاتحتاج إلى تطوير فى نظم النقل و التوزيع كما أن مفاقيد خطوط النقل و التوزيع أقل. من جهة أخرى فإن التوزيع الموزع يعرض نظام القوى بأكمله للخطر حيث أنها مختلفة عن طرق التوليد التقليدية المعتمدة على الحركة الدورانية. لذلك فإن أداها مختلف مقارنة بالمولدات الكهربية التقليدية و خاصة فى ظروف الأعطال. إن العزل يطبق حين يتم تغذية الأحمال من التوليد الموزع فقط و يتم فصل شبكة القوى الرئيسية. هذا العزل قد يؤدى - بدون قصد-لأخطار و يهدد سلامة البشر و المعدات و نظم القوى. لذلك فإن اكتشاف واقعة العزل سيزيد من وقاية و اعتمادية النظام.

هذه الأطروحة تقدم طريقة لإكتشاف واقعة العزل عن طريق استحداث عدم تطابق للطاقة الراجعة و phase locked loop معدلة. من أهم نتائج هذا العمل هو اكتشاف العزل تحت ظروف ضعف شبكة القوى و أسوأ حالات التحميل. فعند حدوث العزل فإن الحل المقترح يخل بإتزان النظام بتحويل تردد النظام بعيد عن القيمة الاعتبارية. و بالتالى الطريقة المقترحة تكتشف العزل عن طريق التغير الحادث فى التردد. تم نطبيق و اختبار هذه الطريقة وفقا لمعايير IEEE-1547. تظهر نتائج المحاكاة أنه عند حدوث العزل يتغير التردد بشكل حاد و يخل باتزان النظام. كما تم تطوير نموذج معملى لاختبار الطريقة المقترحة. وقد تطابقت الاختبارات المعملية مع المحاكاة بما يؤيد صحة و كفاءة الطريقة المقترحة. و من خلال هذه الأطروحة فقد تم عرض و مناقشة هذه النتائج بالتفصيل.

Chapter 1

INTRODUCTION

1.1 Smart grid

The "smart grid" is a next-generation electrical power system that is characterized by the use of communications in the generation, distribution, and utilization of electrical energy. The smart grid allows bidirectional communication between the customers and utility. Like the internet, the smart grid consists of controls, automation, and integration of renewable energy sources like solar and wind. These technologies integrate into the electrical grid to meet electric load demand.

The smart grid changes the energy industry into a new era of reliability, availability, and efficiency. During the transition period, it will be critical to carrying out testing, technology enhancements, consumer education, improvement of standards and regulations. The advantages of the smart grid include:

- More efficient and reliable system.
- Fast recovery of the system when a fault occurs.
- Reduction in operational and structural costs.
- Increased integration of renewable resources.

- Improved system protection and security.

Conventional power distribution systems are passive networks, where electrical energy at the distribution level is always supplied to the customer from upstream power resources that are connected to the bulk transmission system. The concept of smart grid is introduced to exploit the benefits of small local renewable generation. Besides these benefits, integration of renewable energy sources creates several issues. Some technical problems are defined as:

1. Power Quality
    a. Harmonics in the system
    b. Voltage variation (sag and swell in voltage)
    c. Frequency variation
2. Power fluctuation
    a. Transient power fluctuations
    b. Seasonal fluctuations in power
3. Storage
4. Islanding
5. Power system protection
6. Optimal placement of RES

In this thesis, islanding has been addressed in detail. Islanding occurs when DG is supplying power to load while the main utility grid is disconnected [1],[2]. Islanding can be either intentional or unintentional. The aim of intentional islanding is to build a power "island" when system faces some disturbances such as faults. However, the active part of the distribution system should detect the disconnection from main grid and shuts down

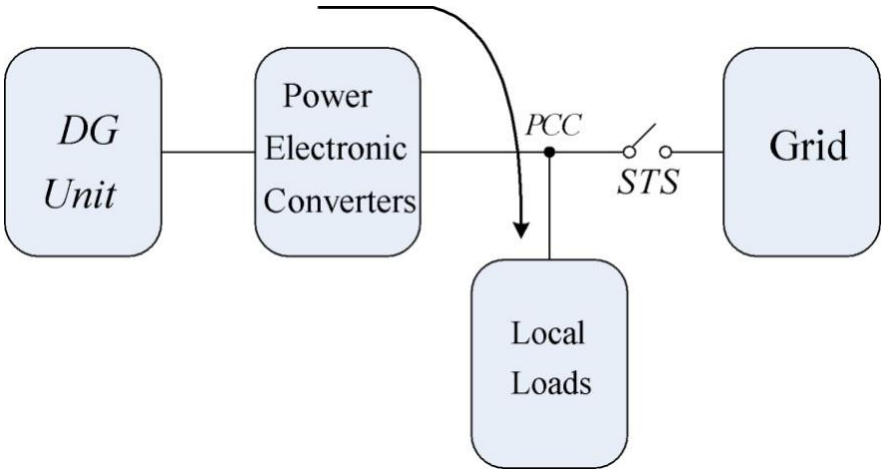

Figure 1-1: Islanding mode operation of DG system

DGs in areas where island mode operation is not allowed [3]. The unintentional islanding causes numerous issues in terms of power quality, voltage and frequency stability, safety, and interference [4],[5]. The IEEE 1547.2-2008 standard specifies that unintentional islanding condition has to be detected within a maximum delay of 2s [6], [7]. UL 1741 standard specifies the disconnection of DG system when unintentional islanding occurs [3]. Therefore, finding effective solutions to resolve this problem is necessary.

1.2 Thesis motivation

Significant developments in renewable energy and advancement in power electronics increase the penetration level of distributed generation in power systems. Integration of renewable energy sources increases the power generation capacity and brings a considerable change in topology of how electric power is generated, transmitted and distributed. Power electronics has revolutionized the power sector as DG units can be installed near to local loads. Application of multiple DGs in the distribution system is becoming common practice with the integration of DG resources. This practice is widely adopted due to the various

advantages of DG which include environmental friendly operation without upgrading transmission and distribution (T&D) systems and low T&D line losses [4],[8]. However, numerous problems should be tackled before the DG units are installed to the networks. These problems include frequency and voltage stabilizations, intermittency of the renewable resources, and power quality issues.

Sometimes intentionally or unintentionally, utility gets disconnected and form a microgrid while the microgrid remains electrically energized due to the presence of renewable energy sources. Islanded system is shown in Figure 1-1. If DGs are not capable of meeting the load, then voltage and current variations are measured which can easily detect that utility is disconnected or islanding is occured. But if DG is capable to meet load demand when the utility is disconnected then it is difficult to quantify major variation in voltage and current, hence detecting islanding becomes difficult and more challenging. Several attempts have been done to detect islanding but non-detection zone (NDZ) remains and that needs to be reduced. The region where islanding detection techniques are not working is designated as NDZ. Detection of islanding is important because it is a great hazard to utility line workers and customer's equipment if the voltage and frequency provided by the DG are not properly regulated. Therefore, an efficient islanding detection technique needs to be developed to address the aforementioned problem.

1.3 Thesis objectives

The aim of this thesis work is to develop a technique that detects islanding events and to ensure the stability and reliability of the power systems. The objectives of this thesis are:

1. To develop a fast and accurate method that can detect islanding event and has negligible non-detection zone (NDZ).
2. To design test bed to investigate the developed technique with worst loading conditions.
3. To analyze the proposed method of islanding detection under stiff and weak grid conditions.
4. To develop experimental setup in order to validate the theoretical results.

1.4 Thesis contribution

The main contribution of this work is to develop a novel efficient islanding detection technique. This work proposes a self-created reactive power mismatch and modified phase locked loop to detect islanding. A positive feedback loop is introduced in PLL. When islanding occurs, the positive feedback loop drifts the frequency away from its nominal value. Artificial neural network (ANN) based controller is implemented in PLL that helps PLL to quickly reach its steady state and detects islanding within a fraction of a millisecond. Self-created reactive power mismatch based on voltage variation is proposed to detect an islanding when the system has a resistive load. Hardware setup is developed to analyze the frequency behavior of the system after islanding. The summary of contributions of this thesis are listed below:

1. Development of a new and efficient method that can detect islanding conditions.
2. Development of artificial neural network based PLL.
3. Designing a test system on MATLAB Simulink.
4. Hardware implementation to validate the theoretical findings.

5. Development of laboratory prototype to investigate the developed technique in worst loading conditions.

1.5 Thesis breakdown

The organization of the thesis is as following. In Chapter 1, an introduction of this work is explained which includes the motivation behind working on this topic, the problem statement, an outline of objectives and the contributions. In Chapter 2, a literature review is discussed. A detail discussion on active and passive islanding detection techniques is presented. In Chapter 3, grid synchronization controller is discussed. Independent control of active and reactive power between grid and DG system is described. The active and reactive power reference tracking of the developed controller is also elaborated. The proposed technique for islanding detection and ANN based modified PLL is discussed in Chapter 4. The experimental setup where the detailed discussion on each component used in laboratory prototype is also discussed in Chapter 4. In Chapter 5, simulation results of controller testing, power sharing between grid and DG system and islanding detection are discussed. In Chapter 6, conclusion and future directions are highlighted.

Chapter 2

LITERATURE SURVEY

The demand of electric power is predicted to rise significantly in the near future. Having foreseen this challenge, advancement in the technology for efficient and environment-friendly power generation has attained a great deal of interest in the recent years. Hence renewable energy sources and micro-grids are rapidly populating the modern power generation network. But the integration of DGs creates issues like stability, reliability and power quality. The technological advancement of these renewable energy sources has been investigated with a lot of interest. The work proposed here is on a specific topic in the domain of distributed generation, which is to protect the system by detection islanding conditions.

The research on unintentional islanding detection is rapidly growing to ensure that power system is operated under the standard requirements [9]. Depending on anti-islanding methods, many relays like under/over current or voltage relay, under/over frequency relay are used to protect the system [4]. Numerous methods have been used to detect islanding events. It can be classified into central (remote) and local methods as shown in Figure 2.1. In this chapter, the details of these methods are explained and evaluated.

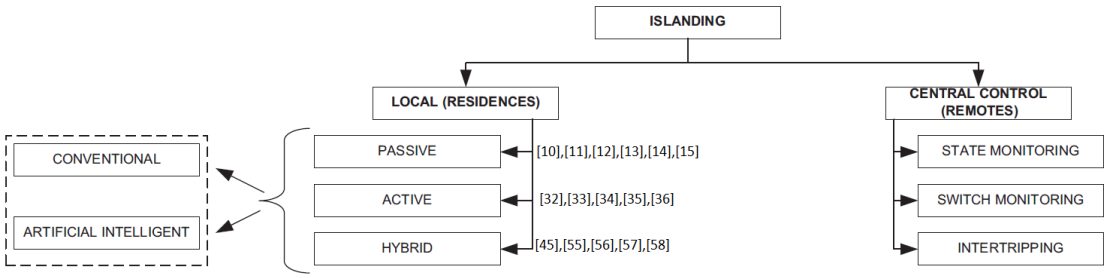

Figure 2-1 Islanding detection methods

2.1 Central (remote) techniques

Central control methods are not influenced by the number of inverters, system size, generator type and penetration level. The central methods are communication-based methods, therefore, the implementation of central methods is very costly [10]. A tight connection between utility and DG units is needed in applying communication techniques. Table 2.1 shows the summary of central techniques for islanding detection. Some remote techniques like system state monitoring, switch state monitoring and inter-tripping are described below.

2.1.1 System state monitoring

System state monitoring is a method for determining system states from a model of the power system network with a reduced number of state measurements. This method is generally regarded as a function of the Distribution Management System (DMS), which is a complementary of SCADA systems. The method is used to detect unintentional islanding by monitoring the parameters of the distribution system like frequency and voltage [11]. The islanding event can be detected if the system parameter can be detected from the disconnected area. This method is highly effective in detecting unintentional islanding if

the system is properly equipped with measuring instruments. However, the implementation cost is very high. The voltage sensitive devices embedded in the PV-based DG inverter are connected to SCADA system Monitoring of voltage for each generator in the distribution grid can be an expensive and difficult process with a huge number of DGs.

2.1.2 Switch state monitoring

The SCADA system can be used to measure the status of the circuit breakers (CB) and reclosers that could island a power system. However, this method requires an improved communication between the DG units and utility, which leads to extra costs. Transfer trip detection schemes require all the CB that island the DG to be monitored and directly linked to the DG control, or through a central substation SCADA system. When an islanding is detected, the islanded area is determined by transfer trip signal and sends a signal to the DGs to remain in or discontinue operation [10]. The transfer trip scheme is incorporated with SCADA to sense the status of circuit breakers and reclosers. The scheme allows for the additional control of DGs through the utility and increases the coordination between the DGs and utility. However, the method has a complexity cost because of the growth of the system complexity

2.1.3 Inter-tripping

Another method that can be used for islanding detection is inter-tripping, which is theoretically different from central control techniques. Inter-tripping also generally relies on the communication between the sensors and generating units. This method sense the opening and closing on contact and send a signal to all generators that are supplying power to the islanded zone [10].

The above central techniques are used because of their reliability. The review shows that central control techniques are preferable because these techniques can avoid non-detection zones (NDZ), where the DG is capable of meeting demand under islanding. Central control methods are also not influenced by the number of inverters, the size of system, type of generator, and penetration level. However, a tight connection between utility and DG units is needed in applying communication techniques.

Table 2-1: Remote islanding detection techniques.

Methods	Advantages	Disadvantages	Improvements
SCADA system	Communicate with all DG	Cost implementation high	Computationally expensive
Transfer trip scheme	• Simple concept • Avoid NDZ	• Expensive • Complicated	Direct transfer trip can avoid islanding
Wired cable or non-wired	Easy to implement	Cost concern for DG below 2 MW	Needs any possible media to transfer the signals

2.2 Local islanding detection techniques

Local islanding detection techniques measure system parameters to detect islanding like voltage, frequency, current, and harmonic distortion. It can be further classifying these techniques into passive, active, and hybrid techniques. Local islanding detection methods are further classified into passive and active methods. A literature overview of local islanding techniques was conducted and discussed in detail.

2.2.1 Passive techniques

Passive techniques monitor the parameters of the system such as voltage, frequency, harmonic distortion, and current at the PCC with the utility grid. These parameters fluctuate when the islanding occurs. The parameters typically used to detect islanding conditions are frequency and voltage [12],[13],[14],[15],[16]. Various traditional passive islanding detection techniques can be summarized as shown in Figure 2-2.

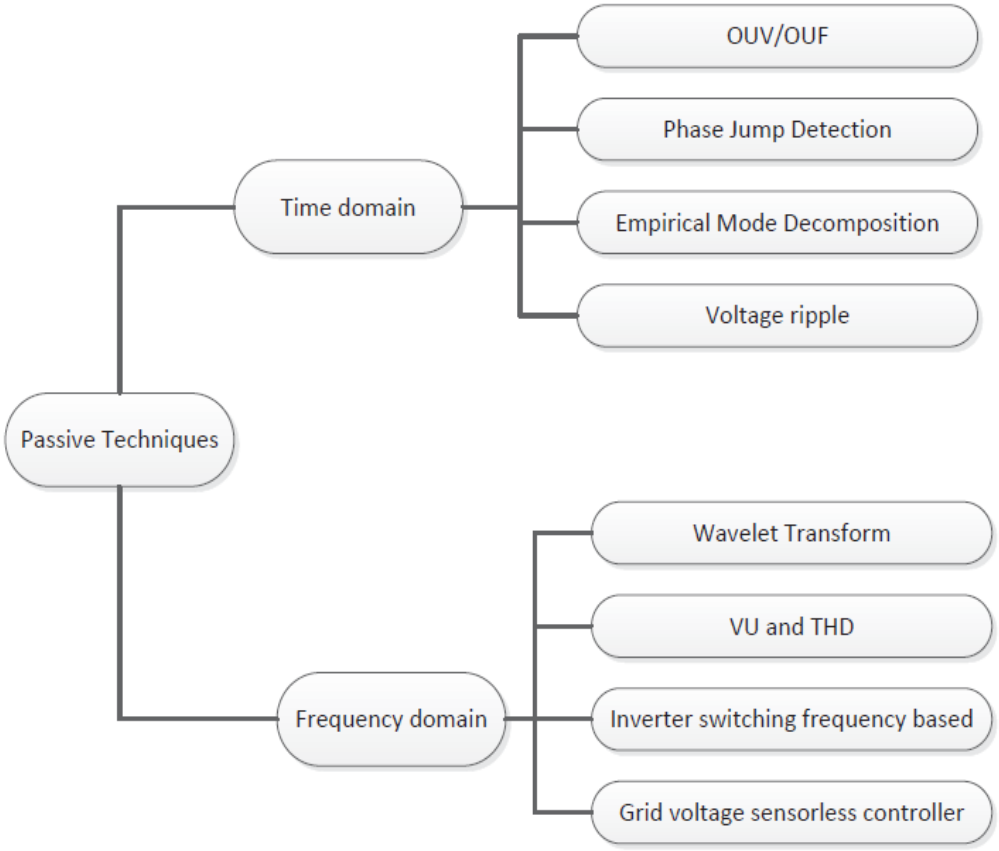

Figure 2-2 Passive islanding detection technique [90]

2.2.2 Under/over voltage and under/over frequency

The Over/under frequency protection (OFP/UFP) [17] and over/under voltage protection (OVP/UVP) [18],[19],[20] are the oldest techniques adapted to protect the distribution system. The protection relays for this technique are placed on a distribution feeder to determine the various types of abnormal conditions. This technique is usually used for grid connected photovoltaic inverters. These protection methods considered to be based on the power flow at PCC between the photovoltaic inverters and grid, which refers to the active power (P) and reactive power (Q). The drawback of the UVP/OVP and UFP/OFP is the large NDZ [21]. Therefore, some improvement was made to overcome the large NDZ components. A method is introduced to decrease the NDZ of UVP/OVP and UFP/OFP by comparing the P–V and P–Q of the controlled constant current inverters [22]. The islanding detection based on the performance of the interface control, which is an additional parameter, was implemented in parallel to the UVP/OVP and UFP/OFP to reduce the NDZ. Another new passive technique based on the rate of change of voltage phase angle is introduced to detect islanding condition and have negligible NDZ [23].

2.2.3 Voltage phase jump and voltage drifting detection

In phase jump detection (PJD) the phase difference between the terminal voltage and current is monitored for a sudden jump. The PJD technique searches for a sudden variation in phase angle. This method is easy to implement because only modifying the PLL is required. The ability to neutralize the inverter is only required when the phase errors exceed the threshold. This method does not affect power quality. However, PJD is unsuitable in detecting islanding for all the operating conditions of the load [24]. The drawback of the

PJD leads to a failure in detecting the islanding condition when the power generated by DG is matched with load requirement.

Voltage drifting technique depends on the change of active power of DG. Therefore, active power reference (P_{ref}) is defined as a piecewise linear function of voltage. It is designed to reduce the voltage at PCC that eventually decreases the active power of DG when islanding occurs. Therefore voltage drifting method is used when DG operate at its peak power [25].

2.2.4 Harmonics measurement

This method measures the variation of the total harmonic distortion (THD) at the PCC. The DG will be disconnected if THD exceeds a certain threshold. Two monitoring parameters, namely, voltage unbalanced and the THD of current, are also proposed to detect the islanding operation of DG. However, this method is facing difficulty to detect islanding conditions because of the high Q factor $\left(\text{where } Q = R\sqrt{C/L}\right)$ and the threshold selection problem [12].

2.2.5 Voltage unbalance

The voltage unbalance (VU) generally varies because of the changes of the load and the network despite the small changes in the DG loading [26]. Therefore, effectively detecting the islanding operation is possible if the unbalance of the three-phase voltage of the distributed generation is continuously monitored. Special identification was conducted to monitor the VU variation from the steady state and normal loading conditions. Therefore, each step is compared with the VU identification values and any abrupt VU is identified as

islanding [27]. The one-cycle average of the voltage unbalanced and voltage unbalanced variation, was checked at every 1/4 cycle (4.17 ms).

The most of the preferences in choosing passive islanding detection are the cost and simplicity of implementation. Passive techniques are effective in many cases. However, the major drawback of passive techniques is the large NDZ, which fails to detect the islanding condition. The summary of passive islanding detection techniques is shown in Table 2.2.

Table 2-2: Comparison of passive islanding techniques

Method	Implementation speed	Weakness	Improvement
UVP/OVP [28]	Easy but detection time is variable	Large NDZ	Compared with P-V and P-Q, for constant current controlled inverters
UFP/OFP [29],[30]			
PJD [31]	Complex in implementation	Failed to detect islanding when DG generates power equal to load demand.	Controlled by using a PLL
THD [32],[33]	Easy but hard to choose threshold	Failed to detect islanded in high-quality load	Need artificial intelligent classifier
Voltage unbalance	Easy but need large power mismatch	Not applicable to signal phase system	Combine UV and THD of current and voltage magnitude variation

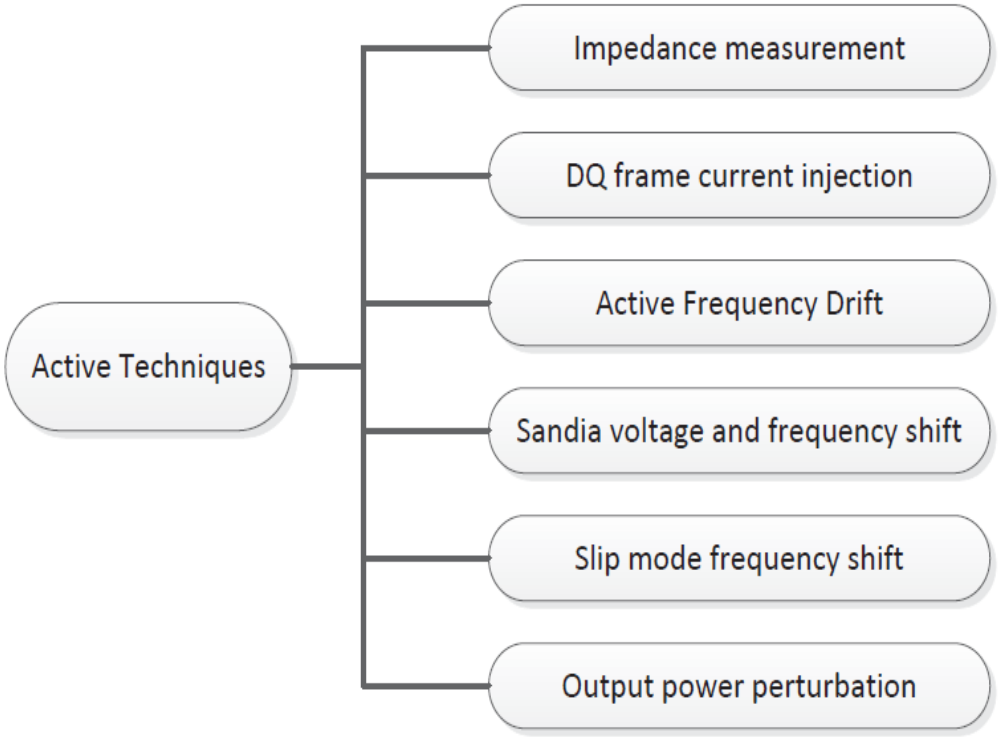

Figure 2-3 Active islanding detection technique [90]

2.3 Active techniques

Recently active techniques have been applied by introducing disturbance into the grids. These disturbances vary the system parameters when islanding occurs [34][35]. Various active islanding detection techniques are described in Figure 2-3. The active frequency drift [5],[36],[37],[38] slip mode frequency shift [39],[40] and Sandia frequency shift [41] are three commonly used active techniques for islanding detection. Comparison of active islanding detection techniques is shown in Table 2.3. Some active techniques are described and discussed in detail below.

2.3.1 Impedance measurement

The impedance-based method measures the magnitude of the set of frequency-dependent reference impedances and measures the impedance at the PCC to detect islanding event

[42]. In active method, shut inductor is momentarily coupled with the supply voltage shortly, and the short circuit current and supply voltage drop are used to measure source impedance. Based on the value of impedance the islanding condition is detected. Many impedance detection methods have recently been proposed because of the impedance method has less NDZ. The experiment reveals that the impedance detection method based on islanding detection do not have a NDZ in the single inverter systems [42].

2.3.2 Slip-mode frequency shift (SMS)

Slip mode frequency shift [39],[40],[43] methods use positive feedback for islanding detection. The combination of SMS with Q-f is an active technique that forces the DG frequency to the unstable region when islanding occurs [44]. SMS is also efficient in islanding detection (lesser NDZ) compared with other active techniques. SMS also introduces a phase shift perturbation, which can lead to noise, measurement inaccuracy, and quantization error in practice. This limitation can be answered by introducing an additional phase shift called the improved-SMS (IM-SMS) [45].The IM-SMS was verified through digital simulation and experimentation, which results in simplicity, easy implementation, and high reliability.

2.3.3 Active frequency drift (AFD)

The active frequency drift [5],[36],[37],[38] (AFD) method is forcing variation in the output of inverter by introducing positive feedback to accelerate inverter current frequency. The AFD uses the waveform of the inverter current, which is inserted into PCC [11],[12],[46]. The advantage of AFD is the ease of implementation in microcontroller based inverters. All inverters must have identical AFD or else would fail to detect islanding

conditions in the multiple inverter cases [12]. AFD is also effective for purely resistive loads [47]. However, problems occur in islanding detection such as the supposition of the unity power factor operation of PV inverters, which fails in the frequency-shift method [48]. The RMS value and Fourier series coefficients of current are used to improve the conventional AFD. However, the method can be further improved using AFD with positive feedback [49].

2.3.4 Sandia frequency shift (SFS).

The Sandia frequency shift [41] (SFS) method uses positive feedback for islanding detection. SFS is implemented in combination with Sandia Voltage Shift (SVS) - based islanding detection. This combination is extremely effective [12]. However, SFS creates issues in power quality and stability such as the drawback of AFD which is the power quality issue caused by the discontinuous waveform. It can be overcome using the SFS anti-islanding algorithm [50].

Table 2-3: Comparison of active islanding detection technique

Method	Implementation Speed	Weakness	NDZ
Impedance measurement [51]	Easy and fast	Cannot detect islanding in multi-inverter system.	Large for high-Q load
SMS [52]	Slow	Cannot detect islanding when load is resonant RLC	Large for high-Q load

AFD [53],[54]	Easy and medium	Create power quality	Large for high-Q load
SFS [55], [56]	Fast but difficult	Create power quality and stability	Large for high-Q load

2.4 Hybrid techniques

The hybrid technique is a combination of the active and passive techniques. Some hybrid techniques are briefly discussed.

2.4.1 Voltage unbalance and frequency set point

This method uses positive feedback, harmonic distortion and voltage unbalance (VU) techniques, where the drawback of both techniques are canceled out when simultaneously applied [57]. The calculation of the VU for each of the DG is used instead of the THD because the VU is more sensitive to disturbance than THD. Therefore, any disturbance applied to DGs could produce a spike in the VU. The technique also efficiently discriminates between islanding condition and local switching.

2.4.2 Method based on voltage and real power shift

It uses a rate of the voltage change and a real power shift to answer the limitations of the active and passive techniques in islanding detection [47]. The technique can detect the islanding condition with large DG units working at a unity power factor. However, the active power shift (APS) is applied to the system if the passive technique cannot perfectly detect the islanding condition. APS can eliminate the injecting perturbation from time to time to detect islanding similar to other active techniques [47]. However, APS only can vary the

active power of the DG at the unity power factor. In the proposed method, only one DG changes the real power compared with the positive feedback technique, where all the DGs collectively inject disturbances in the system [47].

2.4.3 Voltage fluctuation injection (VFI)

This technique uses voltage fluctuation injection, that can be obtained using a high impedance load [58]. Islanding detection correlation factor (CF) is proposed for small-scale DGs, typically less than 1 kW. The two-stage method, which is the passive technique for the protection scheme, and the active technique uses CF as a backup to attain higher effectiveness. This technique uses digital signal processing to calculate the rate of change of frequency (ROCOF), the rate of change of voltage (ROCOV), and CF of the distribution synchronous generator and to accurately decide between islanding and non-islanding disturbances [58].

2.4.4 Signal processing methods

The signal processing (SP) methods present various features, such as time-frequency distribution (TFD) of a time series, which eases the analysis and quantification of the signals regardless of the succeeding classification technique. The linear TFD techniques are popularly implemented in determining the islanding condition because such implementation is faster than those of non-linear methods. The comparison of some signal processing techniques are shown in Table 2.4. The following sections describe some of the SP tools used in islanding detection.

2.4.5 Wavelet-transform (WT)

The wavelet theory is the mathematical model for non-stationary signals with a set of components in the form of small waves called wavelets. WT can be either continuous (CWT) or discrete wavelet (DWT). CWT is applied using an online measuring technique for the voltage in DG units. The Procrustes algorithm was used in extracting the noise in the signals to eliminate the noise and to prevent islanding [59]. The technique creates numerous coefficients to reduce the computational efficiency of the algorithms, which allows us to focus more on using the DWT technique instead of the CWT technique.

A WT-based approach to monitor voltage and frequency variations, where the Daubechies wavelet served as the basis [60]. Some of the useful features in this method are the improvement in the islanding detection capability of protection relay, the simultaneous observation of information, and the simplicity to programming. The wavelet packet transform (WPT) based on voltage signal at PCC is introduced in [61]. The method is based on the (ROCOP) from the output power of DG. The method introduced a new index called the node rate of change of the power (NROCOPI), which is used to quantify the change of the power at each WPT sub-band. Daubechies of order 10 served as a basis of WPT, which had a smaller number of wavelet coefficient compared with others without affecting the accuracy of the results.

In [62], [63] the wavelet was applied to detect the islanding condition of wind turbines. The method used DWT with Daubechies db5 to detect islanding. All signal processing methods for islanding detection are computationally expensive and takes long time to detect islanding conditions.

Table 2-4: Comparison of signal processing islanding detection technique

SP method	Parameter	Key indicator	Islanding detection (time)
CWT (Wavelet) [64]	Voltage, Current, Power	Modulus local maxima	0.6 s (ROCF)
DWT (Wavelet) [65]	Voltage, Current, Power	Multi resolution analysis	Less than 2 s (45 ms)
DWT (Wavelet) [66]	Voltage, Current, Signal	d1 Coefficients	Less than 0.5 s
DWT (Wavelet)	Spectral change of PCC voltage	Energy value of second level wavelet	2.5 power frequency cycles
DWT (Wavelet) [67]	Voltage	Fifth decomposition level	Less than 0.2 s

2.5 Intelligent classifiers

The information generated by any type of signal processing method can be used to identify the characteristics of the island mode operation. In this section, the use of intelligent classifiers combined with signal processing techniques are investigated

2.5.1 Artificial neural network (ANN)

The ANN is a computational structure model of a biological process that attempts to implement the mathematical model instead of using a biological brain neural network in which the brain contains all the useful information and the data memory [68]. ANN is

widely used in numerous areas, including in islanding detection [68]. The ANN is usually used with a signal processing technique such as WT. In a related work, a hybrid technique was approached using ANNs in detecting the islanding condition of mini hydro distribution system [68]. The ANNs were combined with WT to identify the islanding condition. The approach detects islanding conditions with a high degree of accuracy and high quality factor of load performance. This technique is also suitable for multiple DG applications [69]. The DWT was used to extract the feature from current signals. The signal was then extracted using a correlation coefficient and was validated using ANN. Only one signal was analyzed, and only one of the ANN input is used to detect the islanding condition [70].

2.5.2 Probabilistic neural network (PNN)

It is based on a Bayesian classifier technique which is used in pattern recognition applications. PNNs contain 4 layers, which are the input layer, pattern layer, summation layer and output layer [71]. A PNN does not require a learning process. The WT integrated based technique was proposed for fault detection in [72]. The combination uses the multi-resolution analysis (MRA) of the DWT and the Parseval′s theorem. It uses to extract distribution features at dissimilar resolution level. The features were then classified using PNN. In [73], PNN was used to detect islanding and monitoring health of DC side of PV system. The wavelet analysis was used as an input of the PNN, and the output was the class of fault location. The PNN is a very precise way of classifying the location of the fault. PNN with various parameters were derived at a target DG location to detect the islanding condition [74].

2.5.3 Decision trees (DT)

Another classification technique used for islanding detection is the decision tree (DT). In [75] DT was trained, and the online performance of DT was evaluated in a controlled islanding strategy. This splitting criterion is a difficult task and can affect DT technique for classification problems. Splitting criterion is a statistical approach used in conditional interface tree. In [76], DT with DWT was used for islanding detection. DWT is used to classify the features from the transient voltage and current signals, where the DT was used to recognize the islanding condition. However, this technique was modified and applied in hardware as presented in [77]. A hybrid technique was proposed in which DT is combined with the frequency positive feedback and with a voltage of the DG can detect islanding with almost zero NDZ [78]. The C4.5 DT was introduced for islanding detection in a DG system by Lin and Dong [79]. The C4.5 is an algorithm and used to build decision tree by using training data. The main advantage of C4.5 DT is the minimization of the NDZ, the ability to operate under various operations, and the different network topology. However, the result from the C4.5 DT was not always the best result because the technique can be improved with other optimization methods such as the pruning method of DT. In [75], the technique obtained the threshold setting by selecting a new set of parameters, such as voltage, current, active and reactive power, power factor, and frequency. However, the system information of phasor measurement unit (PMU) measurements was used with DT classifier in [80]. DT was used to detect abnormal system operation behaviors related to islanding possibility. Some paper compared several classification techniques such as DT and neural network [81] to identify the best classification accuracy in detecting the

islanding condition, where the DT is said to be the best classification technique than neural network.

All islanding detection techniques have some drawbacks. The drawback of passive techniques is the large NDZ, which fails to detect the islanding condition. The local load affects the determination of the islanding detection. For active technique, the main limitation is the perturbation in the system. The detection time for the islanding detection is slow because extra time is needed for the system to response to the perturbation. Signal processing techniques need large computation time and memory to process the signal.

A novel islanding detection is proposed. The proposed technique mitigates all the limitations and drawbacks of previous techniques. The proposed islanding technique has negligible non-detection zone, and can detect islanding conditions within fraction of milliseconds. Proposed technique does not affect power quality of the system and detects islanding in all cases.

Chapter 3

SYSTEM DESCRIPTION AND CONTROLLER IMPLEMENTATION

In this chapter the details regarding the implementation of the current controller are discussed. One of the platforms used for this is MATLAB/SIMULINK, which is used for implementing and testing of developed controller. The self-created reactive power mismatch is discussed in detail.

Due to the advancement in power electronics, the penetration of renewable sources is increased. Renewable energy sources like wind and the solar system need an efficient and robust controller to integrate them with existing grid. The increase in penetration of renewable sources helps in meeting load demand. Figure 3-1 shows the overview of the grid-connected distributed generation system. The renewable energy sources (wind, solar and fuel cell) are connected to the utility. The power conversion unit is not like traditional generation unit, it requires control system to convert the power generated from renewable sources and feeds it to the existing grid. The controller is categorized into two groups, 1) grid side controller and 2) input side (DC-link) controller. This work focuses on developing grid side control. The developed controller is 1) independently controlling the active and reactive power between grid and DG system, 2) synchronizing the renewable sources with

the utility, 3) stabilizing the voltage at the PCC. The detailed description of the system and the developed active and reactive power controller is described in Figure 3-2.

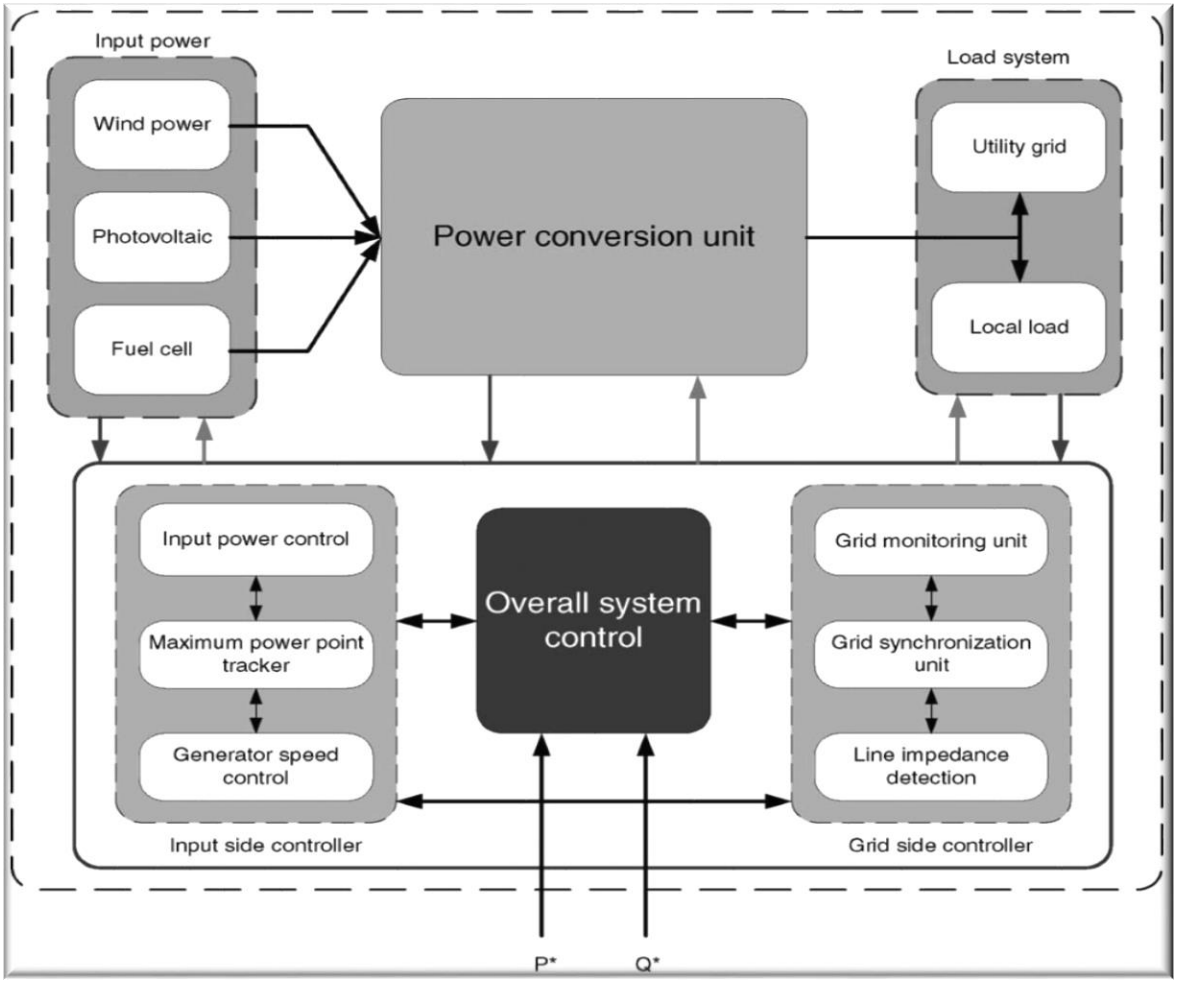

Figure 3-1 Overall DG topology [91]

3.1 System description

Power system needs to be more flexible and reliable. Applications of modern control and communication systems and power electronics have led to the smart grid concept. Increasing penetration of renewable energies with the existing grid opens an area to develop novel control strategies to overcome the power quality issues. Power electronics

is used to convert conventional power systems into smart grid since they allow controlling the power flow between grid and distributed generation systems. AC-DC converters with bi-directional power capability are the key elements in distributed generation systems. Wind turbines and photovoltaic systems need AC-DC inverter to insert power into the existing grid. The schematic diagram of grid connected voltage source converter (VSC) is shown in Figure 3-2.

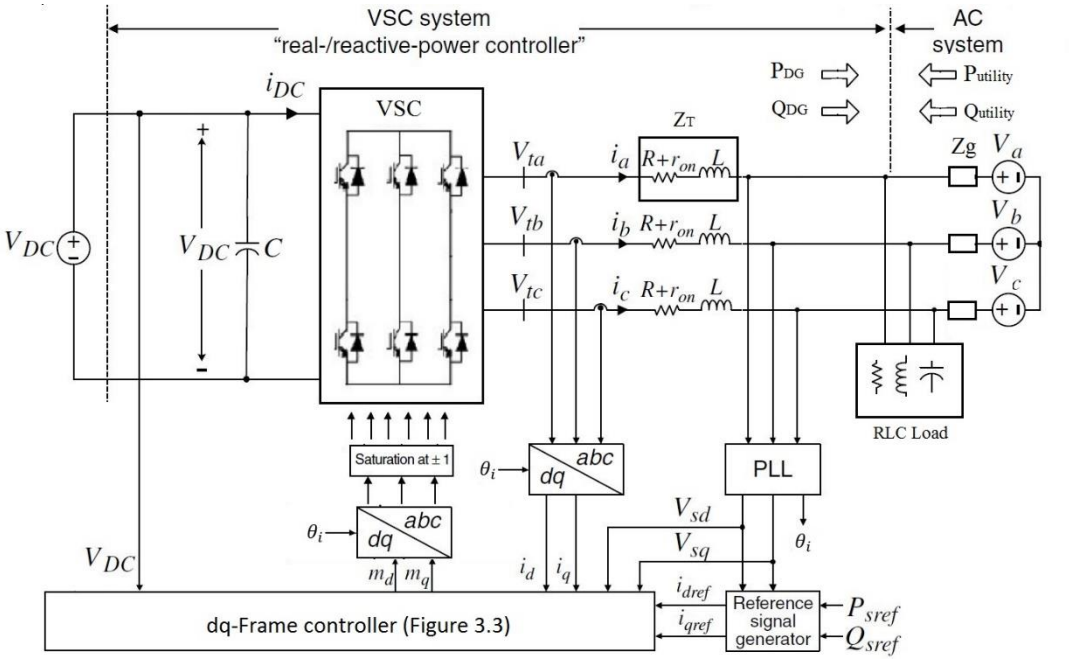

Figure 3-2 Schematic diagram of three-phase grid connected system [83]

The resistance Z_T at AC side of VSC represents the conductance power loss. The DC side of VSC is considered as a constant DC source. VSC is connected with AC system through series resistance $R + r_{on}$ and inductance L. V_{abc} is considered as a three-phase balanced grid voltage. The inductor is connected at PCC and it is tuned to give smooth current waveform. i_{abc} is the line current of the system. Z_g is the grid input impedance. dq components of current and voltage are i_d, i_q, V_{sd} and V_{sq} respectively. Phase angle and line current amplitude control the active and reactive power respectively.

The dynamic model of active and reactive power controller is mathematically described in equations (3-1) and (3-2). Here state variables are i_q, i_d whereas V_{td}, V_{tq} and ω are the control variables.

$$L\frac{di_d}{dt} = \left(L\frac{d\rho}{dt}\right) i_q - (R + r_{on})i_d - \widehat{V_s}\cos(\omega_0 t + \theta_0 - \rho) + V_{td} \quad (3\text{-}1)$$

$$L\frac{di_q}{dt} = \left(L\frac{d\rho}{dt}\right) i_d - (R + r_{on})i_q - \widehat{V_s}\sin(\omega_0 t + \theta_0 - \rho) + V_{tq} \quad (3\text{-}2)$$

Here $\omega = d\rho/dt$. In equations (3-1) and (3-2) $\cos(\omega_0 t + \theta_0 - \rho)$ and $\sin(\omega_0 t + \theta_0 - \rho)$ make the equations non-linear. Now by assuming the initial conditions where $\rho = 0$, $\omega_0(t) = 0$ and $\rho(t) = \omega_0 t + \theta_0$, equations (3-1) and (3-2) will become

$$L\frac{di_d}{dt} = L\omega_0 i_q - (R + r_{on})i_d + V_{td} - \widehat{V_s} \quad (3\text{-}3)$$

$$L\frac{di_q}{dt} = L\omega_0 i_d - (R + r_{on})i_q + V_{tq} \quad (3\text{-}4)$$

In the above equations, the input is $\widehat{V_s}$. This work focuses on developing the control strategy to independently control the flow of active and reactive power between grid and DG system.

3.2 Current controller

Two control modes are used to control the active and reactive power of the system. These are 1) current mode control (CMC) and 2) voltage mode control (VMC). In CMC, active power is controlled by phase angle and reactive power is controlled by line current amplitude of VSC with respect to PCC voltage. The line current is precisely monitored and controlled by the current control loop. In VMC, active power and reactive powers are

controlled by phase angle and voltage amplitude of VSC respectively. The VSC is protected against overcurrent conditions due to the current regulation in CMC. The advantages of CMC are 1) dynamic performance, 2) robustness against variations in parameters of the system and 3) higher control precision [82].

The CMS is used in this work, and the dq components of line current i_d and i_q control the real and reactive power respectively. The voltage and current signals are converted in dq-frame and processed by compensator to produce the output control signals. After transformation from dq-frame to abc-frame, the control signals are fed to PWM generator. Finally, the pulses are fed to the inverter. Active power and reactive power are exchanged between utility and DG system. Active and reactive power at PCC are described below [83]

$$P_s(t) = \frac{3}{2}\left(V_{sd}(t)i_d(t) + V_{sq}(t)i_q(t)\right) \tag{3-5}$$

$$Q_s(t) = \frac{3}{2}\left(- V_{sd}(t)i_q(t) + V_{sq}(t)i_d(t)\right) \tag{3-6}$$

In equations (3-5) and (3-6), V_{sq} becomes zero due to PLL. So, the equations (3-5) and (3-6) are reduced into

$$P_s(t) = \frac{3}{2}V_{sd}(t)i_d(t) \tag{3-7}$$

$$Q_s(t) = -\frac{3}{2}V_{sd}(t)i_q(t) \tag{3-8}$$

Figure 3-3 illustrates the current control scheme in dq-frame. Real and reactive power are controlled by i_d and i_q respectively. e_d and e_q are the error signals. u_d and u_q are output

of PI controller. V_{DC} is the voltage across DC link capacitor. Active and reactive power references in term of i_{dref} and i_{qref} are shown in equation (3-9) and (3-10).

$$i_{dref}(t) = \frac{2}{3V_{sd}} P_{sref}(t) \tag{3-9}$$

$$i_{qref}(t) = -\frac{2}{3V_{sd}} Q_{sref}(t) \tag{3-10}$$

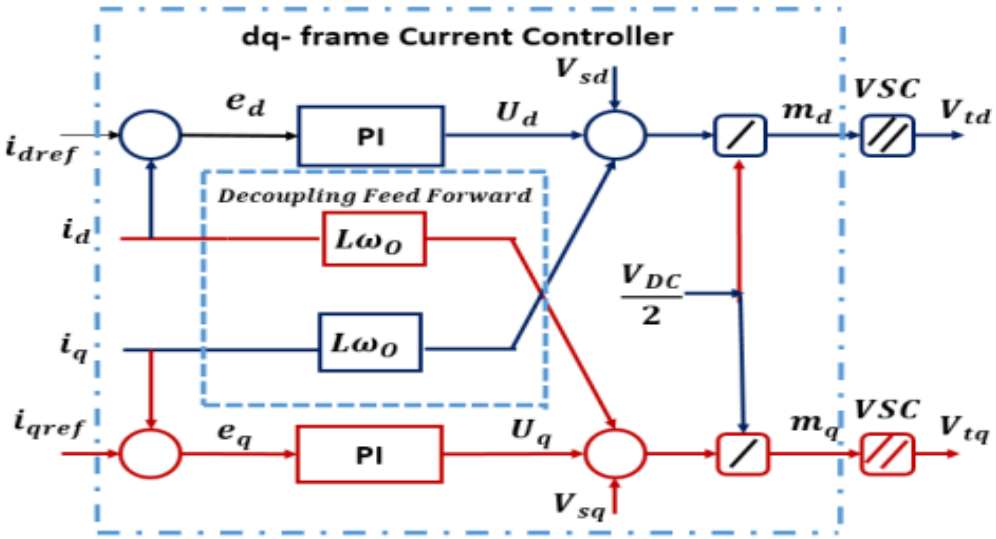

Figure 3-3 dq-frame current controller [91]

Equations (3-11) and (3-12) are derived from equations (3-7) to (3-10). The dynamic model of the AC system is described in equations (3-11) and (3-12). [83].

$$L\frac{di_d}{dt} = V_{td} - V_{sd} + L\omega_O i_q - (R + r_{on})i_d \tag{3-11}$$

$$L\frac{di_q}{dt} = V_{tq} - V_{sq} - L\omega_O i_d - (R + r_{on})i_q \tag{3-12}$$

In equations (3-11) and (3-12) V_{td} and V_{tq} are mathematically described as

$$V_{td}(t) = \frac{V_{DC}}{2} m_d(t) \tag{3-13}$$

$$V_{tq}(t) = \frac{V_{DC}}{2} m_q(t) \tag{3.14}$$

In equations (3-11) and (3-12), the state variables are i_d and i_q, and the control inputs are V_{td} and V_{tq} and the disturbances in the system are represented by V_{sd} and V_{sq}. The terms i_d and i_q are coupled due to the existence of $L\omega_O$. To decouple the dynamics, the decoupling feed forward terms m_d and m_q are introduced. The decoupling terms can be defined as follows [83].

$$m_d = \frac{2}{V_{DC}}\left(u_d - L\omega_O i_q + V_{sd}\right) \tag{3-15}$$

$$m_q = \frac{2}{V_{DC}}\left(u_q + L\omega_O i_d + V_{sq}\right) \tag{3-16}$$

The gain of PI controller can be determined by using equation (3-17) and (3-18). Here τ_i is the time constant. Its value depends on system requirement. It ranges from 0.5 to 5 ms.

$$K_p = {}^{L}/_{\tau_i} \tag{3-17}$$

$$K_i = {}^{(R + r_{on})}/_{\tau_i} \tag{3-18}$$

3.3 Proposed self-created reactive power mismatch

Self-created reactive power mismatch is proposed to detect islanding condition. In proposed algorithm, based on voltage variations, reactive power changes its reference point. The change in reference of reactive power with respect to the change in voltage is described in this section. Both grid and DG are backing up the voltage at PCC. The active and reactive power consumed by the load are described in equations (3-19) and (3-20).

$$P_L = P_{DG} + P_{Utility} = 3V_{PCC}^2 \frac{1}{R} \tag{3-19}$$

$$Q_L = Q_{DG} + Q_{Utility} = 3V_{PCC}^2 \left(\frac{1}{2\pi f_o L} - 2\pi f_o C\right) \quad (3\text{-}20)$$

f_o and V_{pcc} are the nominal frequency and voltage respectively. L, R, C are inductive, resistive, and capacitive component of the load respectively. P_L and Q_L are the active and reactive power consumed by the load. P_{DG} and Q_{DG} are the active and reactive power supplied by the distributed generation respectively. Active and reactive powers coming from grid are denoted as $P_{Utility}$ and $Q_{Utility}$ respectively. After islanding, active power mismatch (ΔP) causes the voltage to deviate from its nominal value. The reactive power mismatch (ΔQ) variates the frequency of the system. ΔP and ΔQ are described in equation (3-21) and (3-22) [84].

$$\Delta P = P_{utility} = P_{DG}\left(\frac{1}{(1+{}^{\Delta V}/_{V_{pcc}})^2} - 1\right) \quad (3\text{-}21)$$

$$\Delta Q = \frac{3V_{PCC}^2}{2\pi f_o L}\left(1 - \frac{f_o^2}{(f_o+\Delta f_o)^2}\right) \quad (3\text{-}22)$$

In the proposed method, the change in voltage at PCC and frequency variations are used for islanding detection. The voltage variation due to active power mismatch also changes the consumption of load reactive power, thus creating the reactive power mismatch between the DG and the local load [85] . By using equations (3-19) – (3-22) the relationship between active power and reactive power mismatch with system frequency are described in (3-23) and (3-24) [84].

$$\Delta P = \frac{P_{DG}}{f_O}\left[1 + \left(\frac{f_O}{\Delta f_o}\right) + \left(\frac{\Delta C}{C}\right)\right] \Delta f_o \quad (3\text{-}23)$$

$$\Delta Q = -\frac{Q_{DG}}{f_O}\left[1 + \left(\frac{f_O}{\Delta f_o}\right) + \left(\frac{\Delta C}{C}\right)\right] \Delta f_o \quad (3\text{-}24)$$

Where Δf_o is the change in frequency after islanding. V_{pcc} is the instantaneous value of voltage at PCC. Equations (3-23) and (3-24) shows that both active power mismatch (ΔP) and reactive power mismatch (ΔQ) deviate the frequency during islanding. It is observed that variation in frequency due to reactive power mismatch is more significant as compared to the variation in frequency due to active power mismatch [85]. Therefore, based on voltage variations, this work introduces self-created reactive power mismatch to detect islanding condition for resistive load. The reactive power control strategy allows the DG to absorb or inject extra reactive power into the system to create artificial reactive power mismatch. V_N is the rated phase voltage of the system. Equations (3-25) and (3-26) set the new reactive power reference based on the change in voltage at PCC. If the voltage at PCC is greater than 1.01*V_N, it means DG is suppling active power more than load consumption. In this case the reactive power reference is set by using equation (3-25).

$$Q_{ref1} = -|V_L|^2 * \left(\frac{f_o - f_{min}}{f_0}\right) + Q_{Load} \tag{3-25}$$

Here V_L is the line to line voltage at PCC and f_{min} is the minimum allowable threshold value of the frequency. Here its value is 59.4 Hz. If voltage at PCC is less than $0.98 * V_N$, new Q_{ref} is set by using equation (3-26).

$$Q_{ref2} = -|V_L|^2 * \left(\frac{f_o - f_{max}}{f_0}\right) + Q_{Load} \tag{3-26}$$

f_{max} is the maximum allowable frequency. Here f_{max} is 60.5 Hz. Equation (3-25) and (3-26) change the reactive power reference of the controller in such a way that the frequency will deviate when islanding occurs. This will help in detecting the islanding condition specifically for resistive load or load having resonance frequency of f_o.

$$Q_{sref} = \begin{cases} Q_{ref1} & V_{PCC} > 1.01V_N \\ Q_{ref2} & V_{PCC} < 0.98\,V_N \\ Q_{load} & 0.98V_N < V_{PCC} < 1.02V_N \end{cases} \quad (3\text{-}27)$$

Reference signal generator is shown in Figure 3-2. It generates reactive power reference by using equation (3-27). With the help of current controller, $P(t)$ and $Q(t)$ are controlled independently. It also helps in synchronization of DG system with the existing grid.

Chapter 4

PROPOSED ISLANDING DETECTION ALGORITHM AND PHASE LOCKED LOOP DESIGN

4.1 Grid synchronization techniques

Numerous synchronization techniques have been developed to measure the phase angle of the grid voltage. Among them, the most common techniques are zero crossing detection and a phase-locked loop (PLL). Zero crossing detection is the simplest technique to detect phase angle but this method has some drawback such as low dynamics. Furthermore, noise and higher order harmonics in the utility grid affect its output. The latest synchronization technique for measuring the phase angle of the grid voltage is the PLL. The PLL can measure the phase angle of the grid voltage even in the presence of harmonics and noise.

4.2 Phase locked loop:

The phase locked loop (PLL) consists of the phase detector, a loop filter and voltage controlled oscillator [86] as shown in Figure 4-1. The phase detector acts as a comparator. It compares the input signal of PLL (i.e. grid voltage) with the output of PLL and generates a voltage proportional to the phase difference between output and input signals. In PLL the control signal is the voltage of the system. The dynamic characteristics of PLL are

determined by its low-pass filter (LPF). The LPF specifies the capture range (bandwidth) and tracking range of PLL.

The output signal of phase detection is filtered by LPF and fed it to voltage controlled oscillator (VCO). VCO sets the noise margin and tuning range and generates oscillations. The output of VCO is fed back to the phase detector for comparison. The loop continues to work until phase error between the output signal of VCO and the reference signal becomes zero, which means that the phase is being locked, or the phase of input signal exactly matches with the VCO output.

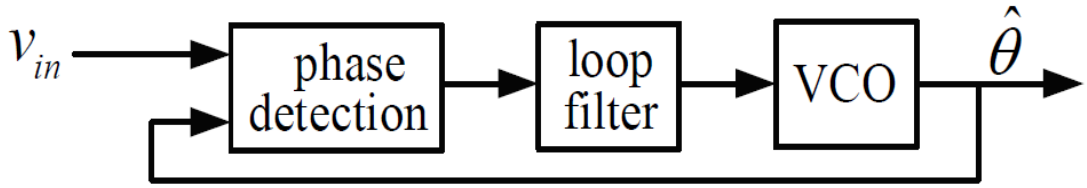

Figure 4-1 Close loop synchronization structure

The PLL locked the phase of the output signal to its input signal. With the help of PLL the system frequency and phase angle can be determined easily which helps in grid synchronization.

4.3 Proposed PLL

In literature, the difference in PLL is based on the different techniques of phase detection. Figure 4-2 shows the graphical representation of $\alpha\beta$ / dq transformation. In Figure 4-3, synchronous reference frame based PLL uses the abc / dq transformation block as a phase detector that converts the voltage signal to d and q channel signals.

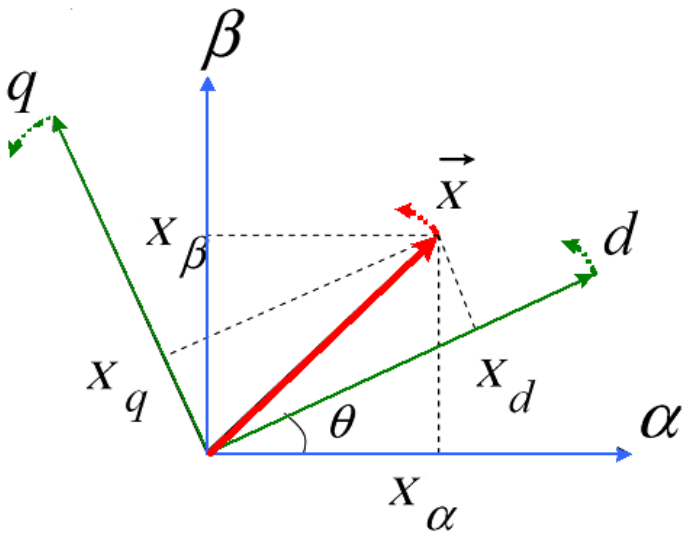

Figure 4-2 Park transformation

$$V_{dqo} = TV_{abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

In [87], PLL is employed to address the nonlinear behavior of system assuming a lossless system and neglecting the effect of impedance between VSC and grid. In this work modified PLL is proposed. The proposed PLL is modeled by considering the effect of impedance, reactive component and losses in the system.

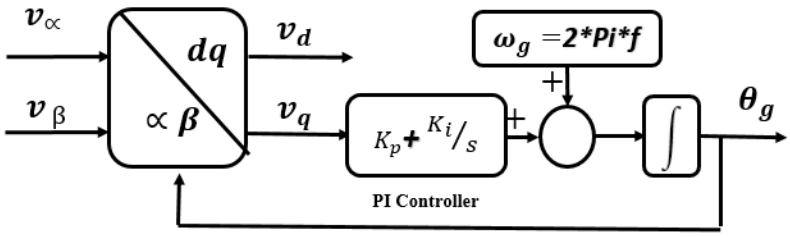

Figure 4-3 SRF phase locked loop

4.4 Mathematical modeling of proposed PLL

VSC is coupled with a grid via three phase current smoothing inductors and delivers the constant power at PCC. Z_g represents the grid input impedance, V_g is the grid voltage.

In Figure 4-4, the VSC is modeled as current source and grid is modeled as a voltage source, both sources are delivering power to the load Z_L and maintaining voltage at PCC.

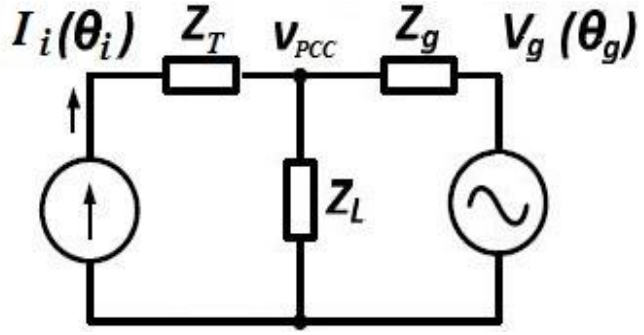

Figure 4-4 Single line diagram of test system

Z_T is the impedance between VSC and grid which represents the losses of the system. As shown in Figure 4.4, both sources are supporting the voltage at PCC. V_{PCC} is controlled by two independent sources and by using superposition principle V_{PCC} can be derived as

$$\widetilde{v_{pcc}} = \frac{Z_T.Z_L}{Z_TZ_L + Z_TZ_{g+}Z_L.Z_g} \cdot \widetilde{V_g} + \frac{Z_L\,Z_g}{Z_L + Z_g + Z_T.Z_L + Z_TZ_g} \cdot \widetilde{I_i}$$

$$\widetilde{v_{pcc}} = \left|\frac{Z_T.Z_L}{Z_TZ_L + Z_TZ_{g+}Z_L.Z_g}\right| V_g e^{j(\theta_g+\varphi_g)} + \left|\frac{Z_L\,Z_g}{Z_L + Z_g + Z_T.Z_L + Z_TZ_g}\right| I_i e^{j(\theta_i+\varphi_i)}$$

$$\widetilde{v_{pcc}} = K_g.V_g e^{j(\theta_g+\varphi_g)} + K_i.I_i\, e^{j(\theta_i+\varphi_i)} \quad (4\text{-}1)$$

Here

$$\varphi_g = phase\left(\frac{Z_T.Z_L}{Z_TZ_L + Z_TZ_{g+}Z_L.Z_g}\right),$$

$$\varphi_i = phase\left(\frac{Z_L\,Z_g}{Z_L + Z_g + Z_T.Z_L + Z_TZ_g}\right)$$

In equation (4-1) K_g and K_i are the loop gains of grid synchronization loop and positive feedback loop respectively [87], θ_g and θ_i are the phase angles and φ_g and φ_i are the phase angle shift due to the existence of reactive components in Z_g, Z_T and Z_L. Equation (4-1) shows that reactive component affects the system [88]. Artificial neural network (ANN) is implemented to detect the islanding and phase angle of grid voltage. It takes less computational time than PI and brings PLL to steady state much faster as compared to PI controller. By using ANN, PLL works efficiently under nonlinear conditions and detects islanding event within fraction of milliseconds. Levenberg-Marquardt back propagation method is used for training purpose. A three-layer feed-forward network with sigmoid

hidden neurons and linear output neurons are used to map the input to an output. The phase error is the input signal of ANN controller. Parameters of ANN are shown in Table 4.1.

Table 4-1: ANN parameters

Description	Parameters
ANN structure	Feed forward
No. of hidden neurones	10
Training Method	Backpropagation
Training Function	Levenberg-Marquardt
Activation function	Sigmoid

The PLL have two loops, the first is grid synchronization loop (GSL) and the second is positive feedback loop (PFL). Both loops are mathematically described in equations (4-2) and (4-3) respectively. The PFL is the perturbation loop that drifts the equilibrium point of PLL away from zero. The Proposed PLL is shown in Figure 4.5.

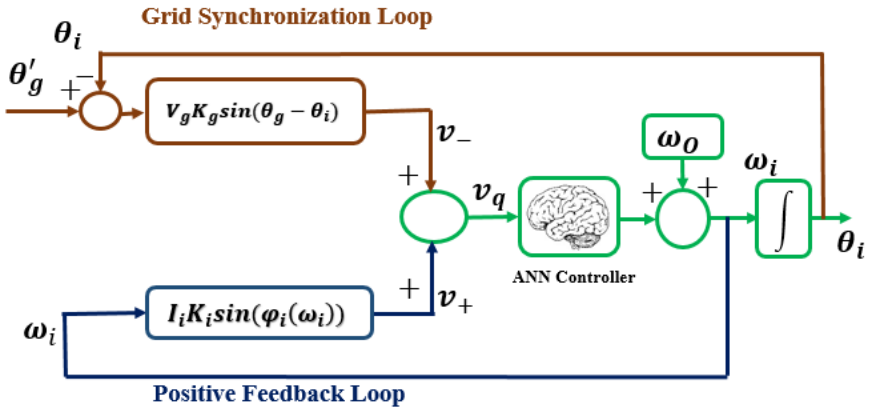

Figure 4-5 Proposed phase locked Loop

$$v_- = V_g . K_g . sin(\theta_g - \theta_i) \tag{4-2}$$

$$v_+ = I_i . K_i . \sin\left(\varphi_i(\omega_i)\right) \tag{4-3}$$

$$v_q = v_- + v_+ \tag{4-4}$$

So, the steady state point of PLL is changing continuously due to disturbance. v_q is the phase error signal that is fed to the ANN controller. In equation (4-3) I_i, K_i and φ_i shows that the perturbation will be increased due to 1) higher injection current, 2) weak grid conditions ($Z_g \approx \infty$) and 3) higher reactive component of load and system. The stability criteria of PLL is given in equation (4-5).

$$|v_-| > |v_+| \tag{4-5}$$

The output of PLL will be stable when the perturbation (v_+) is less than v_-. So, PLL will work fine when injection current and reactive component are low, and grid input impedance is equal to zero. In equations (4-6) and (4-7), K_g and K_i are described as

$$K_g = \left| \frac{Z_T . Z_L}{Z_T Z_L + Z_T Z_g + Z_L . Z_g} \right| \tag{4-6}$$

$$K_i = \left| \frac{Z_L \, Z_g}{Z_L + Z_g + Z_T . Z_L + Z_T Z_g} \right| \tag{4-7}$$

Under normal condition when $Z_g \approx 0$, the positive feedback loop disappears and only grid synchronization loop appears. It means that, in normal conditions the perturbation disappears and the PLL easily tracks the phase angle. The PLL under stiff grid condition ($Z_g \approx 0$) is described in Figure 4.6. In Figure 4.6, θ_g is the angle of the grid voltage and θ'_g is the shifted angle of grid voltage, the phase angle of V_g is shifted due to the reactive components in the system.

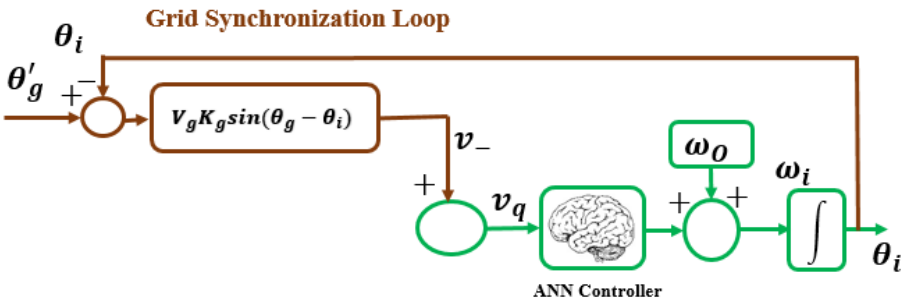

Figure 4-6 PLL under normal condition

$$\theta'_g = \theta_g + \angle \left(\frac{Z_T . (\omega_i) Z_L (\omega_g)}{Z_T . (\omega_i) Z_L (\omega_g) + Z_T . (\omega_i) Z_g (\omega_g) + Z_L (\omega_g) Z_g (\omega_g)} \right) \tag{4-8}$$

Equation (4-8) shows that reactive component in the system affects the phase angle of the grid voltage. Figure 4.7 described that under weak grid conditions when $Z_g \approx \infty$, the grid synchronization loop disappears and the system only left with positive feedback loop. The PFL drifts the frequency away from nominal value to detect islanding condition.

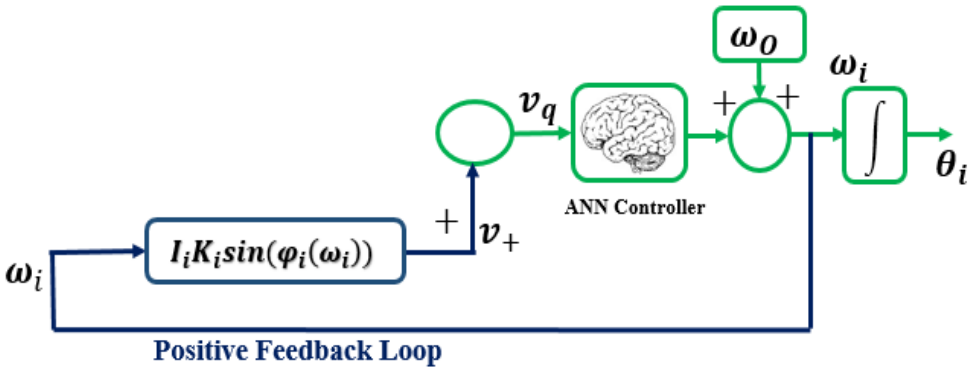

Figure 4-7 PLL under islanding mode

In equation (4-9), φ_i is defined as a function of grid impedance Z_g, system impedance Z_T and load impedance Z_L.

$$\varphi_i(\omega_i) = \angle\left(\frac{Z_L(\omega_i)}{Z_L(\omega_i)+Z_g(\omega_i)+Z_T(\omega_i)Z_L(\omega_i)+Z_T(\omega_i)Z_g(\omega_i)}\right) \quad (4\text{-}9)$$

$\varphi_i(\omega_i)$ is effected by the reactive components in the system. In weak grid conditions, $\varphi_i(\omega_i)$ determines the sign of PLL i.e. for capacitive load $\varphi_i(\omega_i) < 0$ and positive feedback loop tends the frequency towards infinity while $\varphi_i(\omega_i) > 0$ for inductive load and the positive feedback loop drifts the frequency towards zero. However, $\varphi_i(\omega_i) = 0$ for resistive load hence the frequency remains same to nominal value. Under normal condition, (when $Z_g \approx 0$) PLL is stable and follows the nominal frequency of 60 Hz.

In stiff grid condition (when $Z_g \approx 0$), $K_g = 1$, $K_i = 0$, and $\varphi_i(\omega_i) = 0$. Due to $K_i = 0$ the PFL disappears. Under islanding condition (when $Z_g \approx \infty$) , $K_g = 0$, $K_i = |Z_T + Z_L|$, and $\varphi_i(\omega_i) = Phase\,(Z_T(\omega_i) + Z_L(\omega_i))$.

MATLAB Simulink model of proposed PLL is shown in Figure 4.8. Two loops are shown in Figure 4.8. The first loop is grid synchronization loop and the second loop is a

positive feedback loop. PLL gives phase angle and frequency as output signals. The phase angle is fed back to grid synchronization loop whereas ω is fed to PFL.

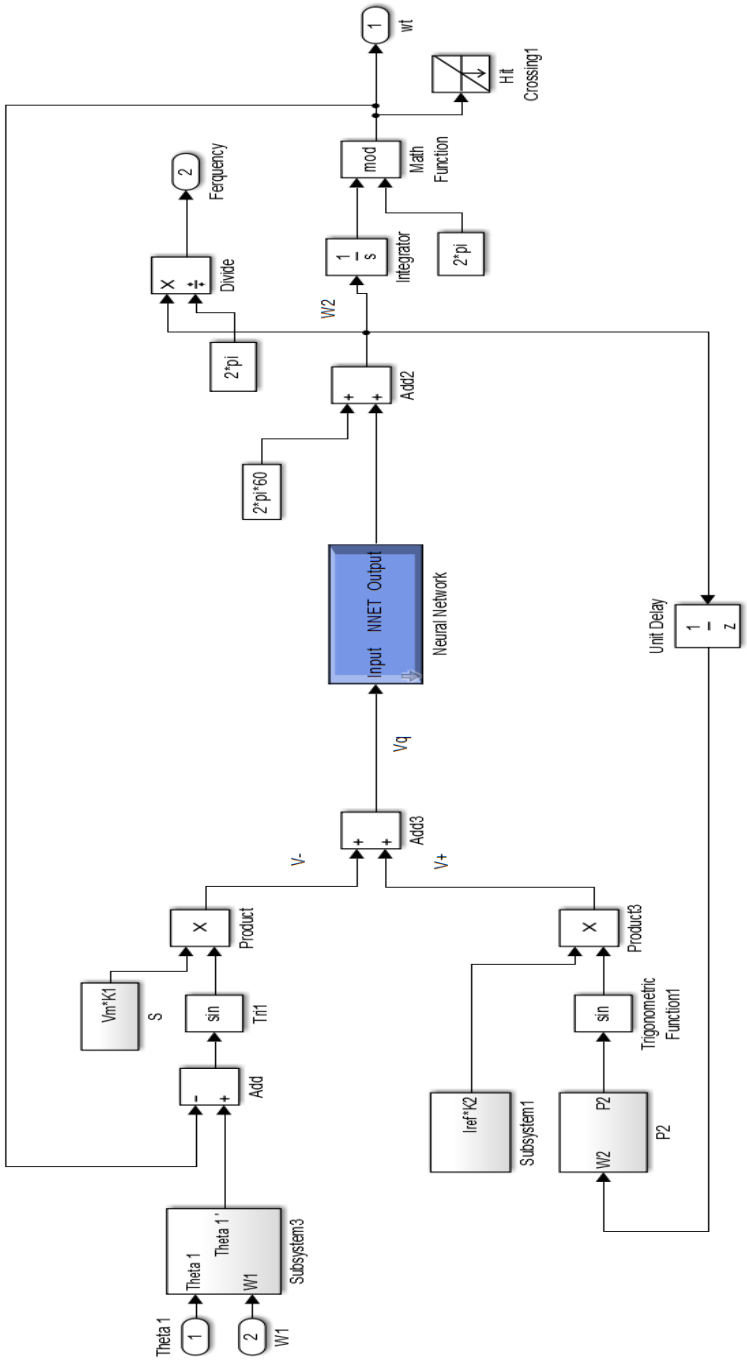

Figure 4-8 MATLAB/Simulink model of proposed PLL

4.5 Islanding detection algorithm

The graphical representation of the proposed algorithm for islanding detection is presented in Figure 4.9.

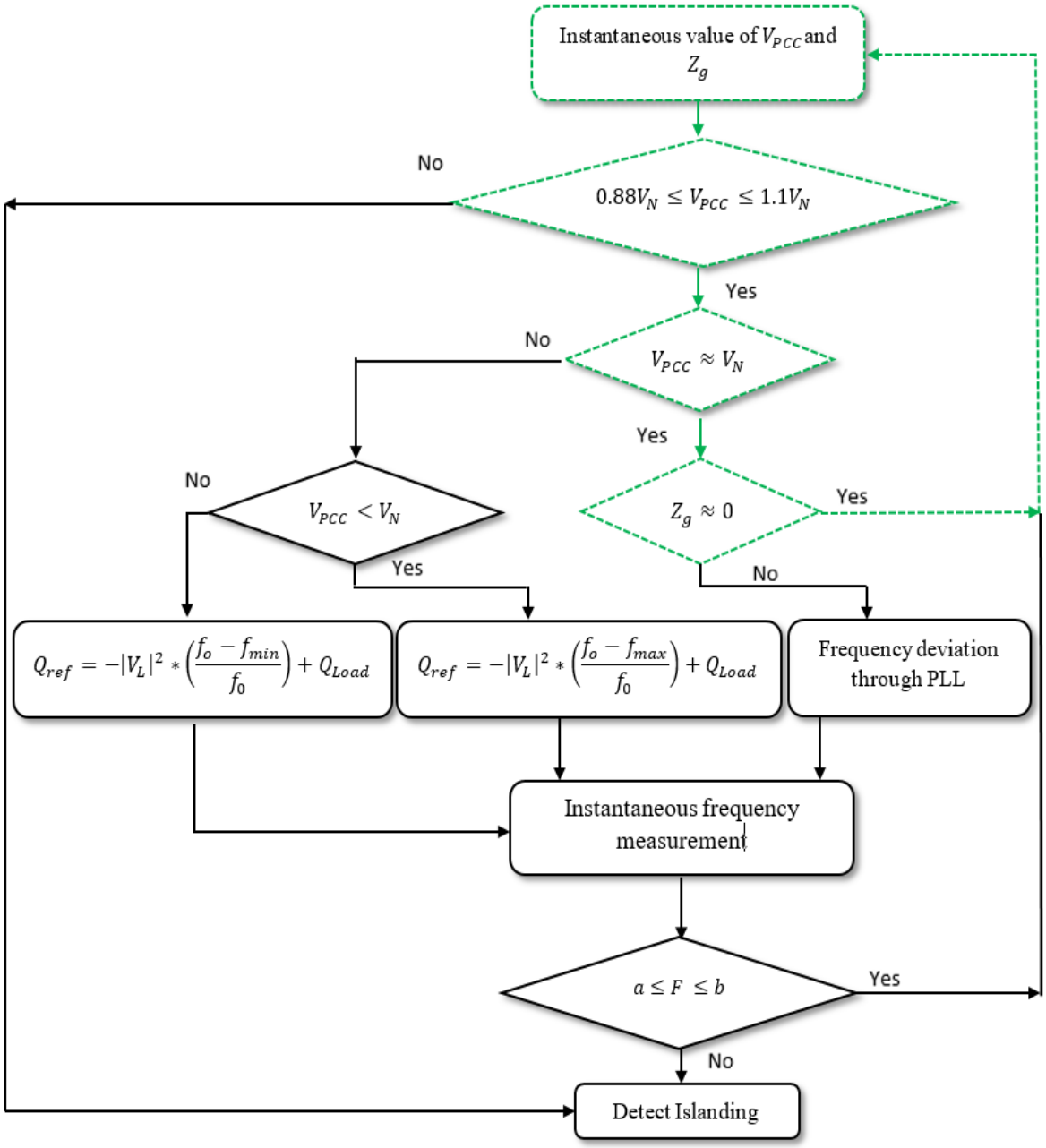

Figure 4-9 Flow chart of proposed islanding detection technique

At every instant, the voltage at PCC, its frequency and reactive power consumed by load are monitored. V_{PCC} and grid impedance Z_g plays a vital role in the proposed algorithm. The doted part of the flow chart shows the nominal operation of the system. The V_{PCC} and its frequency is measured at each instant of time and based on their values the proposed algorithm detects the islanding event. If the frequency and voltage are in their nominal range, then system works fine. In normal conditions value of Z_g is approximately zero.

The grid impedance Z_g gets changed when the main utility is disconnected from the grid and based on the value of Z_g, the positive feedback loop in PLL drifts the frequency either to infinity or to zero depending on the resonance frequency of the RC or RL load. Power mismatch is not required for islanding detection when loads are RC or RL. But when the load is resistive then PLL cannot detects islanding.

Reactive power control strategy is developed to detect islanding event when the load is resistive or RLC load having a resonance frequency equal to the nominal frequency of the system. Reactive power control strategy sets the new reference point of reactive power. Active power mismatch is needed to deviate the system voltage. The active power mismatch required for this system can be calculated by using equation (6-1). If V_{PCC} is not within the specified range of V_N then new reference of reactive power is set by using equation (3-27). Based on the value of V_{PCC} , the new Q_{ref} is set taking into consideration that the frequency will deviate when the utility is disconnected from grid. In this proposed method, the frequency is precisely monitored and the tripping signal is generated when the system frequency deviates from its nominal limits. The proposed algorithm relaxed the

frequency limits to ± 2 % so it can easily differentiate between islanding event and other disturbances in the system. Here “a” is the minimum threshold of frequency and in this work its value is 58.8 Hz whereas “b” is the maximum threshold of system frequency and its value is 61.2 Hz. The threshold of frequency is high. So, the system can differentiate among islanding event and other disturbances in the system.

Chapter 5

SIMULATON RESULTS AND DISCUSSION

In this chapter, the simulation results of current controller and proposed islanding detection method are discussed.

5.1 MATLAB simulation results of dq-frame current controller

The single line diagram of the test system for islanding detection is shown in Figure 5.1. Simulation is done in MATLAB/Simulink. MATLAB Simulink model to test the proposed technique is shown in Figure 5.2. The three-phase grid is connected with inverter and load at PCC. In this work three-phase balanced, sinusoidal grid voltage is considered. DC-link voltage is 500V. The inductor is used to reduce harmonics in the system. Proposed PLL is connected at PCC and it gives frequency and phase angle as an output. The current controller independently controls the active and reactive power of the system. The controller can controls the power sharing between grid, load, and inverter. With the help

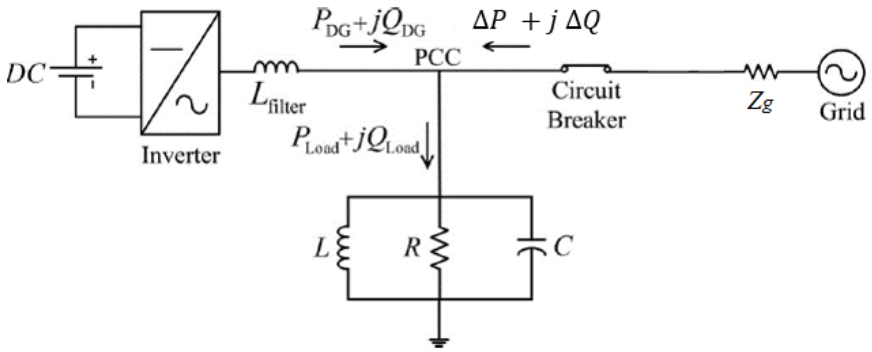

Figure 5-1 Single line diagram of test system for islanding detection

of current controller, active and reactive power can be injected into the grid. The parameters for MATLAB simulation are described in Table 5.1.

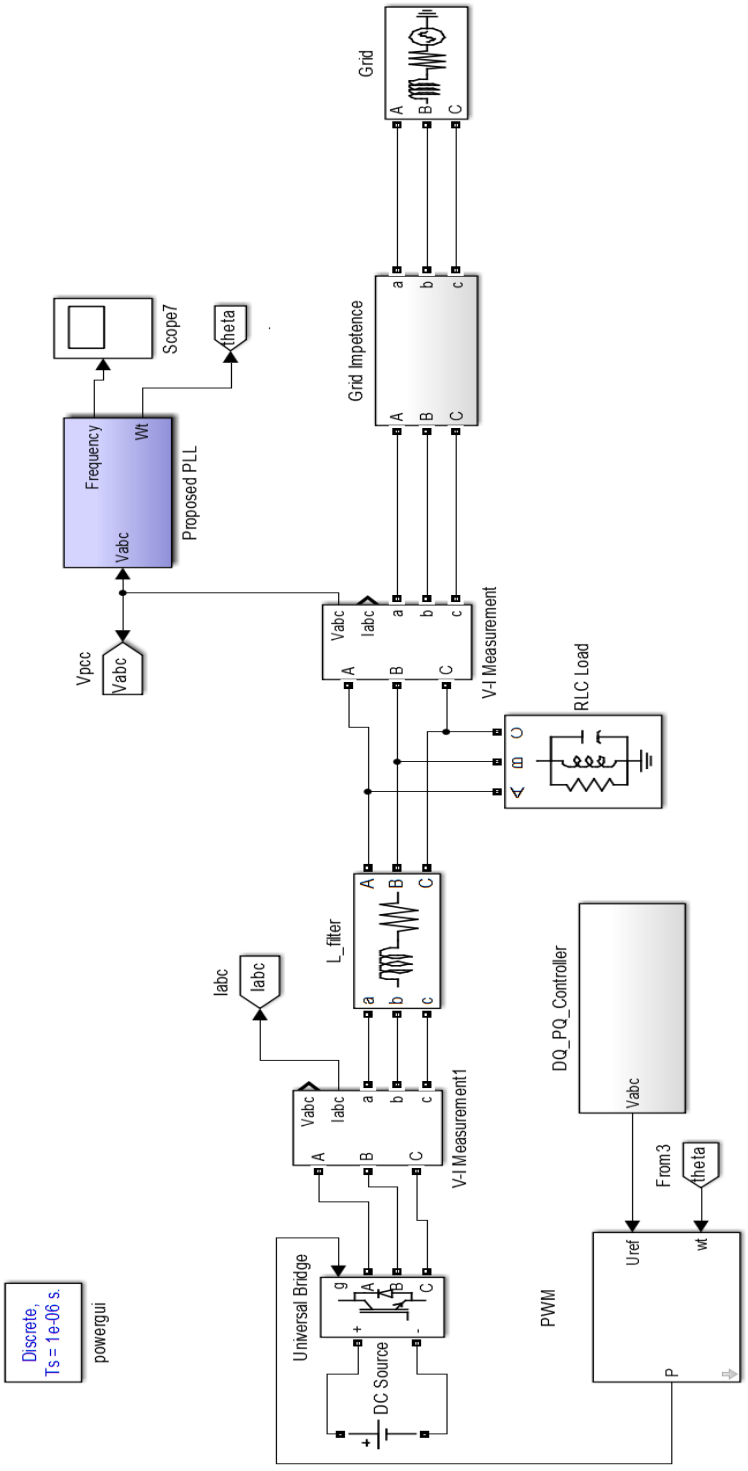

Figure 5-2 Simulink diagram of developed system for islanding detection

Table 5-1 Simulation parameters for controller testing

Grid voltage V_g	110V
Grid Impedance Z_g	0.0813 Ω
τ_i	2 milliseconds
L_{filter}	80 mH
Nominal frequency f_o	20 KHz
k_p	150
k_i	20
V_{DC}	500 V
Time step T_s	1 μs
Carrier frequency f_s	20 KHz

5.1.1 Change in active power reference

Figure 5.3 and Figure 5.4 show the active and reactive power tracking of the inverter. Figure 5.3 (a) shows the three-phase voltage at PCC. It shows that the system voltage is not affected by the change in active power reference. In Figure 5.3 (b), it is shown that amplitude of the current is changing due to the change in active power reference. The current controller regulates the line current to track the new active power reference. So, the variations in current are due to change in reference point of active power. Figure 5.3 (c) shows that at the beginning active power varies from zero to 50 W and at 0.2 seconds it varies from 50 to 300 W. The reactive power remains constant in this case. In Figure 5.3 (c), the reference power is shown in the solid line and the thick line shows the active power generated through DG. The results show that the controller is tracking the reference power quickly and efficiently.

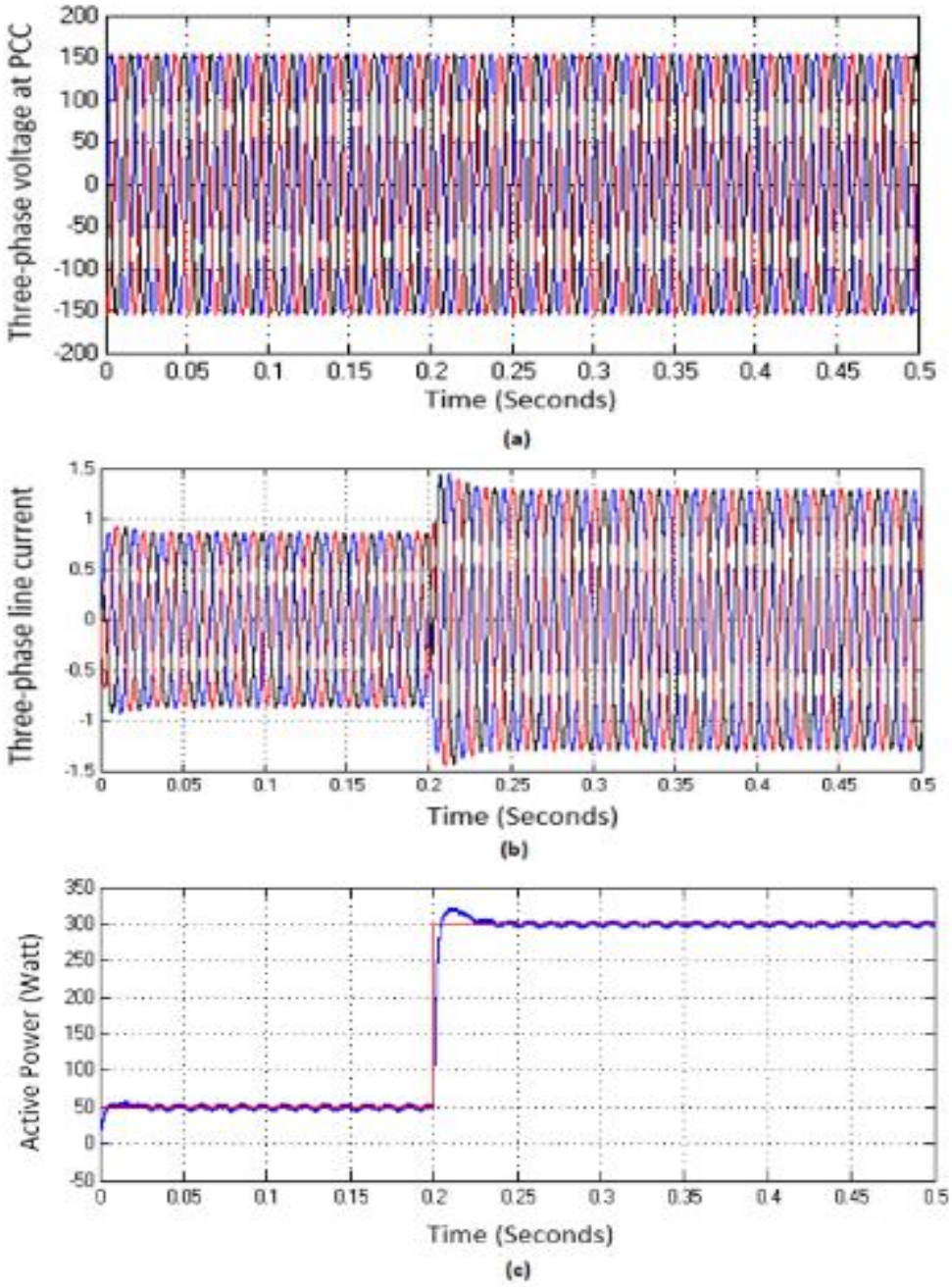

Figure 5-3 Change in active power reference

(a) Three-Phase voltage at PCC

(b) Variation in current due to change in active power reference

(c) Tracking of active power reference.

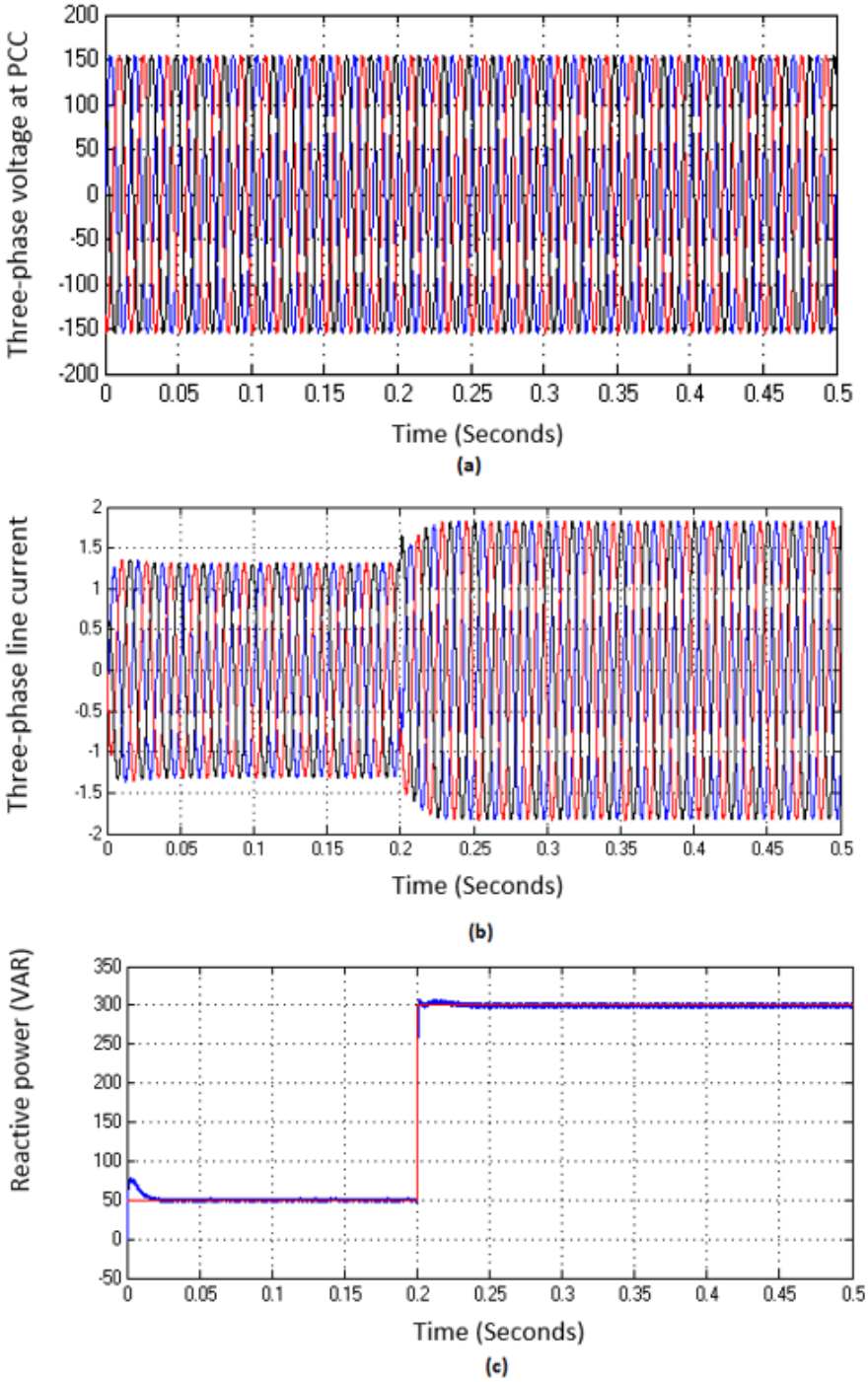

Figure 5-4 Change in reactive power reference

(a) Three-phase voltage at PCC

(b) Variation in current due to change in active power reference

(c) Tracking of active power reference.

The three-phase voltage at PCC is shown in Figure 5.4 (a). It shows that change in reactive power reference of the controller does not affect the system voltage. In Figure 5.4 (b) the amplitude of the current is changing due to change in reactive power reference. The controller is controlling the line current to track the reactive power reference. So, the variations in current are due to change in reference point of reactive power. In Figure 5.4 (c), it is shown that at the beginning reactive power varies from zero to 50 VAR and at 0.2 seconds it varies from 50 to 300 VAR. In this case, the active power remains constant. In Figure 5.4 (c), the reference power is shown as a solid line. The thick line shows the reactive power supplied by DG system.

5.1.2 Change in reactive power reference

The controller is tested based on a simultaneous change in both active and reactive power reference. Figure 5.5 represents the three-phase voltage of the system. Figure 5.6, shows that the variations in current occur due to change in active and reactive power reference. So, the controller tracks the reference point of active and reactive power by regulating the line current. Figure 5.7 shows the simultaneous change in reference of active power. Active power reference changes from zero to 200 W at the beginning and at 0.3 seconds, reference power changes from 200 to 400 W. Figure 5.8 shows that at the beginning reactive power varies from zero to 50 VAR and at 0.1 seconds it varies from 50 to -100 VAR. In Figure 5.7 and 5.8, active and reactive power reference are shown in the solid line and the dark thick line shows the tracking power generated from distributed generation. The results show that the active power and reactive power are tracked efficiently.

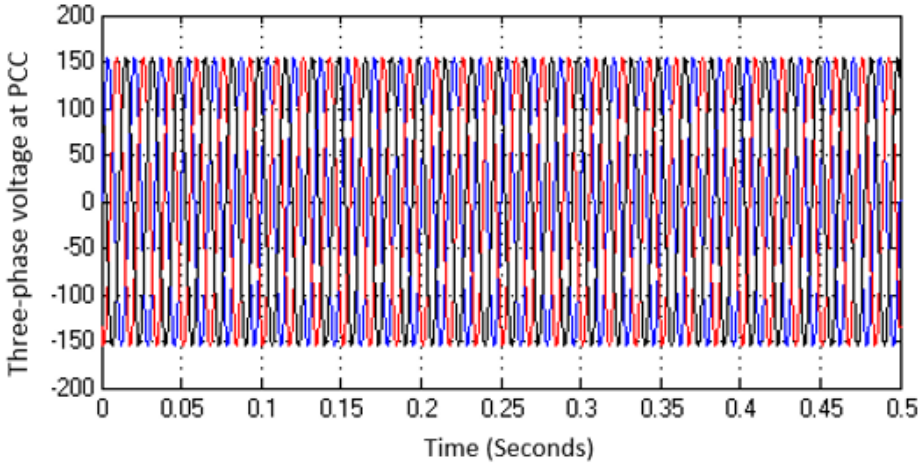

Figure 5-6 Voltage behavior when change occur in both power reference

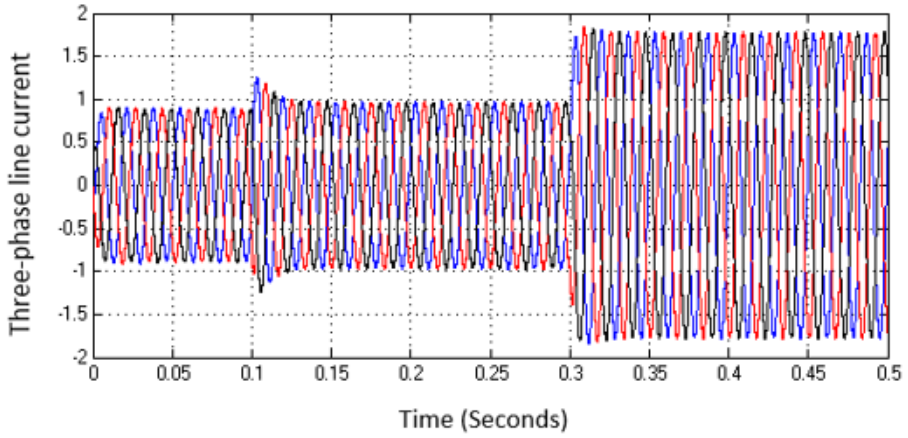

Figure 5-7 Current variations when both power reference are changing

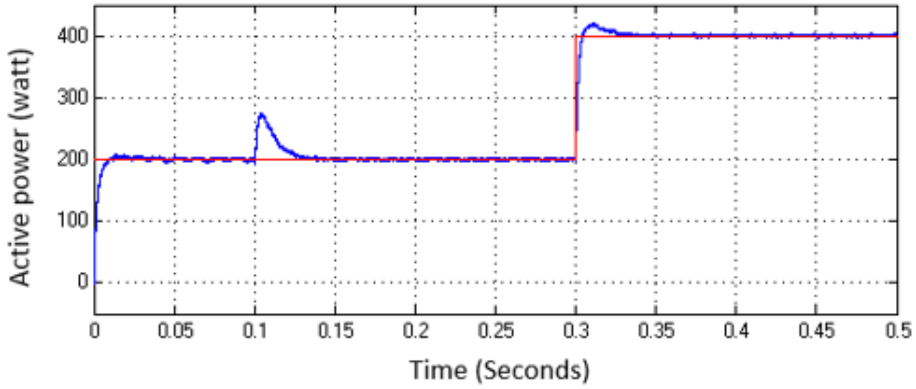

Figure 5-5 Simultaneous change in active power reference

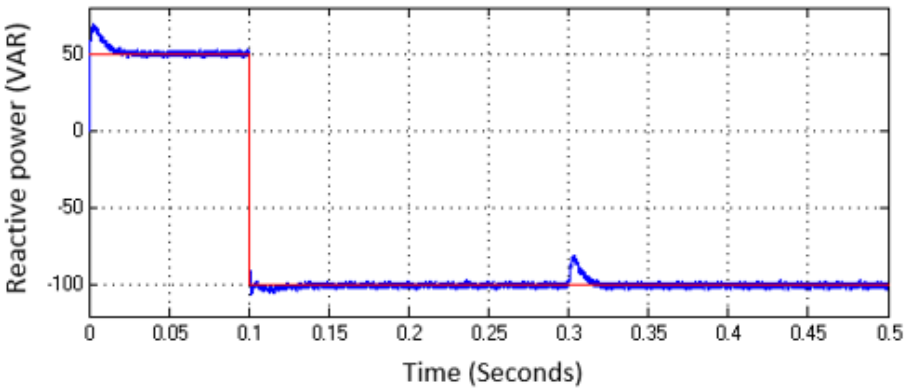

Figure 5-8 Simultaneous change in reactive power reference

The results show that the developed current mode controller is robust and enables the system to regulate the power independently.

5.2 Comparison between ANN and PI controller

Figure 5.9 shows the comparison of artificial neural network based controller with PI controller. The dotted line shows the PLL output with PI controller and Solid red line shows the output of PLL with ANN based controller.

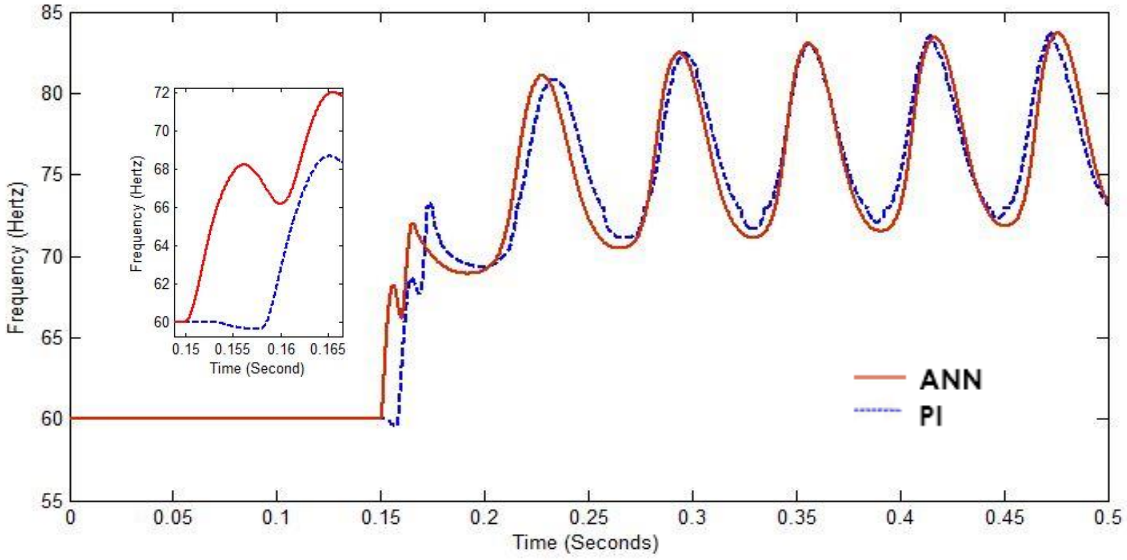

Figure 5-9 Comparison between ANN and PI controller when load is RC

The result shows that in normal conditions both PI and ANN efficiently tracks the system frequency. But when islanding occurs, the ANN response is faster than PI. PLL with ANN based controller quickly deviates the system frequency. Islanding occurs at 0.15 seconds and ANN detects islanding condition at 0.1530 seconds while the PI controller detects it at 0.1602 seconds.

5.3 Simulation results for islanding detection

The schematic diagram for testing the proposed islanding detection technique is shown in Figure 5.2. The parameters for simulation are described in Table 5.2. In this work, system voltage is 230V while the frequency is 60 Hz. The islanding detection algorithm is tested on three types of loads i.e. RC, RL and RLC load.

Table 5-2: Parameters for MATLAB simulation

Z_{L1} (RC)	15 Ω // 50 µF
Z_{L2} (RL)	15 Ω // 70 Mh
Z_{L3} (RLC)	5 // 300 µF // 23.3 Mh
Z_g	100 Ω
Grid voltage V_g	230 V
$f_{nominal}$	60 Hz
Carrier frequency f_s	20 KHz

Islanding occurs at 0.15 seconds. Figure 5.10 to Figure 5.13 show the behavior of system frequency when islanding occurs. Based on frequency deviation the islanding is detected.

Results show that before 0.15 seconds system works fine and PLL is tracking nominal frequency of 60 Hz.

After islanding, the frequency is changing abruptly. Figure 5.10 shows that when islanding occurs, the frequency is going down due to RL load. Figure 5.11 shows that after islanding, the frequency is going to infinity due to RC load. In both cases, PLL follows the resonance frequency of the load. In RC and RL loads, islanding is detected based on grid impedance Z_g and no power mismatch is needed.

Figure 5.12 and Figure 5.13 represent the behavior of system frequency under resistive load. The proposed PLL is not detecting islanding condition in case of resistive load. For resistive load, reactive power mismatch is created to detect islanding. The reactive power reference is changed based on voltage variation. The purpose of changing the reactive power reference is to create a reactive power mismatch between inverter and the load. So, the reactive power mismatch shifts the frequency from its nominal value when islanding occurs. The new reactive power reference is set by using equation (3-27). The variation in frequency when Vpcc is less than 0.98*V_N is shown in Figure 5.12. Figure 5.13 represents the variation in frequency when Vpcc is greater than 1.01*V_N

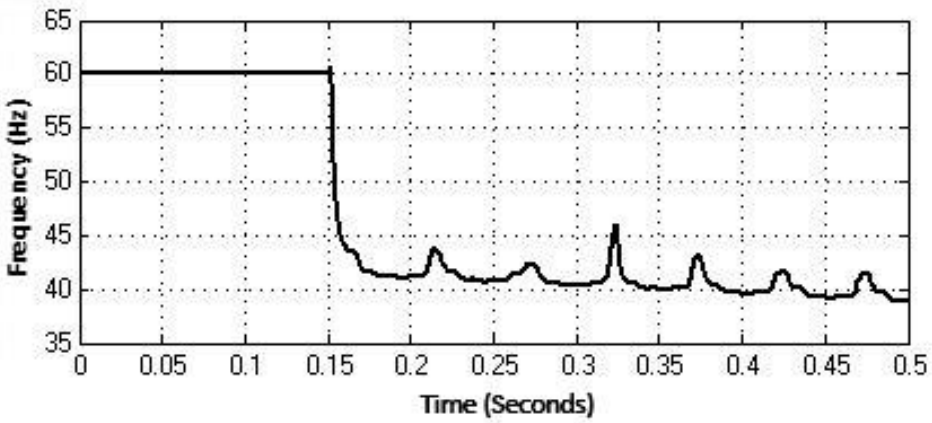

Figure 5-10 PLL output when load is RL

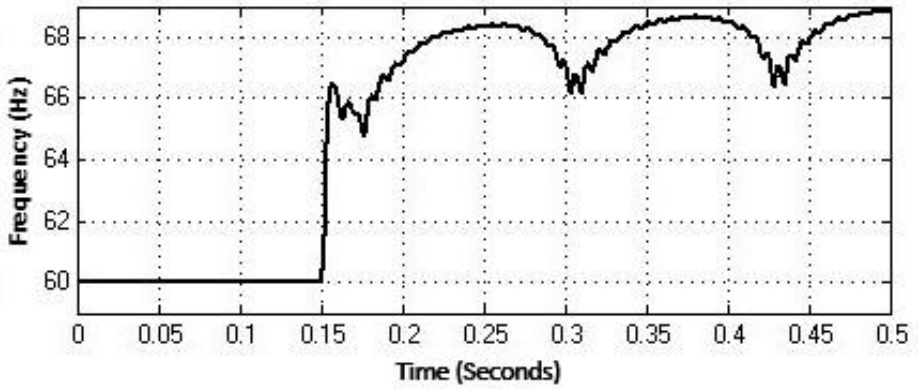

Figure 5-11 PLL output when load is RC

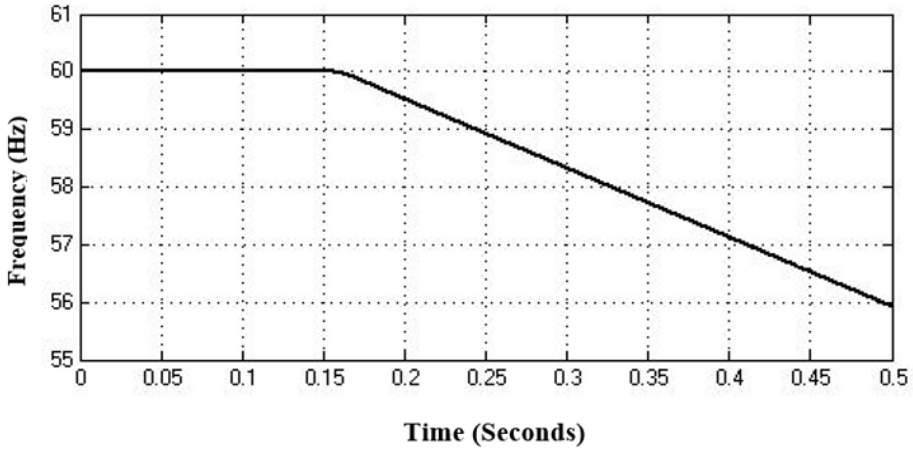

Figure 5-12 PLL output when load is RLC and Vpcc is less than Vn

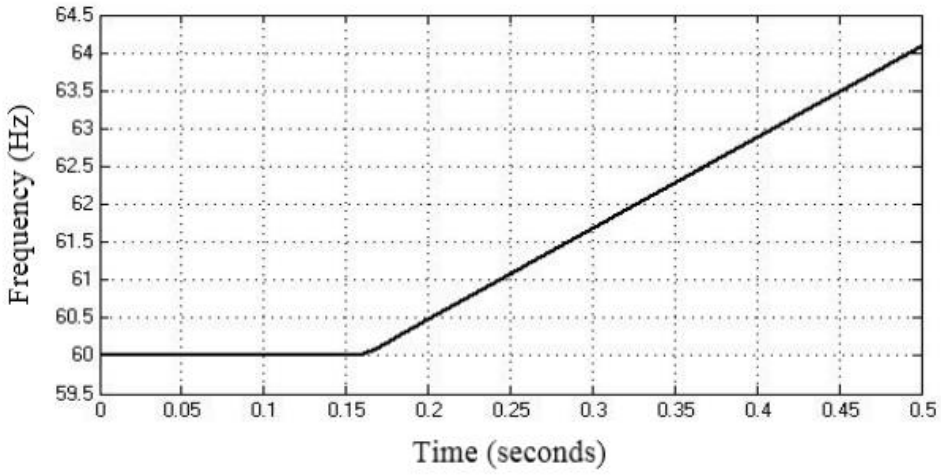

Figure 5-13 PLL output when load is RLC and Vpcc is greater than Vn

The proposed algorithm detects islanding condition in all kind of loads and has negligible non-detection zone. The results show that the variations in frequency due to islanding is very high as compared to the variation due to switching of capacitors or load. So, the proposed islanding detection method can easily differentiate the islanding event with other disturbances in the system. Frequency variation is the key parameter in this technique to detect islanding. Simulation results show the efficiency of islanding detection method.

5.4 Sensitivity analysis due to increase in load demand

Figure 5.14 shows the frequency variation due to sudden increase in load. The results show that the transient in frequency increases as the load increases. The extra load is added into the system at 0.1 seconds. In base case (0% increase in load) the local load is exactly equal to the power generated from DG system. In this analysis DG is not capable of meeting the increase in load demand. The 20% increase in load means that the utility has to supply

power to the meet the extra load demand of 20 %. For base case, the local load is RLC load of 0.5 KW and 50 inductive reactive power.

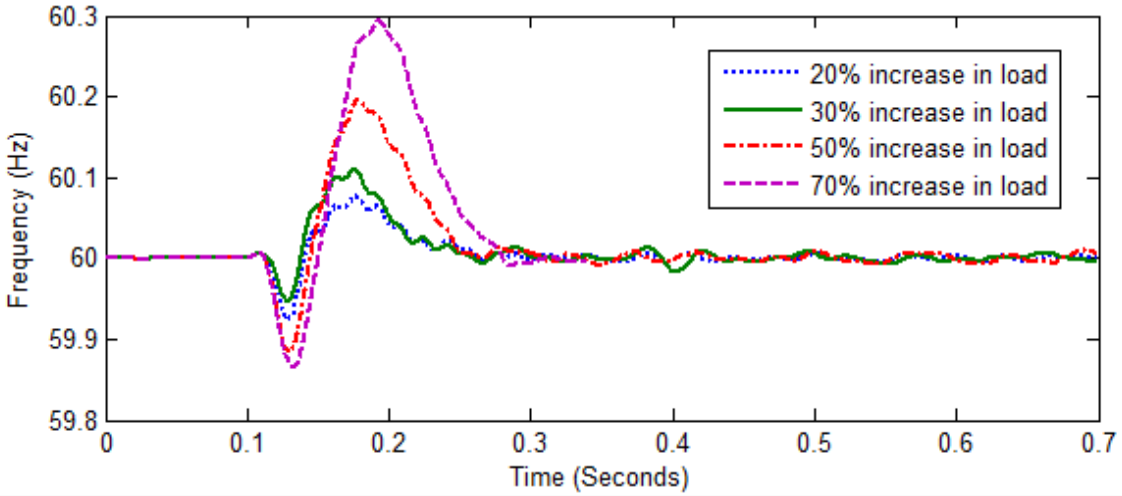

Figure 5-14 Variation in frequency due to increase in load demand

Before 0.15 seconds the system frequency is 60 Hz and after 0.15 seconds the frequency varies due to sudden increase in load and at 0.3 seconds the frequency again comes to its nominal value (60 Hz). The result shows the robustness of developed PLL. In all cases, the modified PLL efficiently tracks the nominal frequency of the system.

5.5 Comparison with literature

Non- detection zone (NDZ) is the criteria to check the efficacy of the islanding detection techniques. Figure 5.15 shows the non-detection zone of the proposed technique. The NDZ for active power is calculated using equation (5-1) [89].

$$\Delta P = -3V * \Delta V * I * cos\ \theta \tag{5-1}$$

Where ΔP represents the active power mismatch. The rated voltage and current is represented by V and I respectively, ΔV is the change in voltage due to ΔP and the power factor of the system is represented by $cos\ \theta$. The maximum and minimum allowable

voltage limits per IEEE standards are 0.9 to 1.1 pu so the allowable deviation in voltage is 0.1 and -0.1. By using the conventional techniques, the NDZ for active power mismatch is 144.49 W and -144.49 W for this system. Now the NDZ for reactive power mismatch can be calculated as [89]

$$\Delta Q = \frac{3V^2}{\omega_n L}\left(1 - \frac{f_o^2}{(f_o \pm \Delta f)^2}\right) \tag{5-2}$$

Where f_o is the nominal frequency of the system, $\omega_n = 2 * \pi * f$ and Δf is the change in frequency. According to IEEE standard [6], the allowable frequency range is from 60.5 to 59.3 Hz which gives the allowable deviations in frequency from -0.5Hz to -0.5Hz approximately. So, the NDZ for conventional techniques is 203.8 Var and – 203.8 Var. With the proposed technique, no active and reactive power mismatch is needed for RC and RL loads because the islanding detection is based on grid impedance Z_g.

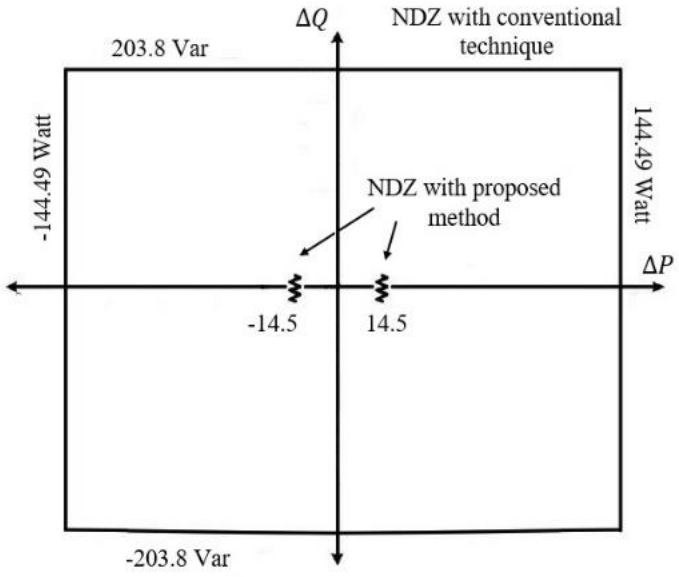

Figure 5-15 Non-detection zone for resistive load

Only for resistive load or RLC load having 60 Hz resonance frequency, the active power mismatch is required. The NDZ of the proposed islanding detection method is from 14.5 W to -14.5 W and that is negligible as compared to the conventional techniques. Figure 5.13 represents the non-detection zone only for a resistive load. The results show that when loads are inductive or capacitive, the system can detect islanding event in 0.301 milliseconds. For a resistive load, the proposed methods take 0.1 seconds to detect an islanding condition. The proposed islanding detection technique detects landing condition in all cases and the detection time is in fraction of milliseconds and have negligible NDZ. The power quality is not affected by proposed active islanding detection technique.

Chapter 6

EXPERIMENTAL RESULTS

6.1 Hardware implementation

A prototype is developed to validate the theoretical results. Real-time inverter, digital controller, programmable loads, distribution panel, voltage and current sensors, amplifier circuit, PV simulator are used in prototype. In this section, the detail description of components, hardware implementation and controller implementation are discussed.

6.1.1 Experimental setup

The signal routing in-between the hardware equipment is shown in Figure 6.1. The inverter is connected to the grid through L_{filter} and the load is connected at PCC. Both DG and grid are supplying power to the local load. The voltage and current sensors are connected with the system to measure the voltage at PCC and current at AC side of the inverter. The power system interfacing board (PSIB) measures the voltage and current of the system. The measured voltage and current are then fed to the dSPACE. There is a bidirectional signal flow between PSIB and dSPACE. The controller is loaded in the dSPACE. It takes voltage and current as input and after processing gives pulse width modulation (PWM) as an output signal. Phase locked loop is also loaded in dSPACE. It measures the phase angle and frequency of the grid voltage. The PWM generated from dSPACE cannot be fed directly to the inverter. The amplifier IC is working as a bridge between dSPACE and inverter. The schematic diagram of connections between dSPACE

and inverter is shown in Figure 6.8. The amplifier IC amplify the PWM from 5V to 15V and the fed in to the inverter. Based on PWM, the inverter generates the AC voltage. The generated AC voltage from the inverter is exactly same as the grid voltage. The magnitude, phase angle, phase sequence and frequency of the generated voltage from inverter are same

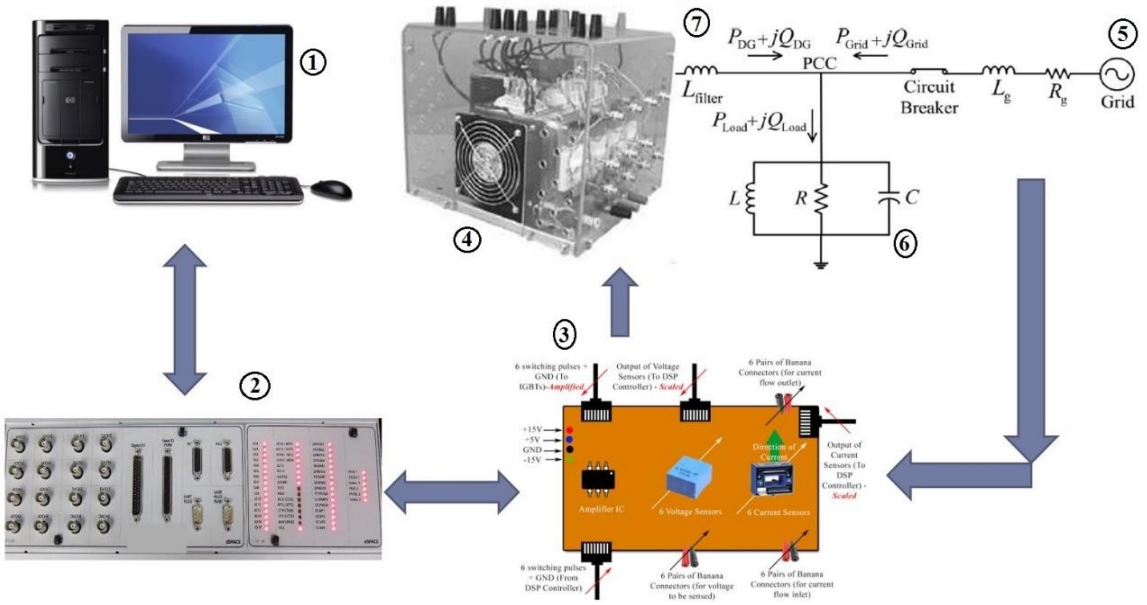

Figure 6-1 Schematic diagram of experimental setup

as that of grid voltage. In Figure 6.1, the components used in experimental setup are described below.

1. Computer
2. Digital controller (dSPACE)
3. Power System Interfacing Board
4. Inverter
5. Utility Grid
6. L_{filter}

The experimental setup is shown in Figure 6.2. The description of each component used in experimental setup is described below.

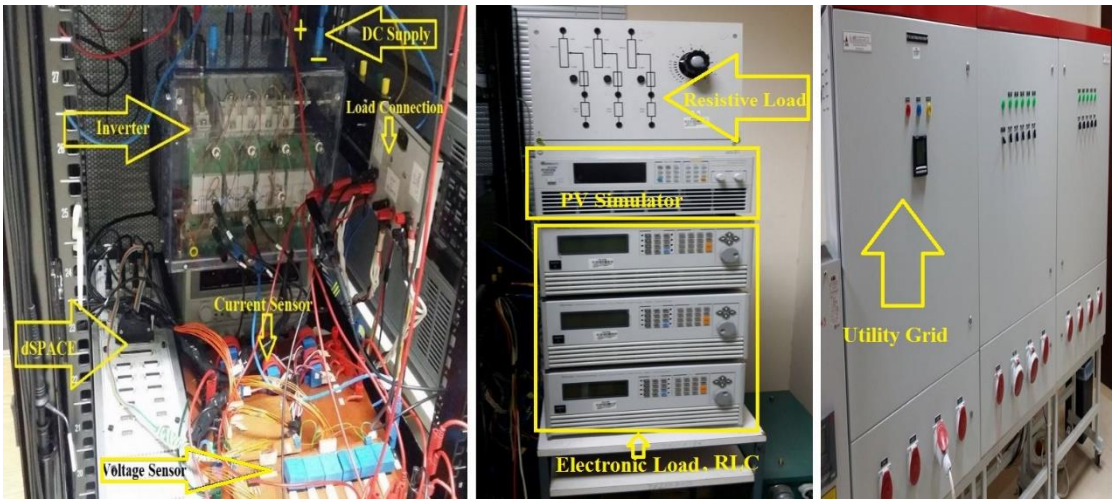

Figure 6-2 Experimental setup

The experimental setup consists of the inverter, digital controller, programmable loads, distribution panel, voltage and current sensors, amplifier circuit, PV simulator, filter. In this work the PV simulator is act as a constant DC voltage source. The DC side of inverter takes DC voltage from PV simulator. The rated voltage of the grid is 230 volts and its nominal frequency is 60 Hz.

6.2 Component description

The detail description of all components used in experimental setup are described below.

6.2.1 Computer

The computer used in this work having 12 processors of 3.3GHz, 26 Gb ram. The computer is equipped with software that can be used to control and visualize the waveforms of the input and output signals of the dSPACE.

6.2.2 Power system interfacing board (PSIB)

The components in the experimental setup cannot take direct signal from each other. dSPACE needs the system voltage and current to scale down within ± 10 volts. The inverter cannot take PWM directly from dSPACE. So, based on that need, PSIB is developed. It is shown in Figure 6.3. PSIB can perform two main functions, first it measures the system

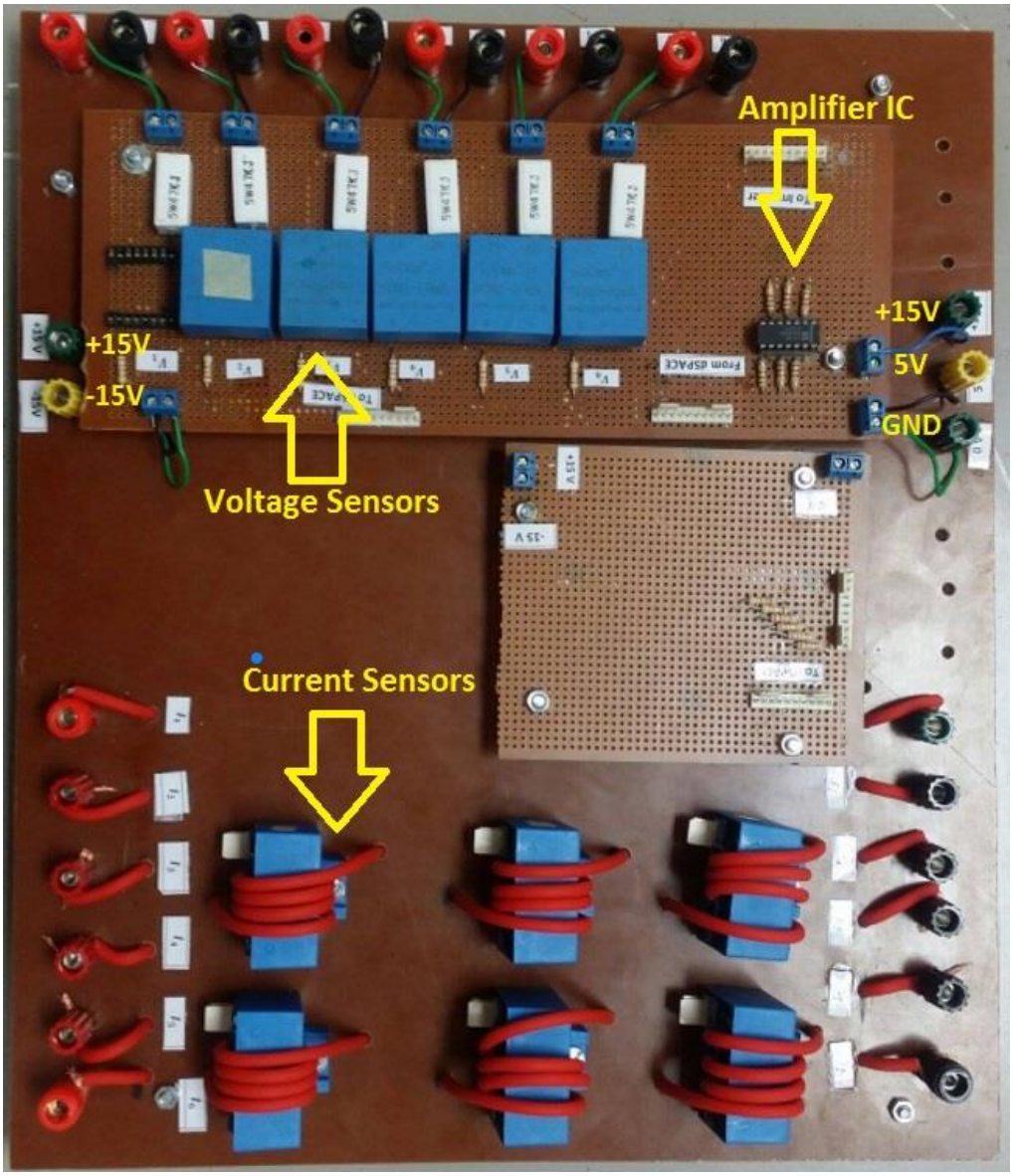

Figure 6-3 Power system interfacing board

voltage and current and second it resolves the interfacing issue in-between inverter, dspace and with the system.

The schematic diagram of power system interfacing board is shown in Figure 6.4. PSIB is well protected and voltage and current can be measured easily. PSIB is equipped with six voltage and six current sensors and has six pairs of connectors for voltage and current

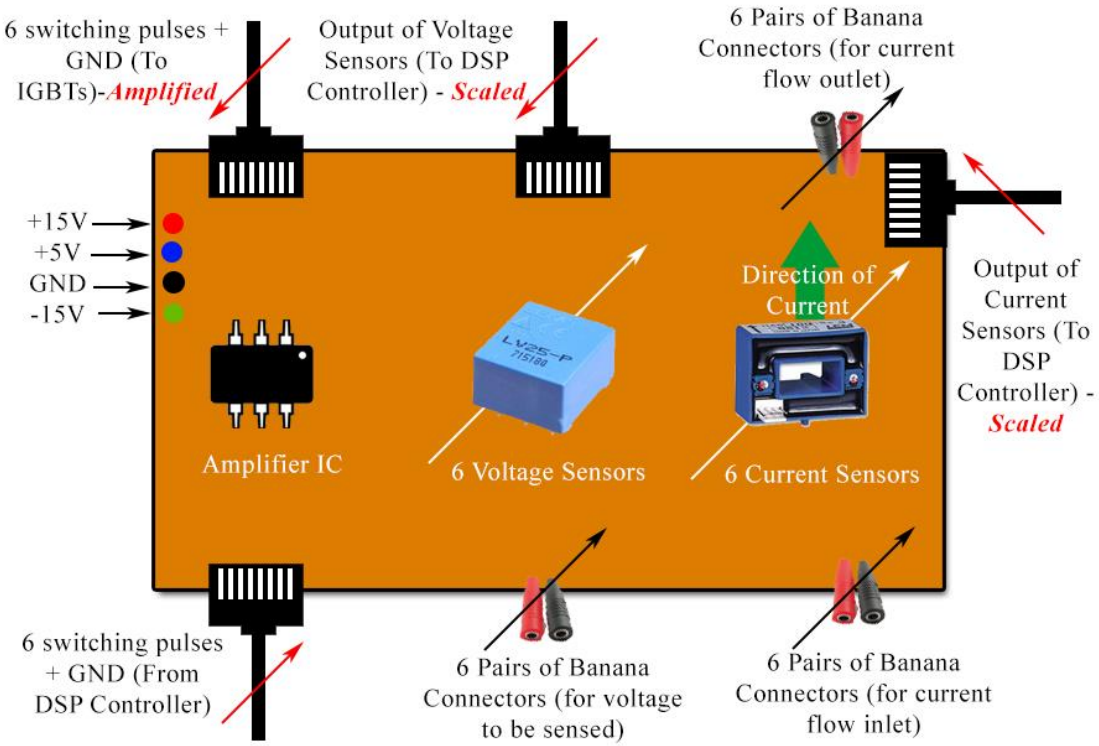

Figure 6-4 Schematic diagram of power system interfacing board

sensors. Six 47 KΩ resistor at the input side of voltage sensor is connected to limit the current. ± 15 volts, zero volts, and 5 volts are used to energize the sensors and amplifier IC. Amplifier IC is used to amplify the PWM and fed it to the inverter. Components used in PSIB are shown in Figure 6.5.

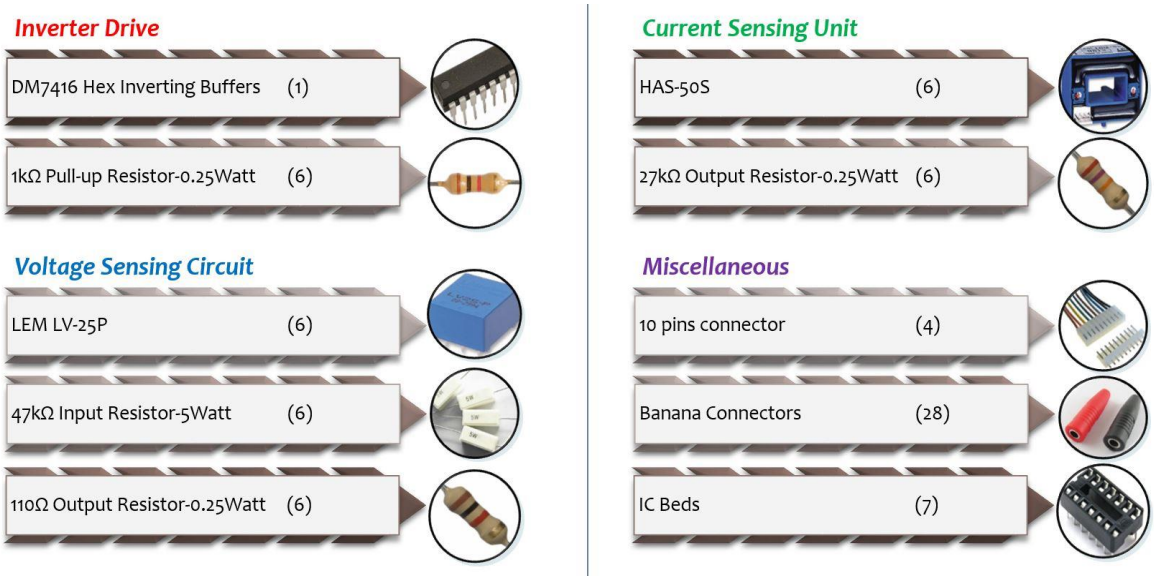

Figure 6-5 Components used in power system interfacing board

6.2.3 Voltage transducers

Voltage transducers are used to reduce the level of the voltage signals, which can be fed to the controller for a possible control action. The basic block diagram of the voltage transducer is shown in Figure 6.6. The dSPACE controller, used in this work has input output range up to ±10V while the actual voltage ratings are much higher. So, voltage transducers are used to make the input voltage waveform compatible with the permissible controller I/O range.

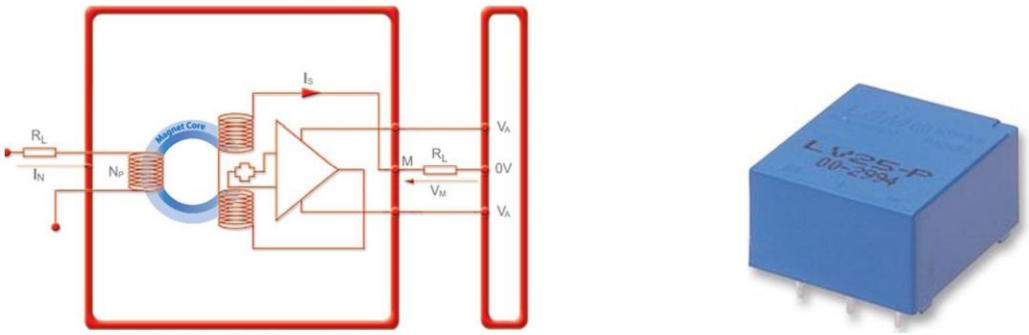

Figure 6-6 Voltage transducer

LEM LV 25P sensor is used as a voltage transducer for the real-time measurement of voltage signal. It can measure DC, AC, and pulsed voltage signals from 10 to 1500 V using the Hall effect. The terminals *HT*+ and *HT*- represent the signal phase connection terminals of supply voltage. The user specified resistor *R* is used as input resistors to limit the input current less than 10mA at the primary side. The resistor *RM* is used as a measurement resistor. The value of *RM* should be carefully selected so that the output voltage will remain in the range less than ± 10V. The voltage terminal $\pm Vc$ represents the terminal of the supplied dc voltage of ±15V.

6.2.4 Current transducers

Current transducers are utilized to transform the high rated current signals into the low valued voltage signals in the distribution system, which can be fed to the controller for a possible control action. The basic block diagram of the current transducer is shown in Figure 6.7. HAS 50-s sensor is used as a current transducer for the real-time measurement of source load and active power filter current. It is a closed loop sensor, which can measure DC, AC and pulsed current signals up to 50A using the Hall Effect.

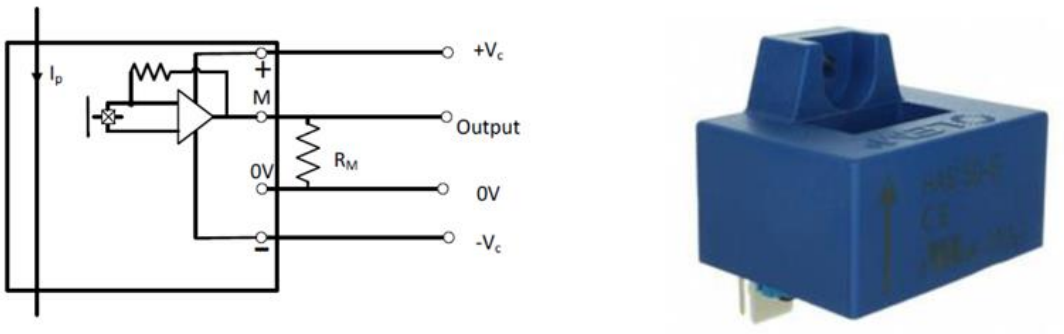

Figure 6-7 Current transducer

A single-phase wire is passed through the current sensor to induce the current in the sensor coil. The output of the sensor is an AC voltage signal, which can be easily used in any industrial controller like dSPACE. The basic block diagram of the current transducer is shown in Figure 6.7, where Ip represents the measured current. The voltage terminal ±*Vc* represents the terminal of the supplied DC voltage of ±15V. The resistor *RM* is used as a measurement resistor. The value of *RM* should be carefully selected so that the output voltage will remain in the range less than ± 10V.

6.2.5 DX 7143 hex inverting buffer (Amplifier IC)

Hex inverter is used to interface the inverter with the dspace. The schematic diagram of Amplifier IC is shown in Figure 6.8. After processing, digital controller gives PWM as an output but its voltage range is of ±10V but inverter needs 15V pulses as an input.

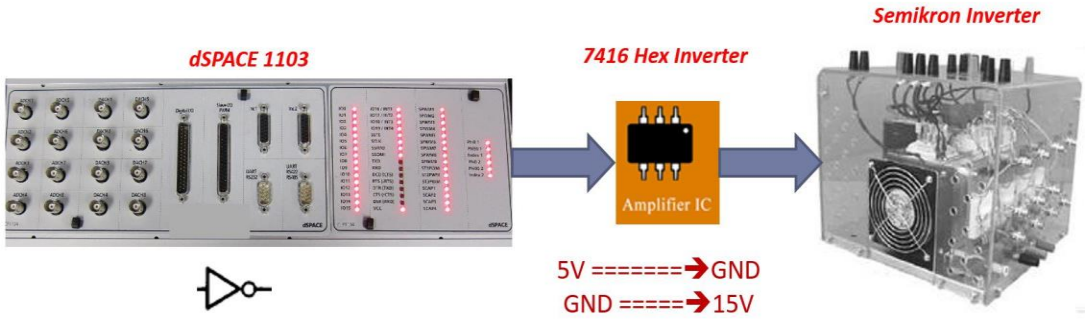

Figure 6-8 Hex Inverting buffer

The digital output of the dSPACE controller is in the range of ±10V, but the gate pulses input required by the real-time inverters are ±15V. Therefore, a double gain amplifier is designed using the hex logic integrated circuit DM7416. The schematic diagram of the hex inverter circuit is shown in Figure 6.9.

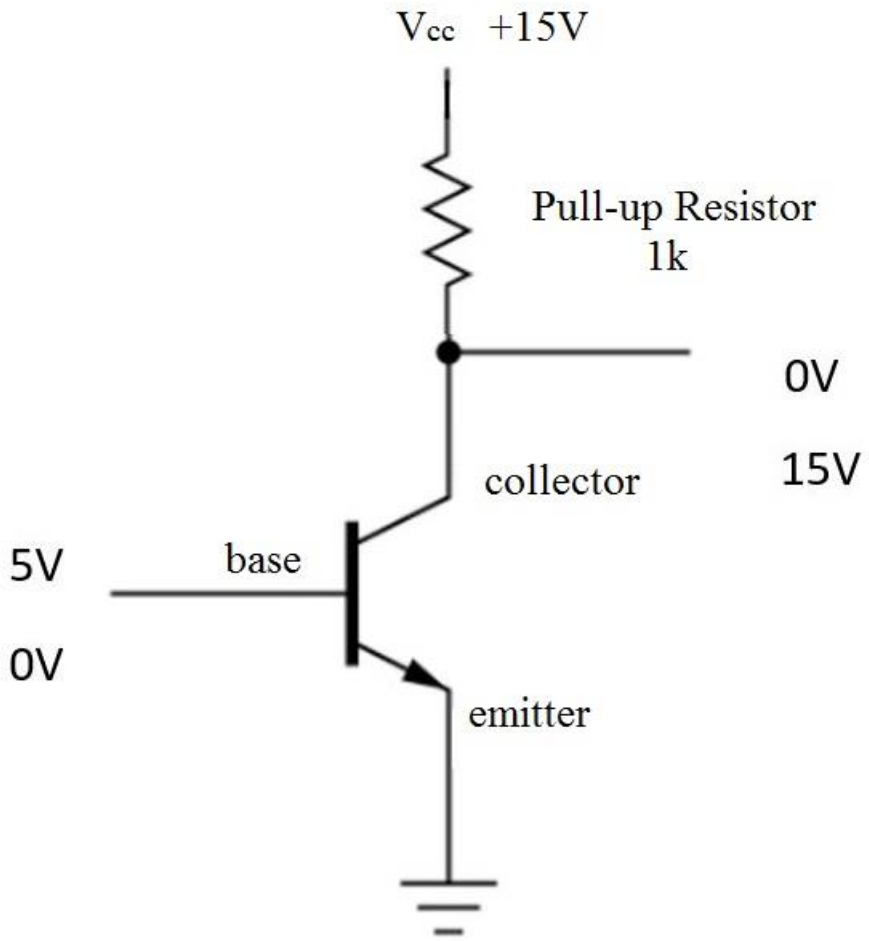

Figure 6-9 working of amplifier IC

This hex inverter has a minimum breakdown voltage of 15 volts. A 15 volts DC supply is provided at the Vcc terminal. The output level can be adjusted using pull up resistors. This hex inverter can sink maximum current up to 30mA.

6.3 Experimental results of dq-controller

In section 6.2, the experimental setup was discussed in detail. Now the experimental results of the developed current controller are discussed. Current controller is capable of synchronizing the inverter with the existing grid. Active power and reactive power can be

injected separately as well as simultaneously. Figure 6.10 shows the experimental setup of grid connected system. Rated grid voltage of the system is 230V and the fundamental frequency is 60 Hz. The load is connected at PCC. Digital controller (dSPACE) takes voltage and current as an input and after processing generates PWM as an output.

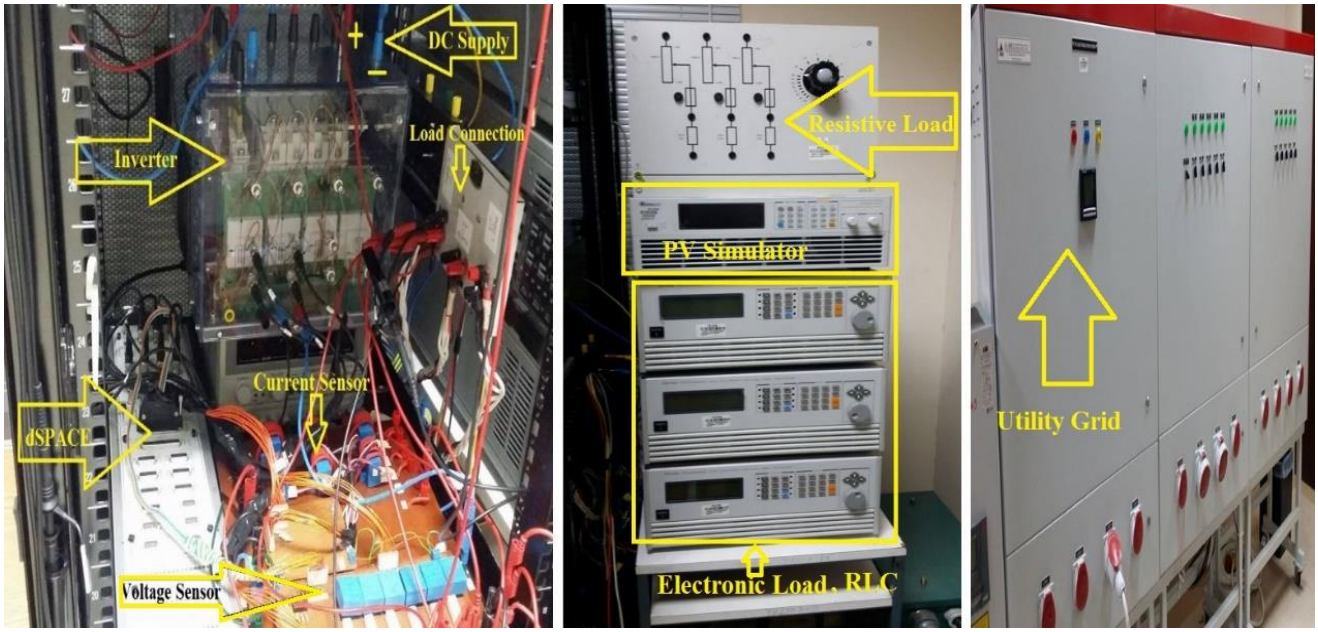

Figure 6-10 Experimental setup for current testing

The power is shared according to the reference setting while the system will remain synchronized. Figure 6.11 shows the synchronization of the system. The dark signal shows the grid voltage while the light grey signal represents the inverter voltage. Both voltages are in-phase and have the same frequency. The current waveform is shown in purple color. The load is resistive; the current is in phase with the voltage.

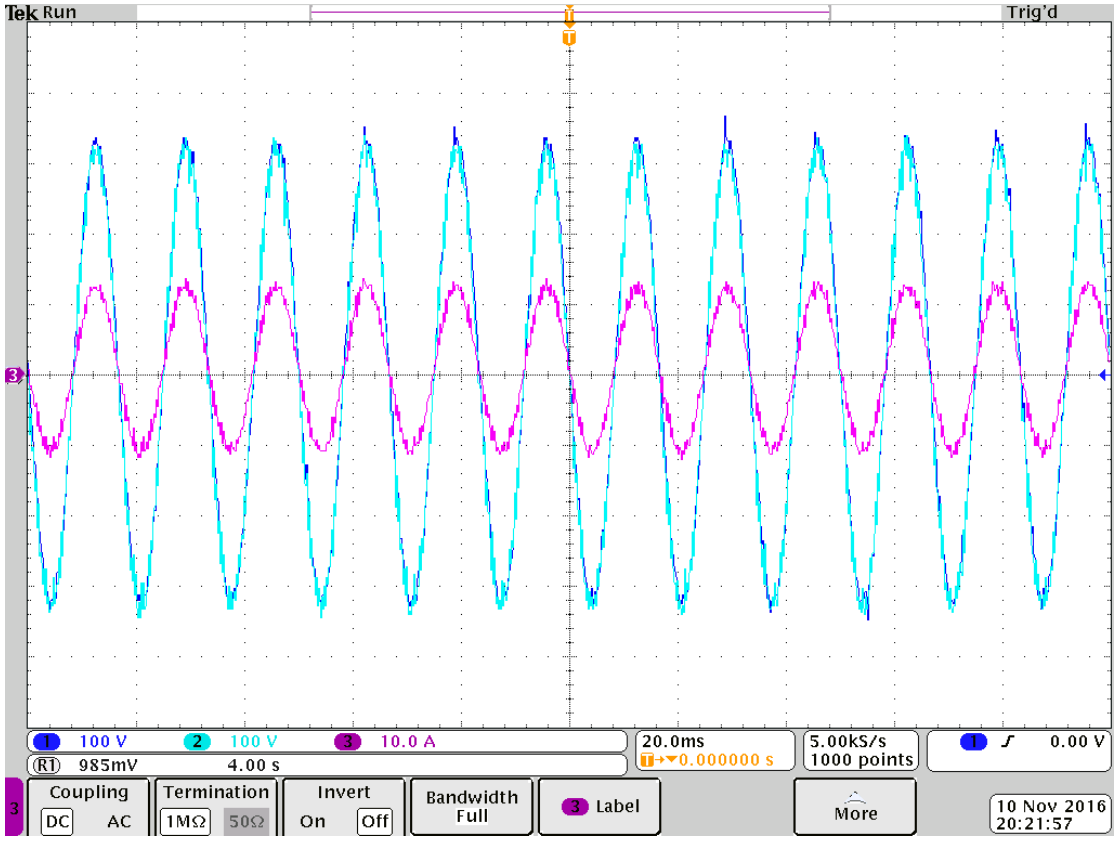

Figure 6-11 Grid synchronization graph

Table 6-1 Parameter for experimental setup for controller testing

Load resistance Z_L (R)	250 Ω
Grid Impedance Z_g	0.8012 Ω
Grid Voltage V_g	230 V
Time step T_s	2610 µs
$f_{nominal}$	60 Hz
L_{filter}	32 Mh
V_{DC}	500V
Carrier Frequency f_s	5 KHz

Table 6.1 shows the parameters for the experimental setup. The power meter is connected to the distribution panel (grid). It measures the root mean square value of voltage and current of the grid as well as the active, reactive and apparent power of the grid. The positive sign on the meter shows that the grid is delivering power to the system while negative sign shows that the grid is absorbing power i.e. (inverter is injecting power into the grid).

6.3.1 Power sharing in-between grid and inverter

In this section, experimental results are discussed. Different cases were run to test the controller. Figure 6.12 to Figure 6.14 represents power sharing between the grid and the inverter. The positive sign means that utility grid is supplying power to the load and negative sign means that grid is absorbing power. Figure 6.12 shows that grid is supplying 68 W and 80 VAR to the load and rest of the power is coming from the inverter. So, both inverter and

Figure 6-12 Grid is supplying power to local load

Figure 6-13 Power sharing between grid and the system

the grid contribute to meet load demand. In Figure 6.13, it is shown that inverter is supplying active power to the load and grid contributes ideally zero watt. Reactive power of 229 VAR is injecting into the grid from the inverter. Figure 6.13 shows the independent control of active and reactive powers between grid and inverter.

Figure 6.14 shows that the active and reactive power are simultaneously injected into the grid. The inverter is injecting 17 W and 299 VAR into the grid.

Figure 6-14 Inverter is injecting power into grid

Results show the efficacy of the current controller. The above current controller is robust and it enables the system to regulate the power independently. It is also capable to synchronize the grid with the DG systems. The experimental results validate the efficiency of the controller.

6.4 Hardware results for islanding detection

The experimental setup for islanding detection is shown in Figure 6.15. A constant DC power source is connected with the grid through an inverter. The inductor is used as a filter. Parameters for experimental setup are described in Table 6.2. Rated voltage of the grid is 230 volts while the rated frequency is 60 Hz. The load is connected at PCC. Time step of 50 μs is used for hardware setup. The switching is done manually to disconnect the grid from the system to create an island. In the simulation, islanding is done at 0.15 second but in the hardware, islanding was done manually so the islanding was not done exactly at the same time. But the results show that the system frequency deviates abruptly when islanding occurs.

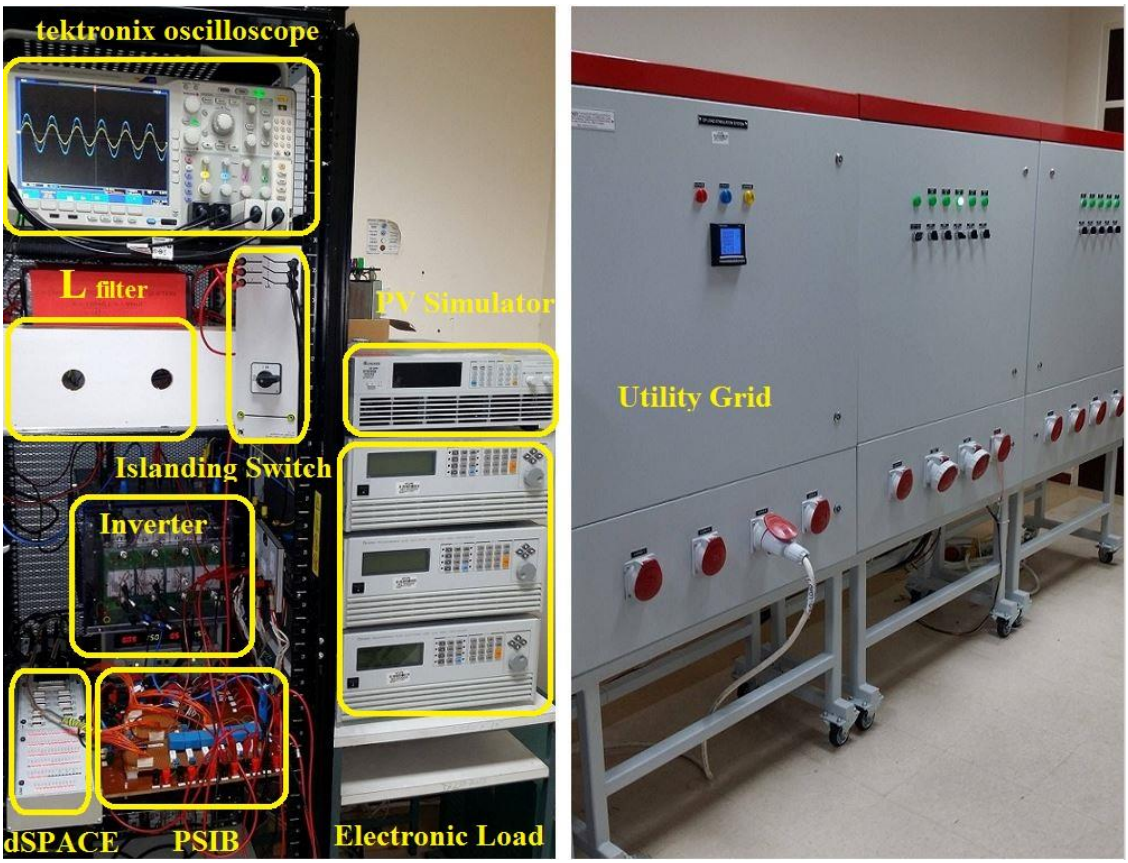

Figure 6-15 Experimental setup for islanding detection

Table 6-2: Parameters for experimental setup

Z_{L1} (RL)	10 Ω // 52.3 mH
Z_{L2} (RC)	10 Ω // 50 µF
Z_{L3} (R)	210 Ω
L_{filter}	33.8 mH
Inverter	Single phase, IGBT, Full bridge
Rated Frequency (f_n)	60 Hz
Sampling time (T_s)	50 µs
Rated phase voltage (V_N)	230 V
Carrier frequency (f_s)	2160 Hz

Islanding is detected when the frequency varies from its specified value. Figure 6.16 and Figure 6.17 represent the PLL output when the load is RL (inductive load) and RC (capacitive load) respectively. In normal conditions, PLL follows the 60 Hz frequency and at 0.15 seconds, the system frequency goes to infinity in RC load and goes to zero in RL load to detect islanding. For the resistive load, the frequency deviation depends on the instantaneous value of V_{PCC} voltage and reactive power mismatch. The new reactive power reference is set based on variation in voltage. For $V_{PCC} > 1.01 * V_N$ then Q_{ref} is set to negative and the frequency goes to infinity. For $V_{PCC} < 0.98 * V_N$, Q_{ref} is set to positive value and the system frequency moves down to zero. The deviation in frequency when load is resistive is described in Figure 6.18 and Figure 6.19 respectively. Islanding is detected based on frequency deviation of the system.

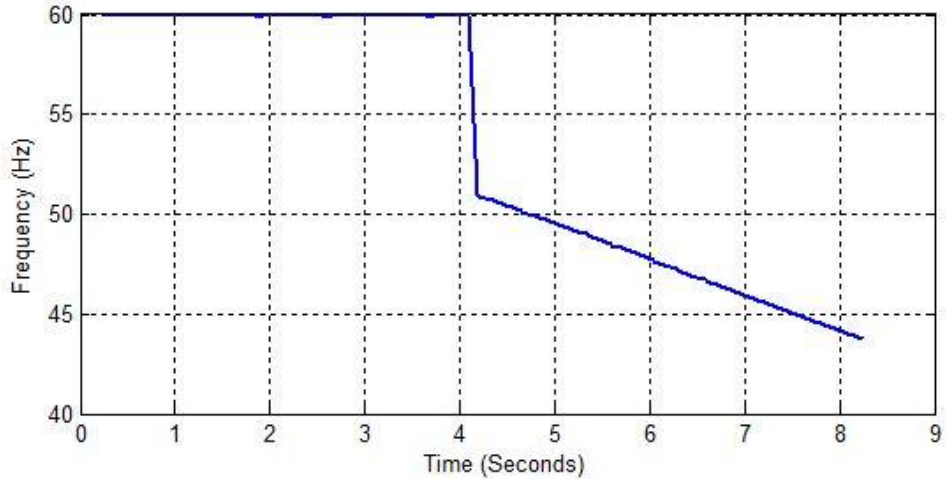

Figure 6-16 Experimental result when load is RL (inductive load)

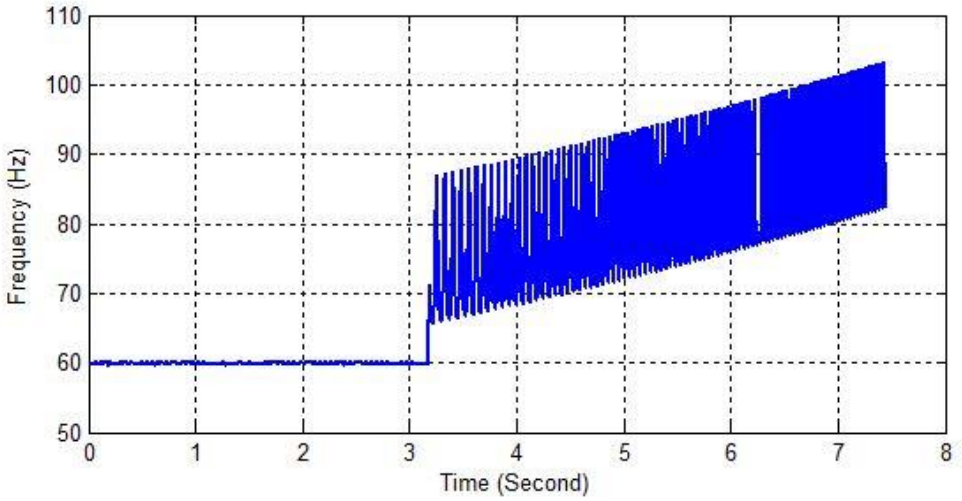

Figure 6-17 Experimental result when load is RC (capacitive load)

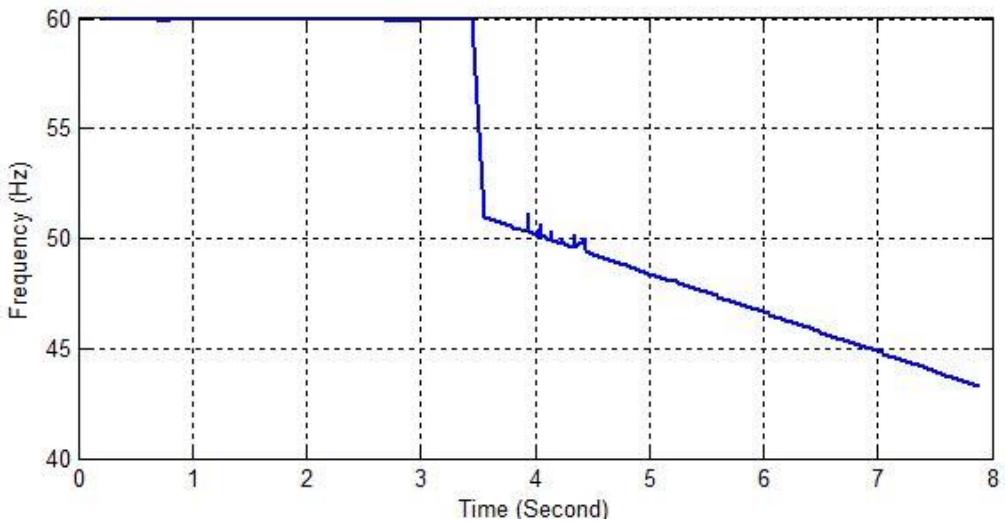

Figure 6-18 Experimental result when load is R and Vpcc is less than Vn

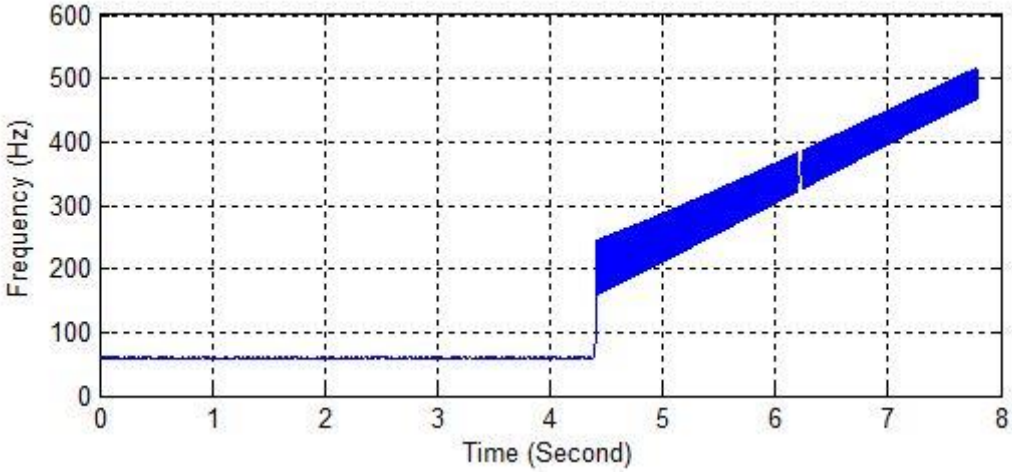

Figure 6-19 Experimental result when load is R and Vpcc is greater than Vn

Both experimental and simulation results follow the same behavior when islanding occurs hence the theoretical results are validated. Both experimental and simulation results show the efficacy of the proposed method. The results show that the developed algorithm can detect islanding in all cases and have negligible non-detection zone.

Chapter 7

CONCLUSION AND FUTURE WORK

In this chapter, the conclusion and inferences of the thesis are summarized. This mainly outlines the considered problem, the proposed solution and analysis of the results. Also, a discussion on the prospects of extending this work in future is presented at the end.

7.1 Conclusion

The purpose of this work is to develop a real-time islanding detection method. A comprehensive literature review has been established. A novel islanding detection method is proposed. Furthermore, active and reactive power controller is developed and tested in real-time. A laboratory scale prototype has been developed for monitoring and detection of islanding conditions.

The conclusion of this thesis can be drawn as:

- A comprehensive literature review has been accomplished for detecting islanding conditions as per IEEE-standard 1547 and UL-1741 standard.
- A novel active islanding detection technique is proposed based on voltage and frequency deviation.
- Self-created reactive power mismatch and modified phase locked loop are proposed to detect islanding events.
- The positive feedback loop is introduced in the phase locked loop to destabilize the PLL output when islanding occurs.

- PI controller in phase locked loop is replaced by artificial neural network (ANN) based controller. So, the PLL works efficiently and quickly reaches its steady state value.
- The results show that by using ANN, the proposed PLL detects islanding within a fraction of a millisecond and has negligible non-detection zone.
- Simulation results show that the proposed PLL can synchronize DG with the grid. When islanding occurs the PFL in PLL deviates the frequency abruptly and detects islanding within 0.301 milliseconds.
- By relaxing the limits of frequency up to $\pm 2\%$, the proposed method can differentiate the islanding condition with other disturbances in the system.
- Experimental results are exactly matched with the simulation results and follow the same behavior under different loading conditions hence the theoretical results are validated and both results show the efficacy of a proposed technique.
- The obtained results have been compared with the published literature and a significant improvement has been observed.

7.2 Future work

For a future work, the following points can be considered as an extension of the work done in this thesis.

- In this thesis, islanding detection technique is developed but power quality issues arise after islanding occurs which needs to be investigated. These issues can be reduced by using electric spring.
- After islanding, efforts can be put to develop protection scheme like relay coordination to protect the islanded system.
- A controller is needed to reduce voltage sag, swell and frequency variation when islanding occurs.
- The analysis of developed islanding detection technique is done on single inverter system, it can be further investigated in a system where multiple voltage source inverters are connected.
- The proposed islanding detection technique and electric spring can be collectively employed to detect islanding events as well as to mitigate voltage variations after islanding occurs.

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Appendix A: Description of hardware component

A.1 Programmable Electronic Load

Programmable electronic loads are designed to to simulate the AC/DC loads. The programmable AC/DC load chroma 63800 is selected to simulate the non-linear RC and RL loads and load conditions under high crest factor as shown in FigureA.1. It is capable of working under distorted mains voltage. The chroma-63800 can be configured as a constant power source up to 1800W, while as a constant current load up to 45 Arms at the

Figure A.1 Programmable loads

voltage range is 50V – 350 Vrms. Three identical units of chroma-63800 are used separately to simulate the three-phase load.

A.2 Inverter/Rectifier Module

SEMITEACH – IGBT inverter and rectifier module are used for real-time voltage source inverter implementation. The basic block diagram of this module is shown in Figure A.2, where a pair of 2200μF DC capacitor is also installed for energy storage purpose. The rectifier input is 230/ 400V while the output may vary up to 600V DC. The input output range of inverter can also vary up to 400V AC and 600V DC with 30A as a maximum current.

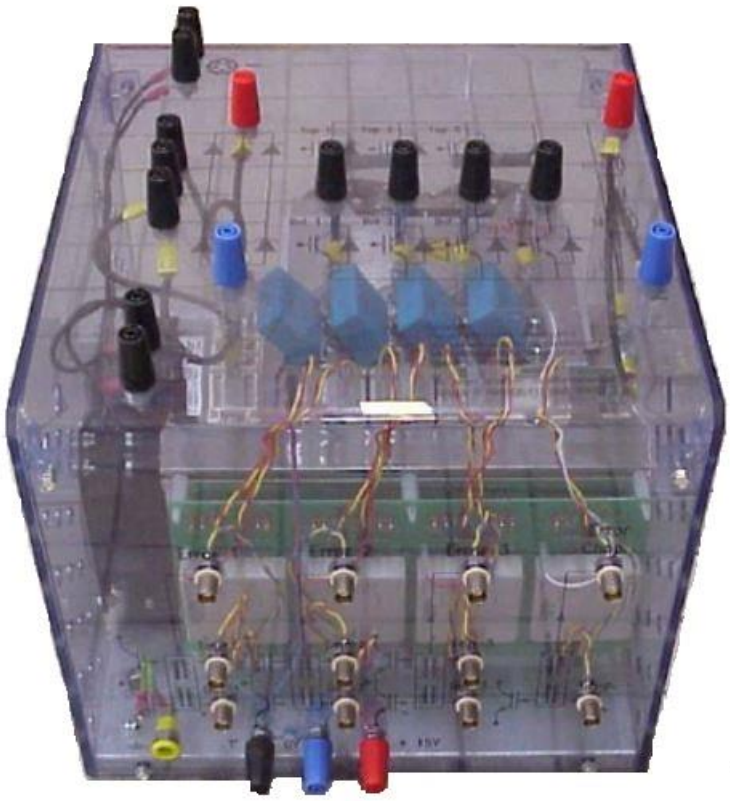


Figure A.2 Inverter and Diode Rectifier

In this study, the voltage source inverter is used. The gate pulses are provided to the inverter generated by the dSAPCE controller using an amplifier. The inverter generates voltage and synchronizes with the grid. A DC voltage source of 15 volts is applied to the gate driven circuit of the inverter.

A.3 Mixed Domain Oscilloscope

Tektronix 4104B-3 mixed domain oscilloscope is used to record the experimental results. It is capable of analyzing signals in both frequency and time domain. It can be used a spectrum analyzer. It has four channels that can be used for the measurement of voltage and current signals. The voltage probe Tektronix TPP-1000 is a 1GHz bandwidth probe used for the measurement of voltage signals up to 300 volts. It offers 10X and 2X attenuation factors. Tektronix TCP0030A probe is utilized for the measurement of source, load current signals. This probe provides the selectable measurement of 5A and 30A with the bandwidth greater than 120 MHz.

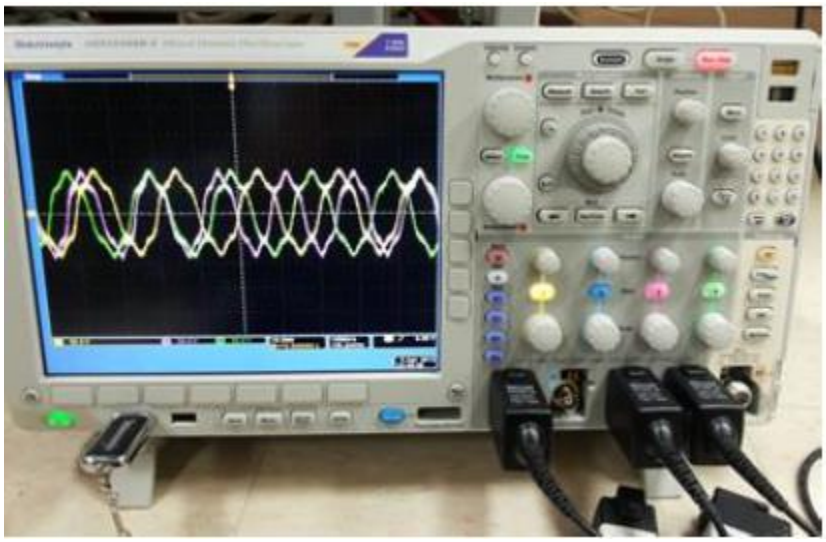


Figure A:3 Tektronix 4104B-3 mixed domain oscilloscope

A.4 Voltage and Current Transducers

Voltage and current transducers are utilized to reduce the voltage and current signals of distribution system, which can be fed to the controller for a possible control action. The dSPACE controller, used in this work has input output range up to ±10V while the actual voltage and current ratings are much higher. So, voltage and current transducers are used to make the input voltage and current signals compatible with the controller I/O range

A.4.1 Voltage Transducer

LEM LV 25P/SP5 sensor is used as a voltage transducer for the real-time measurement of voltage signal. It is a closed loop sensor, which can measure DC, AC and pulsed voltage signals from 10 to 1500 V using the Hall effect. A user-specified input resistor is used to

Figure A:4 Voltage Sensors

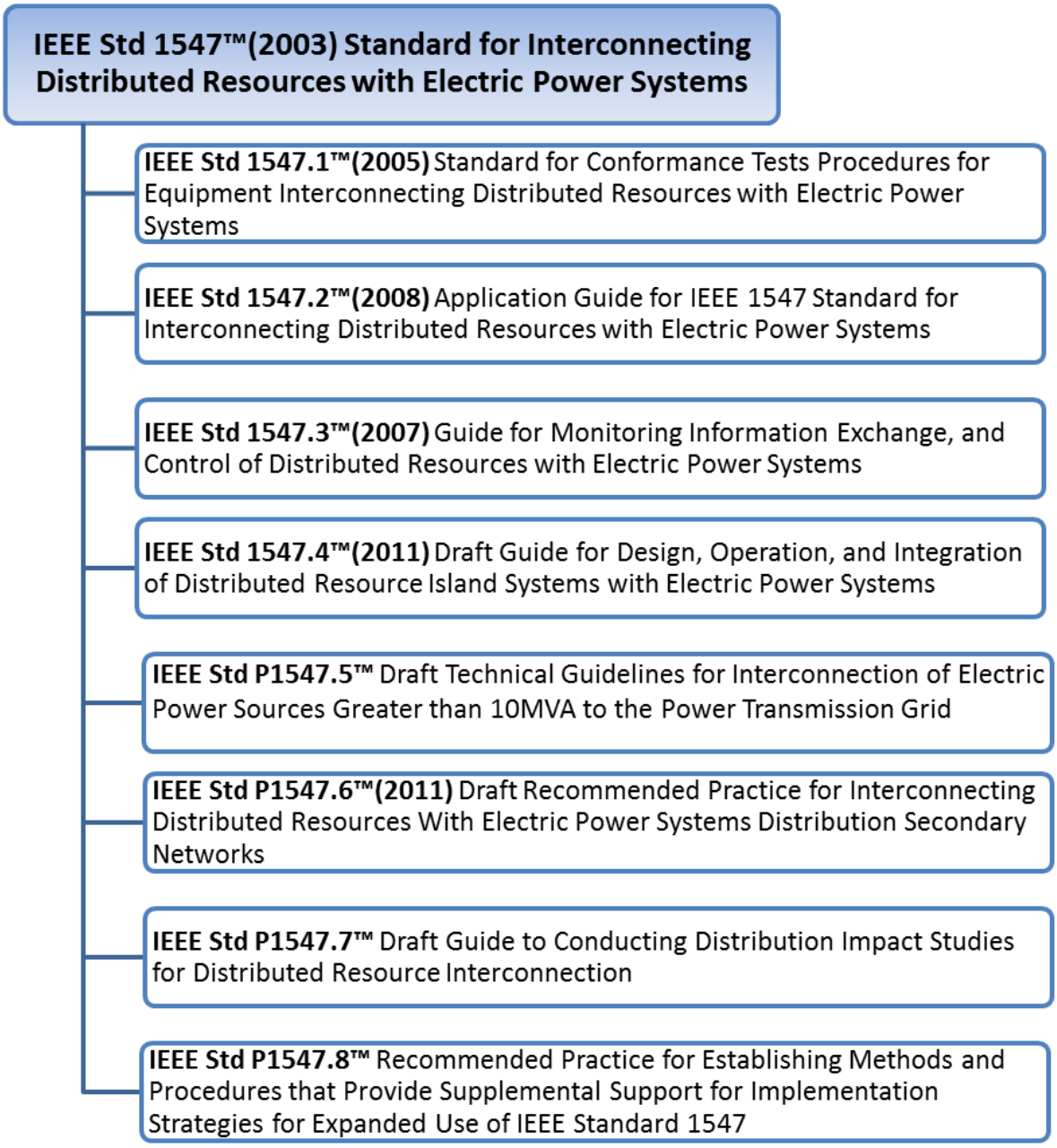
induce a current in the secondary side of the transducer, where a measurement resistor can be used to obtain the output voltage from the induced current. In this work, input resistor of 47 kΩ is used for the voltage measurement.

A.4.2 Current Transducer

HAS 50-s sensor is used as a current transducer for the real-time measurement of source load and current passing through the switch. It is a closed loop sensor, which can measure DC, AC and pulsed current signals up to 50A using the Hall effect. The output of this sensor is an AC voltage signal which can be easily used in any industrial controller.

Figure A:5 current controller

Appendix B: IEEE Standard 1547



Appendix C: dSPACE DS1103 CONTROLLER BOARD: UTILITY AND APPLICATIONS

C.1 dSPACE Controller:

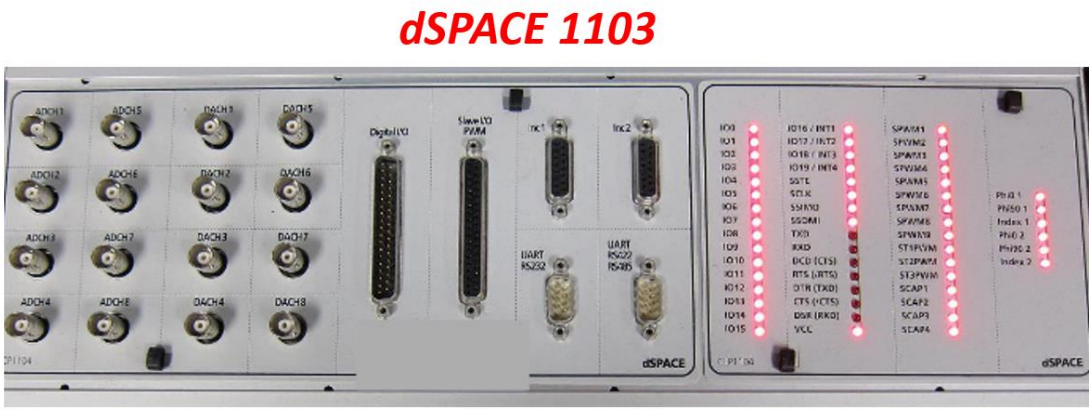


Figure C-1 dSPACE-1103

dSPACE is an industrial controller mainly used for the application development and prototyping. In this study, DS-1103 is used for the real-time controller implementation as shown in Figure C.1. The instantaneous power *p* - *q* controllers are designed in Matlab/Simulink environment with the aid of RTI tools provided by the dSPACE. The dSPACE DS-1103 controller has two major parts: expansion box and connection panel. The connection panel contains 20 analog to digital input channel (ADCH) and 8 digital to analog output channels (DACH).

The system voltage is fed to the dSPACE controller using DACH obtained from the voltage transducers. The real-time current waveforms consisting of load current is input to the dSPACE controller using DACH. The instantaneous power *p* - *q* is implemented using 50 μ sec sampling time. The gate pulses are obtained from the dSPACE using high speed digital DS1103 BIT_OUT block of master PCC.

C.2 Prominent features

1. It is a single board system, providing processing in real-time with an ample range of input/output connections.
2. High speed and precision of the input/output channels
3. Featuring CAN (controller area network) bus which allows communication between controllers and devices without requiring a computer in between.
4. Providing serial interfaces appropriate for automotive application.
5. With PLL-based UART (Universal asynchronous receiver transmitter) for high accuracy baud rate

C.3 Major applications

The DS1103 controller board is an advanced rapid prototyping tool. Following are some of its major applications:

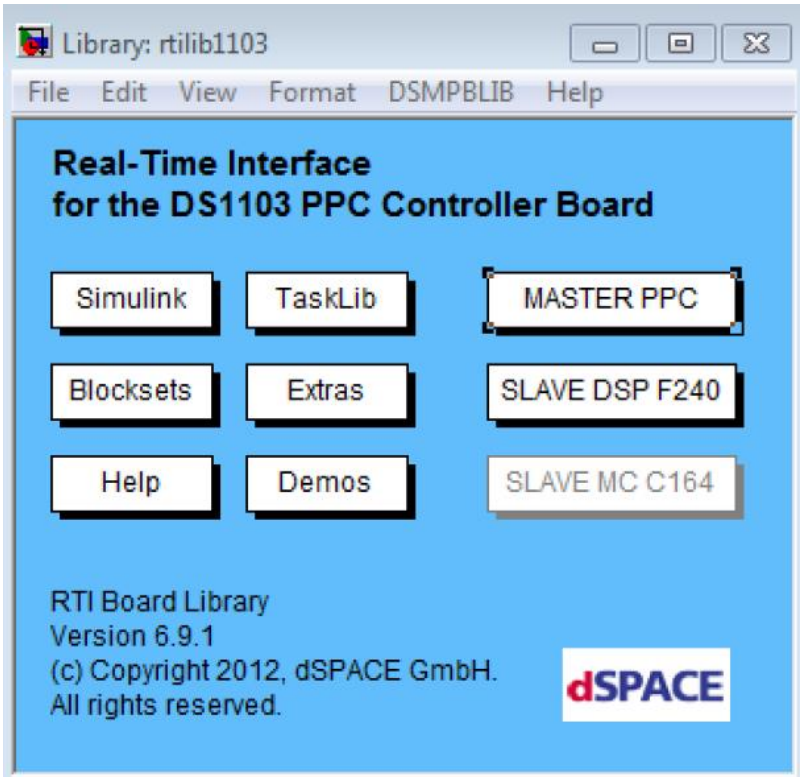
1. Automation and control systems
2. Control of power electronic converters
3. Variable speed drives
4. Robotics
5. Automotive control
6. Active vibration control

C.4 Input/output interfaces

The DS1103 controller board has a variety of input/ output interfaces to meet the needs in a wide range of applications. The details are as following:

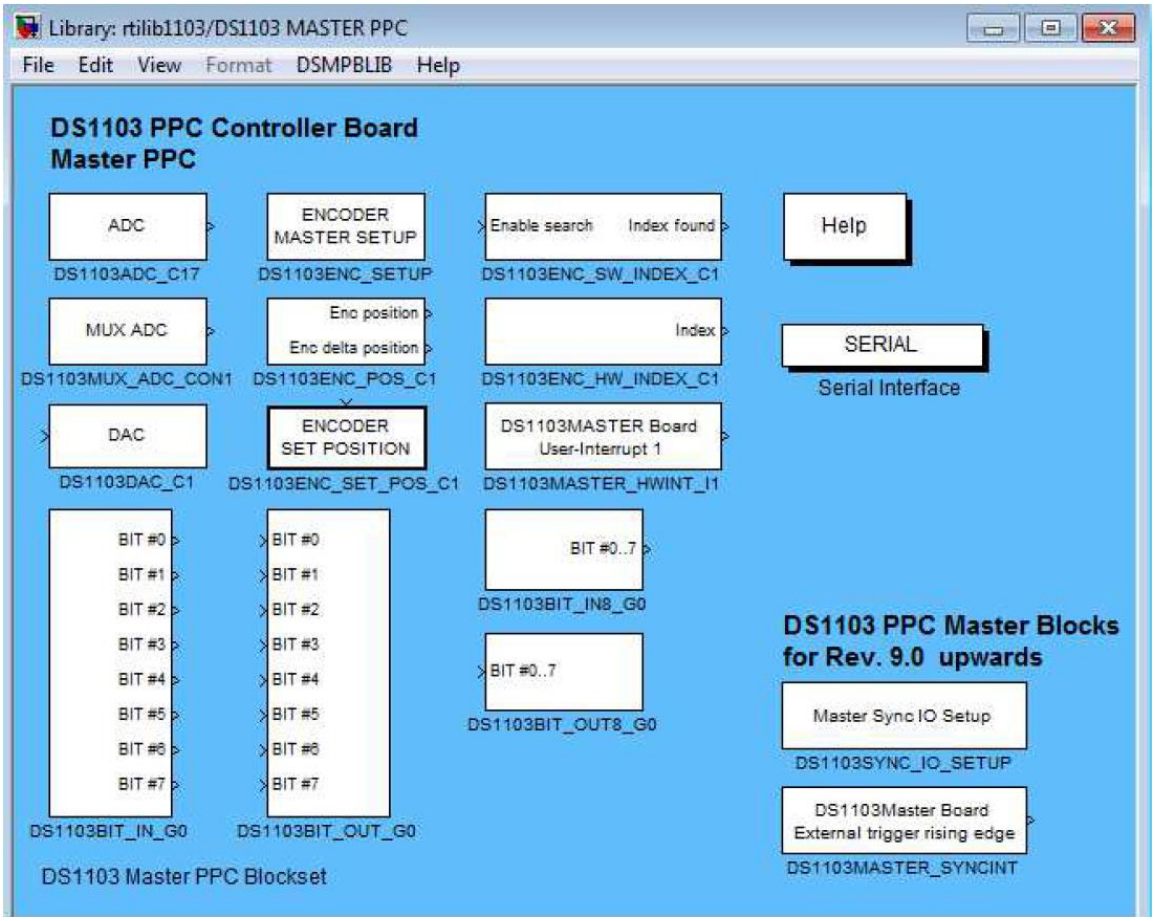
1. 20 A/D channels with 16 bit resolution

2. 8 D/A channels with 16 bit resolution
3. 32 bit digital I/O channels
4. Digital incremental encoder interface (6 channels)
5. Analogue incremental encoder interface (1 channel)
6. Serial interface
7. CAN interface
8. To perform additional I/O task, a slave DSP can be interfaced



C.5 Controller programming with RTI Simulink blocks library

Programming a controller on DS1103 is simplified by RTI (real-time interface) Simulink library. In a very convenient way Simulink models can be programmed on the controller board using the I/O blocks for external connections from this library. It shows the RTI Simulink library. The blocks available in the library enable the user to graphically configure all the I/O interfaces. A view of the RTI master PPC library, which has all the real-time interfacing blocks for the DS1103 controller board.



The various I/O blocks are visible in the figure, such as ADC for analog input signals, DAC for analog output signals, DS1103_BIT_IN block for digital input, DS1103_BIT_OUT block for digital output signals. The description of how to use these blocks is also provided. The help documentation can be accessed from the main RTI library. For the work done in this thesis, mainly the analog I/O interfacing was required. Thus the ADC, MUX_ADC and DAC blocks were used.

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Publications

1. Hybrid Islanding Detection Method for Inverter Based Distributed Generation System (Accepted: 42th IECON Conference Florence, Italy)

2. Reliability Evaluation of Composite Power Systems Considering Impact of Electric Vehicles and Plug-in Hybrid Electric Vehicles. (Accepted: 42th IECON Conference Florence, Italy)

3. Direct Control of Three-Phase Smart Load for Neutral Current Mitigation (Submitted: 19th INMIC Conference, Pakistan)

4. Novel Smart Load Control Based on Fuzzy Logic for Voltage Regulation. (Submitted: 9th GCC Conference Bahrain)

5. Optimization of the Daily Operation of Hydro Power Plant, Coupled with Compress Air Storage. (Submitted: 9th GCC Conference Bahrain)