CURRENT-CONTROLLED CURRENT-CONVEYOR BASED ANALOG NONLINEAR FUNCTION SYNTHESIZER

BY

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This thesis, written by Saad Radhi Al-Abbas under the direction his thesis advisor and approved by his thesis committee, has been presented and accepted by the Dean of Graduate Studies, in partial fulfillment of the requirements for the degree of **MASTER OF SCIENCE IN ELECTRICAL ENGINEERING.**

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To

My Father,

Mother,

Wife,

Brothers,

Sisters

&

Professors

For their patience and encouragement

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All praise and thanks for **Almighty Allah** who gave the ability and power to complete this research successfully.

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LIST OF ABBREVIATIONS

CCCII	:	Second Generation Current-Controlled Current-Conveyor
CCII	:	Second Generation Current-Conveyor
OTA	:	Operational Transconductance Amplifier
MOS	:	Metal Oxide Semiconductor
CMOS	:	Complementary Metal Oxide Semiconductor
BJT	:	Bipolar Junction Transistor
FS	:	Function Synthesizer
PWL	:	Piecewise Linear
HT	:	Hyperbolic Tangent
SPICE	:	Simulation Program with Integrated Circuits Emphasis
RRMS	:	Relative Root Mean Square
ASP	:	Analog Signal Processing
VLSI	:	Very Large Scale Integrated

ABSTRACT

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Thesis Title : Current-Controlled Current-Conveyor Based Nonlinear Function Synthesizer

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In this research, a new CMOS analog function synthesizer building block has been proposed and realized. The proposed approach is based on approximating a second generation current-controlled current-conveyor CCCII nonlinear input-output characteristic by a Hyperbolic Tangent function, and generating multi-harmonics of $tanh$ function by controlling the biasing current of the CCCII. The weighted sum of the generated tanh functions can realize many complex arbitrary nonlinear functions. The circuit was simulated using PSPICE with 0.18 μm CMOS Process Technology, and works with $\pm$0.75 V low power supply. The proposed function synthesizer features wide dynamic range, simple structure of CCCII, low power consumption, and reasonable relative root mean square error.

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يحتوي هذا البحث على تصميم وبناء ومحاكاة دالة تناظرية جديدة تقوم بتوليف الوظائف ذات المواصفات غير الخطية باستخدام تقنية **CMOS** الواسعة الانتشار و المعتمدة في تصميم الدوائر الاكترونية في العصر الحديث. تقوم الدالة المقترحة بتقريب وتوليف العديد من الوظائف ذات العلاقة غير الخطية المعقدة بين مدخلاتها ومخرجاتها, والتي لا يمكن توليفها بالطرق التقليدية المقترحة في البحوث السابقة. يعتمد عمل هذه الدالة على خاصية ناقل التيار المبرمج **CCCII** غير المثالية تحت شروط معينة والتي تماثل بدرجة كبيرة الدالة الرياضية المشهورة دالة الظل القطعي (**HT**) **Hyperbolic–Tangent**.

تقوم فكرة عمل هذه الدائرة الإلكترونية أولا على تقريب خصائص الدخل والخرج في ناقل التيار المبرمج بدالة الظل القطعي (**HT**) و من ثم تقوم دائرة عاكسة التيار باكساب دالة الظل القطعي (**HT**) قيمة ربح إيجابي أو سلبي. وفي المرحلة الأخيرة, تجمع التيارات الخارجة من مضخم تيار الربح لتكوّن وتولّف وظائف غير خطية معقدة جدا. تمتاز دائرة الدالة التناظرية المقترحة بمزود طاقة منخفض الجهد و دائرة إلكترونية بسيطة و قدرة على تقريب الدوال غير الخطية المعقدة لنسبة جيدة جدا من الدقة و تمتاز أيضا باستهلاك طاقة قليلة مقارنة بالوظيفة المعقدة التي تقوم هذه الدائرة المقترحة بإنجازها.

درجة الماجستير في العلوم

جامعة الملك فهد للبترول والمعادن

الظهران – المملكة العربية السعودية

مايو 2014 م

CHAPTER 1

INTRODUCTION

1.1 Motivation

Analog signal processing (ASP) represents an important area of analog integrated circuits analysis and design, which covers many different applications. One of the most important parts in the ASP is the function synthesizers which generate very useful mathematical relationships between inputs and outputs. There are versatile application fields with the function synthesizer circuits, especially in telecommunication, medical equipment, hearing devices, disk drivers, instrumentations, communication, neural networks, display systems, and classification algorithms that can be achieved by synthesizing Gaussian function as an example [1].

Analog nonlinear function synthesizer's circuit's topologies have been developed over the years to have attractive features and specifications like; synthesizing more than one function simultaneously, programmability, simple circuitry structure, compatibility with digital VLSI system, wider dynamic range, less number of transistors, low power supply, synthesized function accuracy, low power consumption, independency of process variations, and high operation frequency [1]. All of these features bring the challenges to

design a new analog nonlinear function synthesizer circuit satisfying most of these trends and requirements.

Currently, most of recent researches and publications are concentrating on designing analog function synthesizers that shall be suitable for low-voltage low-power CMOS realization to be compatible with portable applications and to be integrated with CMOS mixed-mode VLSI technology. Moreover, current-mode approach is highly recommended because of its high performance, compared with its voltage-mode counterpart, in terms of bandwidth, circuit complexity, signal independency of variations, and supply voltage improvements.

Over the last 4 decades, the realization of analog FS circuits have been designed utilizing wide library of electronic elements and devices, such as diodes, linear resistors, MOSFETs, BJTs, Op-Amps, OTAs, and CCCIIs. All of these approaches have been used extensively based on their linear/nonlinear input-output relationships.

However, although CCCII offers interesting high performance properties as a versatile current-mode active device, there have been very few publications utilizing the CCCII nonlinear characteristics to develop and realize new analog FSs [2, 3].

1.2 Goal of Research

The ultimate goal of this research is to implement and simulate a new CMOS analog nonlinear function synthesizer that is capable to synthesize any arbitrary complex nonlinear functions utilizing only CMOS transistors technology that is compatible to be integrated with mixed mode VLSI technology and suitable for portable power applications.

This goal can be achieved by using the nonlinearity characteristics of the CCCII and approximating this nonlinear relationship by a well-known mathematical function called hyperbolic-Tangent function. This property of CCCII will lead to very interesting opportunity to realize a general nonlinear function circuit which can synthesize any arbitrary nonlinear functions.

1.3 Thesis Organization

In chapter 2, categorization of different approaches have been utilized to build up a function synthesizer is presented. After that, the nonlinearity characteristics of a CCCII is introduced and discussed in chapter 3. Also, the approach to implement the desired function synthesizer is proposed, PSPICE, and Monte-Carlo simulations results were carried out and discussed in details. Finally, a conclusion exploiting the advantages of the proposed approach with summarized results is given in chapter 4.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In the literatures surveys, many functions with nonlinear input/output transfer characteristics have been synthesized. These proposed functions are, but not limited to, square, square-root, exponential, logarithmic, trigonometric (sine, cosine, tangent), Gaussian, special complex nonlinear functions, and hyperbolic tangent functions.

The technology that models such mathematical nonlinear functions has been grown over the years since 70's, from using diodes, and BJTs transistors to utilizing the MOS transistors that are compatible to be integrated with Mixed-Mode VLSI technology.

The approaches utilized to realize analog nonlinear function synthesizers can be classified into five categories as follows:

1- Piecewise Linear and Nonlinear Approximations.

2- BJT and MOS Differential Pairs Approach.

3- Trans-linear Loop Principle Approach.

4- Taylor Series Expansion Approach.

5- Nonlinearity characteristics of Devices and Analog Building Blocks.

2.2 Piecewise Linear and Nonlinear Approximations

In this technique, the desired nonlinear functions can be approximated by a series of linear or nonlinear segments that follow the changes of the function. The piecewise linear approximation (PWL) is based on the first order or linear equation as given:

$$y = 1 + x \tag{2.1}$$

Therefore, the segments generated by PWL are linear and the accuracy is highly depending on the number of segments used to approximate a nonlinear function. There are many publications in the literature exploiting this approach [4, 5, 6, and 7]. An improved current-mirror circuit has been exploited to synthesize arbitrary nonlinear functions is presented in [6]. This approach is based on utilizing the linear transfer characteristics of current-mirror with two break points feature as shown in Fig. 2.1.

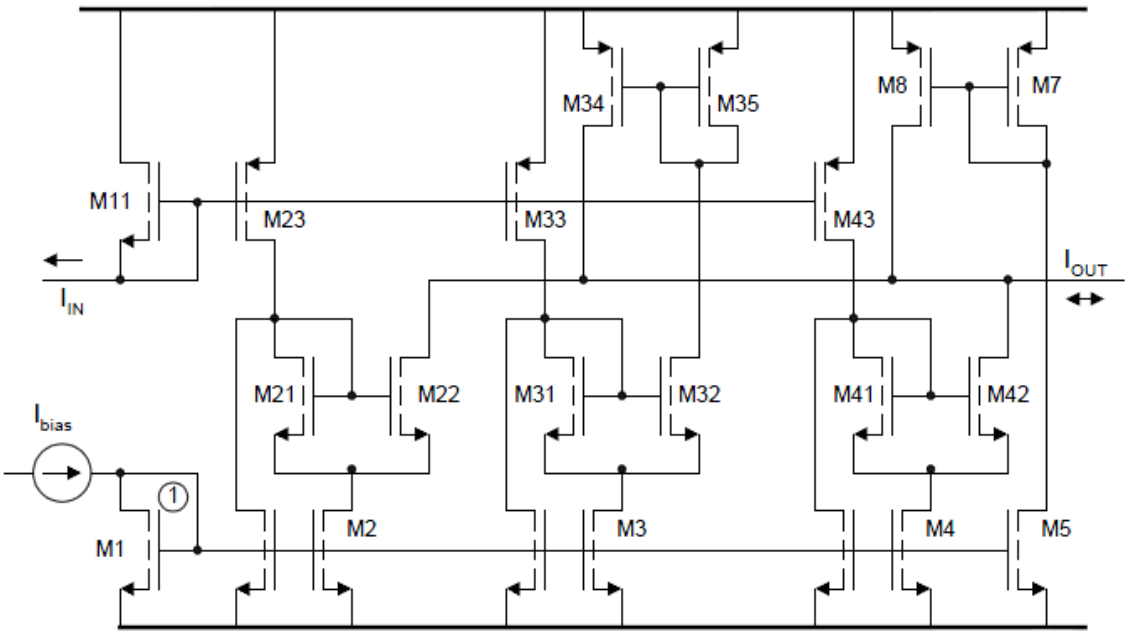


Figure 2.1: Improved Current-Mirrors Combinations introduced in [6]

Several current mirror cells can be combined to approximate any arbitrary functions [6]. Another proposed circuit has been presented in [7] to synthesize an arbitrary analog function by elementary current-mode circuits in which each produces one segment of the required function. However, approach in [6,7] suffers from major sources of error contains; PWL approximation, no strategy to identify breakpoints and the segment slopes, current mirror mismatch, and large number of segments (bulky circuit) to achieve high accuracy of approximation [7].

On the other hand, the nonlinear piecewise approach presented in [8, 9] is based on generating nonlinear segments which makes the accuracy of approximation much better than corresponding PWL approach. Nonlinear transfer characteristics of current mirror analog building block has been presented in [8] to synthesize and approximate any arbitrary analog functions but with main disadvantages of very bulky circuitry block, process variation dependency, and low accuracy. Another published work used second-order approximations (see Eqn. 2.2) to approximate hyperbolic tangent function by generating nonlinear segments [9].

$$y = a_0 + a_1 x + a_2 x^2 \tag{2.2}$$

2.3 Differential-Pair Approach

Another synthesizing technique is to use the concept of transistor differential pair structure using BJTs or MOS transistors. Many analog function synthesizers based on the differential pair approach have been proposed in the literatures [10, 11, 12, and 13]. In [10], an array of BJT differential pairs with one transresistance amplifier proposed to synthesize the sine function. Every differential pair represents a hyperbolic tangent function with different angles, and the combination of these differential pairs can approximate a sine function with accuracy error of 5% [10]. In early 80's, Gilbert proposed a new universal analog trigonometric function synthesizer building block that can generate sine, cosine, tangent, secant, cosecant, and their inverses [11]. This approach was based on differential pair principle implemented by BJT transistors as illustrated in Fig. 2.2. The proposed circuit used to generate only the sine function, and the differential pair used to produce the angle differences needed to synthesize the remaining trigonometric functions [11].

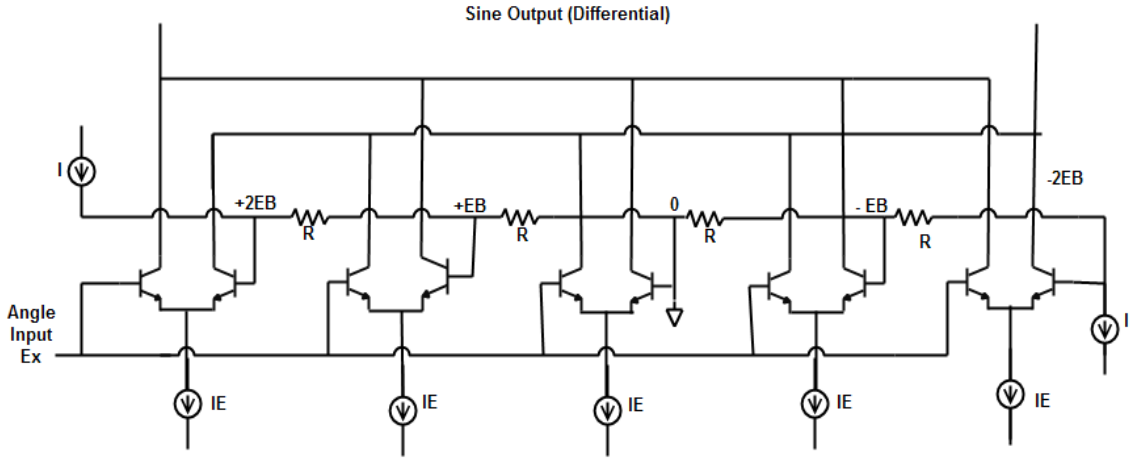


Figure 2.2: BJT Differential Pair Circuit Proposed in [11]

Differential pair approach exploiting MOS transistors was proposed in [12]. The MOS transistor square-law characteristic used to realize a monolithic function synthesizer. This approach can synthesize sine function which is independent of temperature and process variations [12]. An interesting approach utilizing a rigorous mathematical theoretical result to implement a nonlinear function approximation was proposed in [13]. The fundamental relationships used to implement the circuit are as follows:

$$\Omega_n(x) = a_n \left\{ \tanh \frac{nx+\Delta}{2} - \tanh \frac{nx-\Delta}{2} \right\} \tag{2.3}$$

And

$$f_n(x) = \sum_{j=1}^{N} b_j \, \Omega_n(x - t_j) \tag{2.4}$$

The hyperbolic tangent function has been generated by using MOS transistors differential pairs working in weak inversion mode, and the combination of the different angle hyperbolic tangent functions can be utilized in synthesizing complex nonlinear functions [13].

2.4 Translinear Loop Approach

Since it has been proposed in 1975 by B. Gilbert, Translinear loop principle [14] has played an important and useful role in electronic circuits developments, and it has been a very powerful technique that has been utilized over the decades to establish,

enhance, and develop new analog CMOS circuits and specially in synthesizing analog nonlinear functions. A number of circuits have been proposed in [15, 16, 17, 18, and 19] to approximate useful nonlinear function synthesizer system based on Translinear Loop principle.

A trans-linear programmable analog nonlinear function synthesizer was proposed in [15]. Its principle of approximation is based on approximating the nonlinear functions using rational functions. The proposed circuit was implemented by BJT transistors in the form of current mirror scheme and can synthesize exponential, and cosine functions with less than 5 % error for limited dynamic range [15]. Another approach in [16] has proposed a CMOS basic cell utilizing the traditional class AB current mirror and its modification to realize square function. This square cell can be configured to generate 6 mathematical functions which are squaring, multiplier, divider, logarithmic, exponential, and raise-to-power functions [16].

A very useful mathematical function -hyperbolic tangent function- has been approximated to a high degree of accuracy as presented in [17]. The proposed circuit was implemented based on realizing Padè Rational Approximation Equation (2.4) using trans-linear loop technique [17].

$$f_s(x) = \frac{3sx}{3+s^2x^2} \tag{2.5}$$

The proposed circuit used six MOS transistors working in sub-threshold region as shown in Fig. 2.3. It is not programmable circuit since aspect ratios values need to be routine changed to have hyperbolic tangent function with different harmonic.

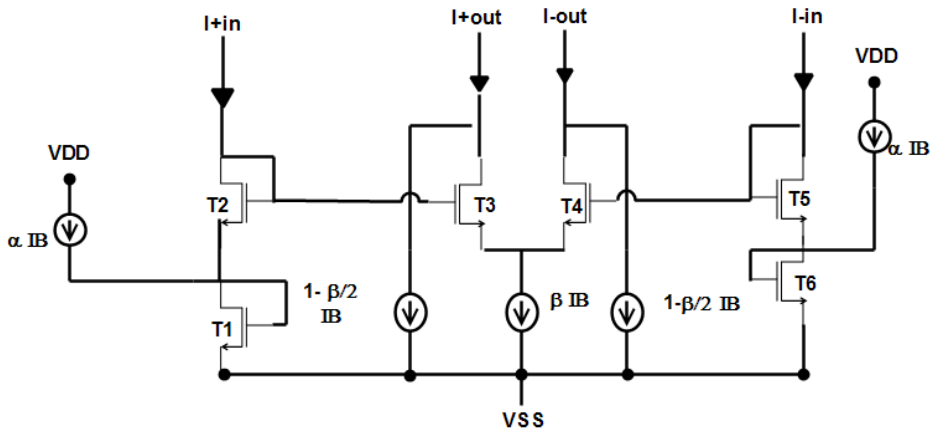


Figure 2.3: Hyperbolic Tangent Approximation Circuit proposed in [17]

A proposed computational analog block was presented in [18]. It is used to realize three mathematical functions which are squaring, harmonic mean calculation, and vector summing and can be programmed to realize these functions [18]. The trans-linear loop proposed circuit-with eight NMOS transistors-is shown in Fig. 2.4. The aforementioned functions can be realized by programming this circuit using three current sources [18].

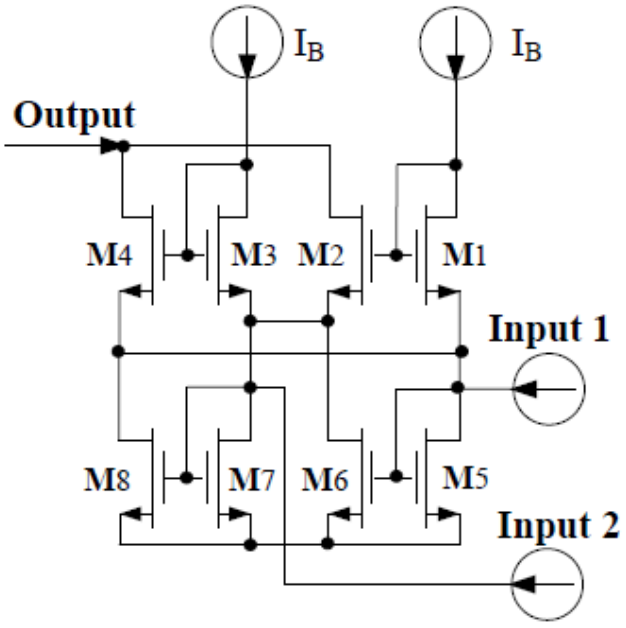


Figure 2.4: MOS Current-Mode Translinear Loop presented in [18]

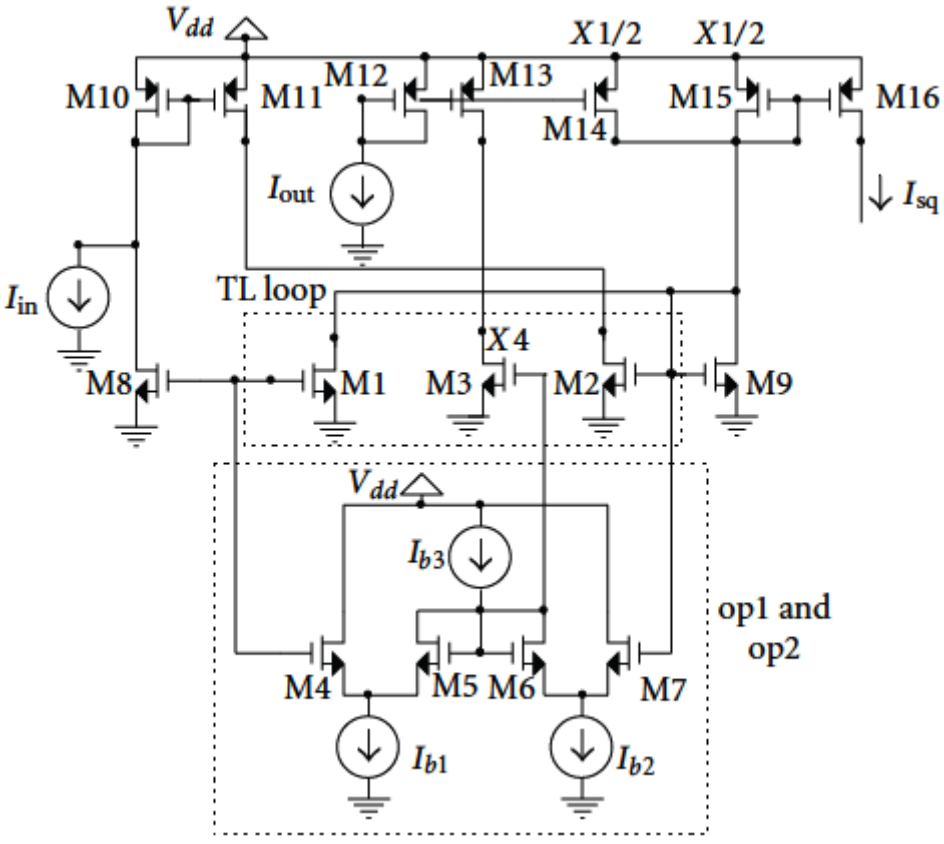


Figure 2.5: Proposed Circuit with two Translinear Loops presented in [19]

Euclidean Distance function was synthesized in [19] using 2 stacked MOS trans-linear loops. This proposed circuit can be used as matching pattern classifier circuit as shown in Fig. 2.5. It is composed of two-quadrant squarer and divider blocks [19]. The MOS transistors operate in strong inverted saturation region. It features low supply voltage (0.9 V), two-quadrant input current, and 1 % error.

2.5 Taylor Series Expansion Approach

Taylor Series Expansion approach is a very useful technique that has been used over years to synthesize and approximate a number of nonlinear mathematical functions that cannot be achieved using the aforementioned approaches. Many analog function synthesizers based on Taylor series approximation method have been proposed [20, 21, 22]. The Taylor Series Expansion formula is given by;

$$y = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + \cdots + a_nx^n, \quad n = 0,1,2,3, \ldots \quad (2.6)$$

$a_0 - a_n$, are arbitrary constant values. These combinations of power factor elements can be used to realize any nonlinear functions combinations. The accuracy of this approach is dependent on the number of terms used in approximations. That is as the number of terms increased, the accuracy of approximation improved.

In [20], a CMOS current-mode analog function synthesizer circuit was proposed. The proposed principle is based on approximating the desired function by using the first three terms of its Taylor series expansion. The approximated terms can then be added with

different weights to obtain large number of nonlinear functions [20]. The proposed circuit was implemented to realize Taylor series expansion of the form

$$y = a + bx + cx^2 \tag{2.7}$$

The proposed circuit is based on the traditional class AB current mirror and its modification to provide current squarer as shown in Fig. 2.6.

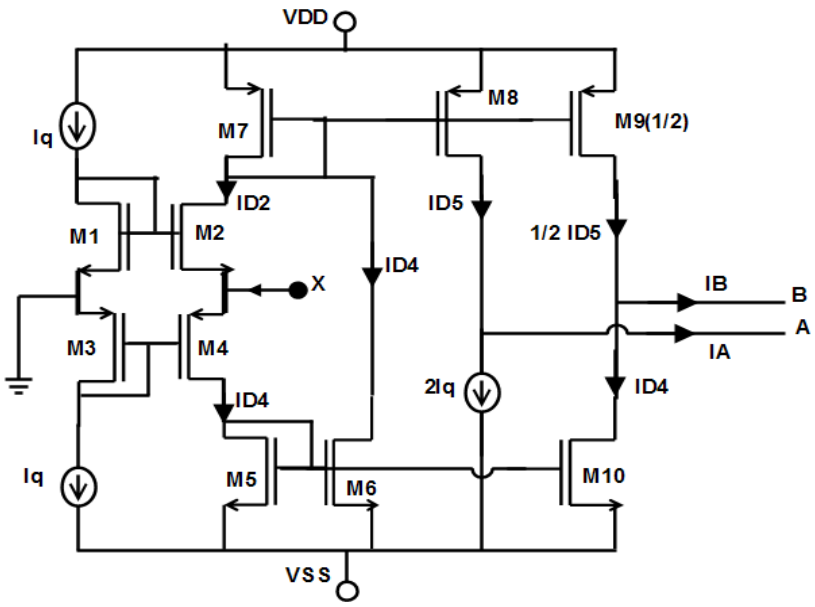


Figure 2.6: the Modified Traditional class AB Current Mirror utilized in [20]

This proposed circuit could realize 18 different mathematical functions but with very limited dynamic range, large power supply of $\pm 10\ V$, and low accuracy for high dynamic ranges.

An improved approach related to the proposed approach in [20] was proposed in [21]. The key idea of this research is to build up on the idea in [20]. That is to approximate various nonlinear functions by their seventh-order Taylor series expansion as follows

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + a_5 x^5 + a_6 x^6 \quad (2.8)$$

The new achievement in this approach was to generate higher order terms without using current multipliers which will give negative impacts on the circuit features if used [21]. That could be obtained by successive use of square cells and the square-difference identity given by:

$$[(A + B)^2 - (A - B)^2] = 4AB \quad (2.9)$$

This technique can simultaneously realize 32 different standard mathematical functions and features less than 5% error for very low dynamic range and large power supply of $\pm 2\,V$. However, the proposed circuit in [20, 21] cannot be programmed to generate arbitrary nonlinear functions.

In a recent publication [22], a current-mode CMOS analog programmable arbitrary function synthesizer circuit has been presented. The proposed circuit is based on approximating an arbitrary function using its seventh-order Taylor series expansion given by:

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3 + a_4 x^4 + a_5 x^5 + a_6 x^6 + a_7 x^7 \quad (2.10)$$

To establish the programmability of the proposed circuit, the published research in [22] has used a current-mode multiplier circuit proposed in [23] as squaring cell, which used to generate high-order terms, since it affords the programmability feature by a voltage source as shown in Fig. 2.7. The principle of operation of the proposed circuit is as follows; each term of the Taylor series expansion is approximated by a current-mode basic building block. The weighted output currents of these blocks are added to form the

desired analog nonlinear function [22]. This approach has 25 MHz frequency of operation, power consumption of 0.6 mW for each SU, limited dynamic range of $[-0.4, +0.4]$, very bulky circuitry implementation, and low approximation accuracy.

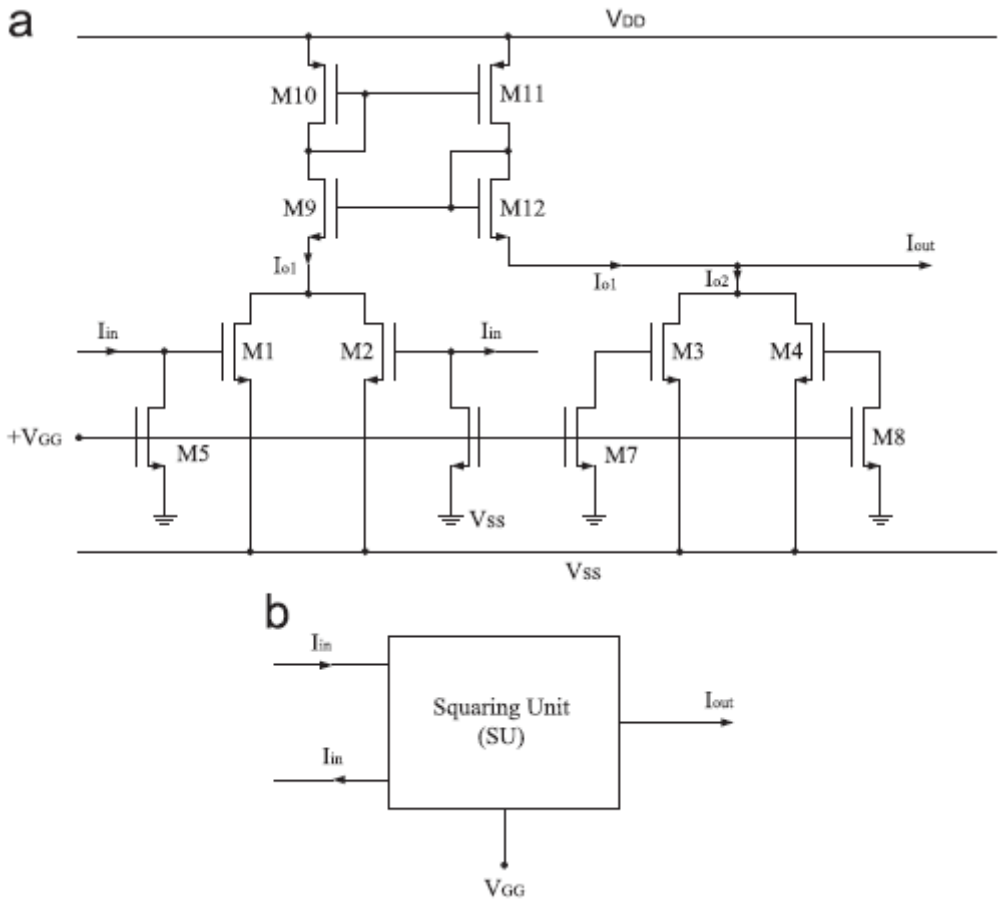


Figure 2.7: (a) CMOS Realization of the Squaring Unit utilized in [22] (b) Symbol of the Squaring Unit.

2.6 Nonlinearity Characteristics of Devices and Analog Building Block Approach

The nonlinearity input-output transfer characteristics of basic electronic devices (diodes, BJTs, and MOSFETs), and analog building blocks (Op-Amps, OTAs, and

CCIIs) have been used over the years to realize function synthesizer circuits. Diodes which have exponential transfer characteristics was utilized to produce piecewise linear segments exploited in synthesizing nonlinear functions as proposed in [24]. The nonlinear characteristic of BJT was utilized to design triangle-to-sine wave converters and some basic trigonometric functions in [25]. Moreover, the square-law and exponential nonlinear characteristics of MOSFETs operated in saturation and sub-threshold region, respectively, have been exploited to realize analog function synthesizer as illustrated in [26, 27, 28]. Also, current conveyors and operational transconductance amplifiers have been used to synthesize some functions using piecewise linear approximation technique [29, 30].

A combination of the exponential characteristics of MOS transistors in weak inversion and the square characteristics in strong inversion has been introduced in [31] to realize the Gaussian functions. The proposed circuit is composed of 5 CMOS transistors to synthesize the square and the exponent functions as shown in Fig. 2.8 [31]. It works only in one quadrant with relative error of 2%.

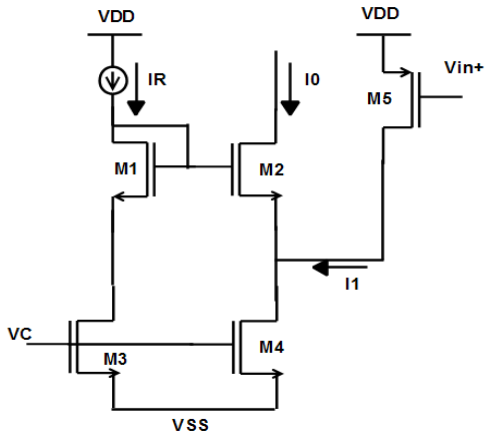


Figure 2.8: Gaussian Function Circuit Proposed in [31]

Unlike aforementioned Gaussian function synthesizer proposed in [31], an improved accuracy Gaussian function generator has been introduced in [32]. The proposed circuit is based on a new approximation function that is able to fourth-order match the Gaussian function as given bellow:

$$g(x) = -\frac{8}{1+(x/2)} + \frac{1}{1+x} - 3x + 8 \tag{2.11}$$

The author has proposed a new squaring cell that can be utilized in realizing the rational approximation function. The proposed circuit composed of 2 squaring cell with 4 current mirrors. It has very limited dynamic range, and operates in only one quadrant.

Operational Transconductance Amplifier OTA has been first utilized as a basic analog building block to synthesize nonlinear functions in [33]. In this research, many basic functions in analog signal processing field have been realized using OTAs such as multiplier (using 2 OTAs), divider (using 3 OTAs), and square rooter (using 3 OTAs), exponentiation (using 5 OTAs) [33]. In addition, piecewise linear approximation has been realized by using OTAs and diodes to generate the required segments. Another approach in [34] has proposed a Triangular/Trapezoidal function generator circuit based on CMOS OTAs. The proposed circuit can configure the slope, height, and horizontal position of the Triangular/Trapezoidal function [34].

Second Generation Current conveyors have also been used to synthesize nonlinear functions [30, 2]. A circuit based on CCII has been designed to synthesize the nonlinear chaotic system parameters [2]. In addition, CCII has been utilized as a nonlinear basic element to realize many nonlinear computational functions such as multiplier, divider,

squarer, square rooter, and used to realize piecewise linear approximation technique as illustrated in [3]. Table 2.1 summarizes approaches reported in the literatures and their results.

Table 2.1: Characteristics of Previous Analog FS proposed in Literatures.

Ref.	**CMOS Tech.**	**Power Supply**	**Power Consmp.**	**Chip Area** $(\mu m)^2$	**BW (MHz)**	**# of Functions**
[31]*	$3\ \mu m$	N/R	N/R	70000	N/R	single
[20]	N/R	$\pm 10\ V$	N/R	324	$25\ MHz$	Multi
[34]	$0.5\ \mu m$	$\pm 1.5\ V$	$0.3\ mW$	4842	N/R	Multi
[17]	$0.35\ \mu m$	$1\ V$	$0.48\ \mu W$	151	N/R	single
[21]	N/R	$\pm 2\ V$	N/R	126	$25\ MHz$	Multi
[18]	$0.18\ \mu m$	$\pm 0.9\ V$	N/R	99.76	$344\ MHz$	single
[19]	$0.18\ \mu m$	$0.9\ V$	$< 1\ mW$	> 1152	$4\ MHz$	single
[32]	$0.18\ \mu m$	$1\ V$	$1\ mW$	N/R	$> 300\ KHz$	single
[1]	$0.18\ \mu m$	$1\ V$	N/R	7.56	$> 300\ KHz$	single
[22]	$0.5\ \mu m$	$\pm 1.5\ V$	$> 5.4\ mW$	12200	$< 25\ MHz$	Multi

* Experimental Results.

N/R: Not Reported.

2.7 Problem Statement

The literature approaches realizations described in previous sections are suffering from one or more of the following drawbacks:

1) The use of bipolar transistors, or MOSFETs operating in weak inversion which results in low speed of operation.
2) The need to use of piecewise linear approximations to approximate the required nonlinear function.
3) Only one or two functions can be realized at a time.
4) The need of special functions, mostly rational functions, to approximate the desired nonlinear functions, which leads to design complex circuit realizations.
5) The use of Taylor series expansion needs many terms to obtain very good accuracy, resulting in large chip area.
6) Use of large voltage supply which is not suitable for portable power applications.
7) Approximation accuracy is limited for small normalized input range.

Beside these disadvantages of the aforementioned approaches, no approach was proposed in order to investigate the feasibility of realizing a generalized transfer function which is not represented by a standard mathematical function except one presented in [20] by M. Abuelma'atti, which can approximate any arbitrary nonlinear functions.

The major intention of this research is to implement an arbitrary nonlinear function synthesizer circuit utilizing CCCIIs nonlinearity characteristics with the following attractive features:

1) Use of CMOS transistors which is compatible with the mixed-mode VLSI technology.
2) Can realize many arbitrary nonlinear functions.
3) CMOS transistors operate in saturation region, exhibiting relatively high frequency of operation.
4) No parameter optimization required.
5) Low supply voltage which is suitable for portable power applications.
6) Approximation is valid for wide normalized input range.
7) Small occupied chip area compared with respect to previous approaches.
8) Work in four-quadrant ranges.

CHAPTER 3

ANALOG NONLINEAR FUNCTION SYNTHESIER

BASED-ON CURRENT CONTROLLED CONVEYOR

3.1 Introduction

Second generation current conveyor CCII, well known active device, has been considered as the most attractive current-mode analog building block since it was introduced by A. Sedra and K. Smith in 1970 [35], that is because of its preferred advantages over other analog circuits like Op-Amps. CCIIs feature very useful characteristics, which are interesting in high frequency analog signal processing applications, such as high bandwidth (speed), large dynamic range, low power consumption, and high linearity. Since 1996, an improved version of CCII has been introduced by A. Fabre [36], called second generation current controlled current conveyor CCCII. In in [36], the parasitic floating intrinsic resistance at port X (R_x) which can be controlled electronically by adjusting the bias current is exploited to advantage.

CCCIIs have been implemented in literatures by two approaches; Differential-pair [37, 38, 39], and/or Translinear cell [36, 40, 41, 42, and 43] structures. Most CCCII designs preferred the differential-pair structure since it is suitable to be input-stage of CCCII than

those in translinear structure to enhance the voltage-following performance [44]. The main contributions with differential-pair implementations are to enhance the voltage and the current transfer accuracy, increase the input dynamic range, minimize the offset tracking error, and increase the operation frequency [45].

The ideal operation of CCCII consists of two combinations; current-follower between terminals X and Z, and voltage-follower between terminals X and Y. These two ideal functions of CCCIIs can be described as a three-port network given by the following matrix equation [36]:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.1}$$

This matrix can be formulated in equations form as follows:

$$\begin{aligned} v_x &= v_y + R_x i_x \\ i_z &= \pm\, i_x \\ i_y &= 0 \end{aligned} \tag{3.2}$$

The high performance CCCIIs are characterized by very low input impedance at port X, very high input impedance at port Y, and high output impedance at port Z as illustrated in Table 3.1.

Table 3.1: CCCII Ideal Node Impedances.

Input/Output Node	Impedance Level
X	0
Y	∞
Z	∞

Fig. 3.1 shows the translinear-based CMOS CCCII core circuit which is composed of two n-channel MOS and two p-channel MOS transistors [42, 43]. The current flowing in M_1 and M_3 is equal to the bias current (I_B), while the drain currents passing M_2 and M_4 are I_2 and I_4, respectively. These four complementary MOS transistors represent the voltage-following function.

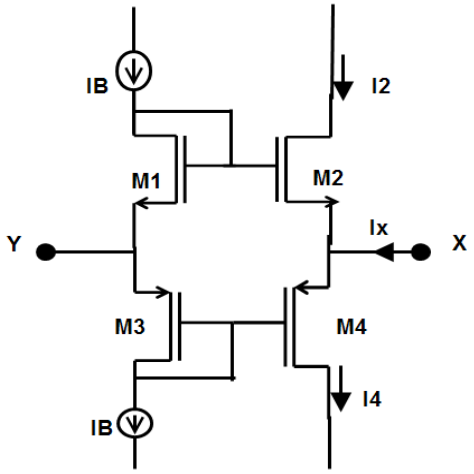


Figure 3.1 CMOS CCCII Translinear Cell Circuit [42, 43]

To extract a relationship between the intrinsic impedance and the bias current, the translinear principle can be applied between gate-source voltages of the four transistors and can be characterized as

$$V_{GS1} - V_{GS3} = V_{GS2} - V_{GS4} \tag{3.3}$$

The input voltage can be expressed as

$$V_{XY} = V_{GS1} - V_{GS2} = V_{GS3} - V_{GS4} \tag{3.4}$$

And by taking KCL at node X, the current relationship is

$$i_x = I_4 - I_2 \tag{3.5}$$

After manipulating previous matrix (3.1), and equations (3.4), and (3.5) mathematically, a relationship between the bias current (I_B) and the intrinsic impedance (R_x) can be extracted as illustrated in [44] and given as follows:

$$R_x \cong \frac{1}{\sqrt{2I_B C_{ox}}\left(\sqrt{\mu_p\left(\frac{W}{L}\right)_P}+\sqrt{\mu_n\left(\frac{W}{L}\right)_N}\right)} \tag{3.6}$$

In this relationship, the intrinsic impedance is inversely dependent on the bias current. And this gives the advantage for controlling the input-output characteristics of CCCIIs by tuning the bias current.

Moreover, the dynamic range for translinear-based structure can be estimated as [44]

$$-\sqrt{\frac{I_B}{\frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}}} \leq V_{XY} \leq \sqrt{\frac{I_B}{\frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}}} \tag{3.7}$$

This is symmetric if and only if the NMOS and PMOS transconductance are matched.

3.2 Translinear CMOS CCCII and its Nonlinear Characteristic

The proposed CCCII utilized in this thesis is the classic translinear-based structure class AB CMOS CCCII [44], displayed in Fig. 3.2. This is a very simplified implementation of the CCCII circuit consisting 4 CMOS transistors M_1-M_4 which build the core translinear cell circuit, another 4 CMOS transistors M_{10}-M_{13} serving as current mirroring circuit, and the remaining $M_5 - M_7$ are introducing the biasing circuit. The translinear combination transistors are functioning as voltage-follower circuit between node Y and X, while current mirror transistors perform the current conveying from node X to Z. These two functions can be expressed in equations form as mentioned in the previous section in equations (3.2).

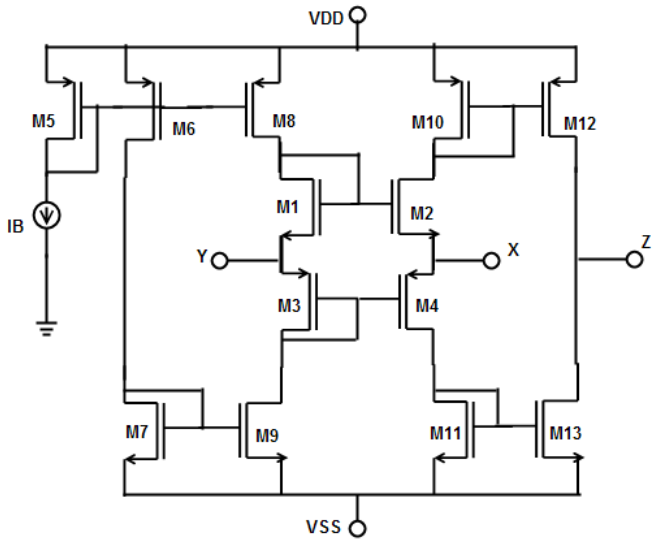


Figure 3.2 Schematic Implementation of CCCII Class-AB based on Translinear Structure [44]

Voltages and currents nodes relationships of the translinear CCCII presented in equation (3.2) are typically formulating the ideal or linear operation of the CCCII; however, that is not the case in practice. CCCII behaves linearly only for restricted conditions on limited range of v_y and i_x values. [46, 47] In natural mode, CCCIIs exhibit considerable nonlinear relationships in their voltage-follower, and current conveying combinations. This nonlinear relationship, between input and output of the translinear class AB CCCII, has been reported and studied by many researches in the literatures [46, 47, 48, 49, and 50] in order to recognize its sources. It was found that the current mirror circuit of the CCCII causes a nonlinearity which will directly enter into the transfer function of the CCCII [48]. The complementary class-AB current mirror and the translinear voltage-follower introduce the nonlinearity of the CCCII in two forms [48, 49]:

- The channel-length modulation error of mirroring transistors,
- The mismatch of the mirror transistors.

That can be illustrated by analyzing a single current mirror with an input transistor M_1 and an output transistor M_2, using Shichman-Hodges [48] model and conventional transistor parameter and voltage notation, leads to

$$\begin{aligned} v_{GS} &= V_{T1} + \sqrt{\frac{2i_{D1}}{\beta_1(1+\lambda_1 v_{DS1})}} \\ i_{D2} &= \frac{\beta_2}{2}(v_{GS} - V_{T2})^2(1 + \lambda_2 v_{DS2}) \\ &\cong \left(1 + \frac{\Delta\beta}{\beta}\right) i_{D1} - \Delta V_T \sqrt{2\beta i_{D1}} \end{aligned} \tag{3.8}$$

Where $\Delta V_T = V_{T2} - V_{T1}$ and $\Delta\beta = \beta_2 - \beta_1$ are identified as the threshold-voltages and the transconductance parameters differences, respectively. It is obvious from equation

(3.8) that the mismatch transistors error due to threshold-voltage differences has noticeable nonlinearity contribution. Though transistor transconductance parameter mismatch does not introduce any nonlinearity in a single current mirror as appears in equation (3.8), this will be very noticeable in the complementary class-AB current mirror where NMOS and PMOS currents are subtracted from each other. [48]

A simulation of the input-output transfer characteristics of the proposed translinear CCCII illustrates this kind of nonlinearity as shown in Fig. 3.3.

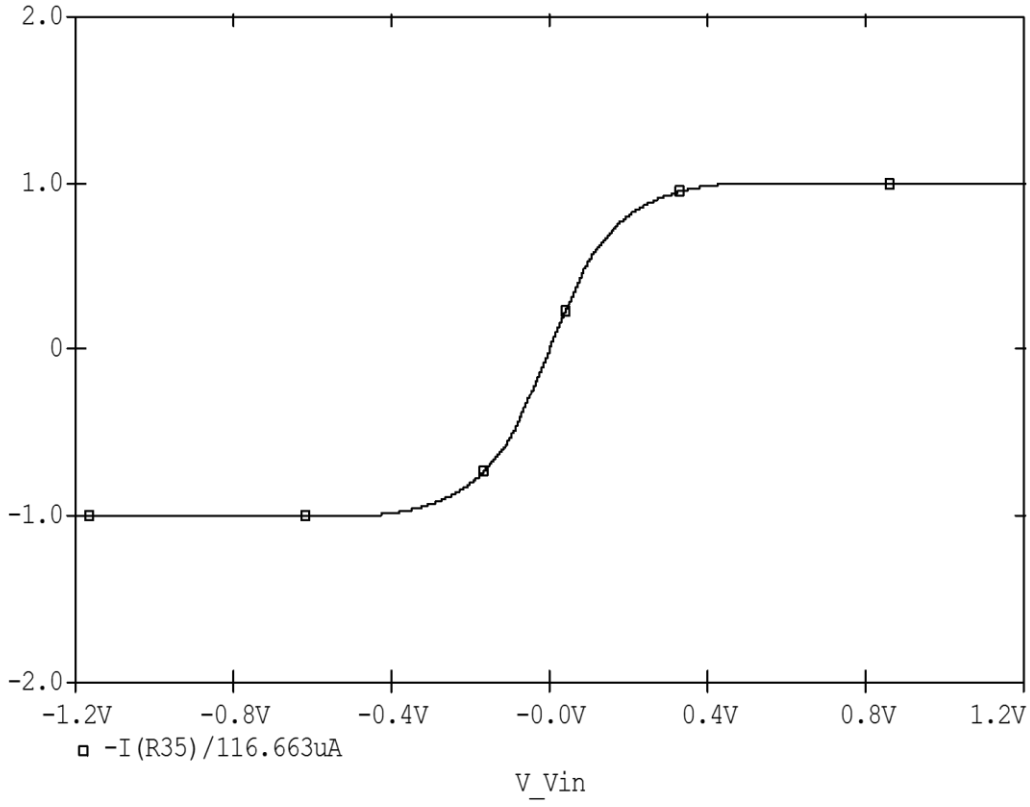


Figure 3.3: Simulation of Normalized Output Current at port Z vs. Input voltage of the translinear CCCII of Fig. 3.2.

This kind of input-output nonlinearity characteristics of the proposed translinear CCCII, shown in Fig. 3.3, is a Hyperbolic-Tangent like shape and can be seen as an interesting

advantage of the translinear CCCII instead of avoiding its use by many reported researches available in the literatures.

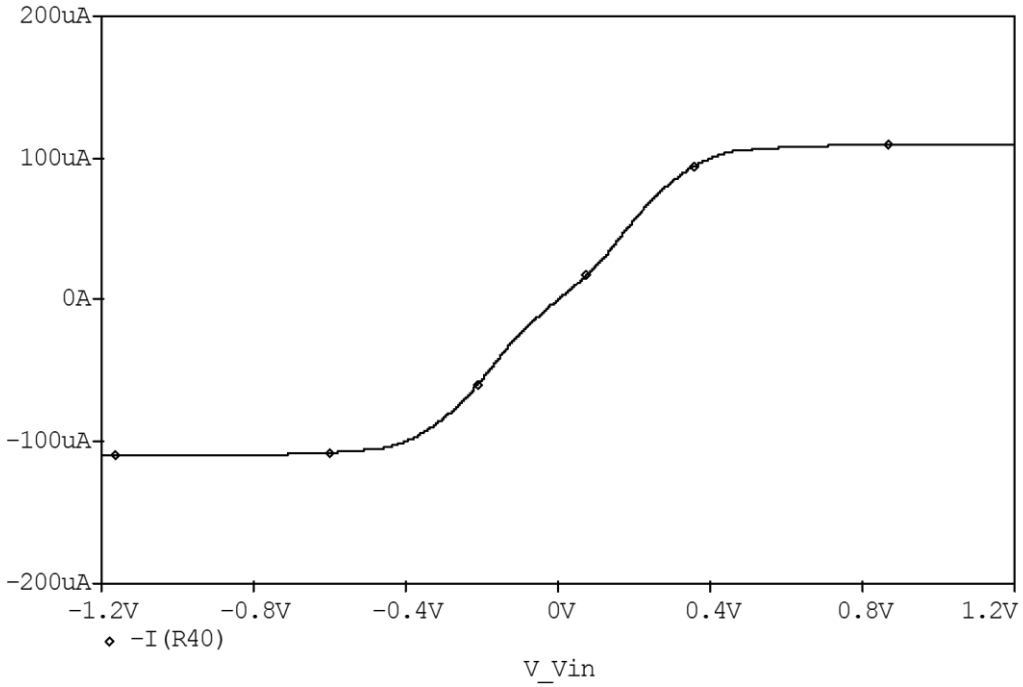


Figure 3.4: Simulation of Normalized Output Current at port X vs. Input voltage of the translinear CCCII of Fig. 3.2.

It appears from Figs. 3.3 and 3.4 that the tanh-shape nonlinear characteristics are contributed by the inherent nonlinearity of the translinear loop and the currents mirrors nonlinearity resulting from the channel length modulation effect.

In addition to the nonlinearity advantage of the CCCII, electronically controlling property can be achieved by adjusting the bias current I_B which leads to produce several Hyperbolic-Tangent functions, so that different values of the biasing current can generate several harmonics of Hyperbolic-Tangent functions without changing the aspect ratios of the CCCII transistors thus, CCCII can approximate $\tanh x$, $\tanh 2x$, or $\tanh 3x$ by adjusting the biasing current values. A simulation of the input-output characteristics of

the CCCII with three different values of the biasing current, shown in Table 3.1 and Fig. 3.5, illustrates this advantage.

Table 3.2: CCCIIs Approximation Using PSPICE Simulation. (Where x is a normalized input voltage $x = \frac{V_{in}}{V_B}$, $V_B = \sqrt{\frac{I_B}{K}}$, $K = K_n \frac{W}{L}$, and $I_o(SPICE\ scaling\ factor) = 118\ uA$).

CCCII circuit #	Biasing Current (I_B)	$tanh$ Function Approximation
CCCII #1	220 μA	$I_{out} = I_o \times tanh(x)\ \mu A$
CCCII #2	120 μA	$I_{out} = I_o \times tanh(2x)\ \mu A$
CCCII #3	22 μA	$I_{out} = I_o \times tanh(3x)\ \mu A$

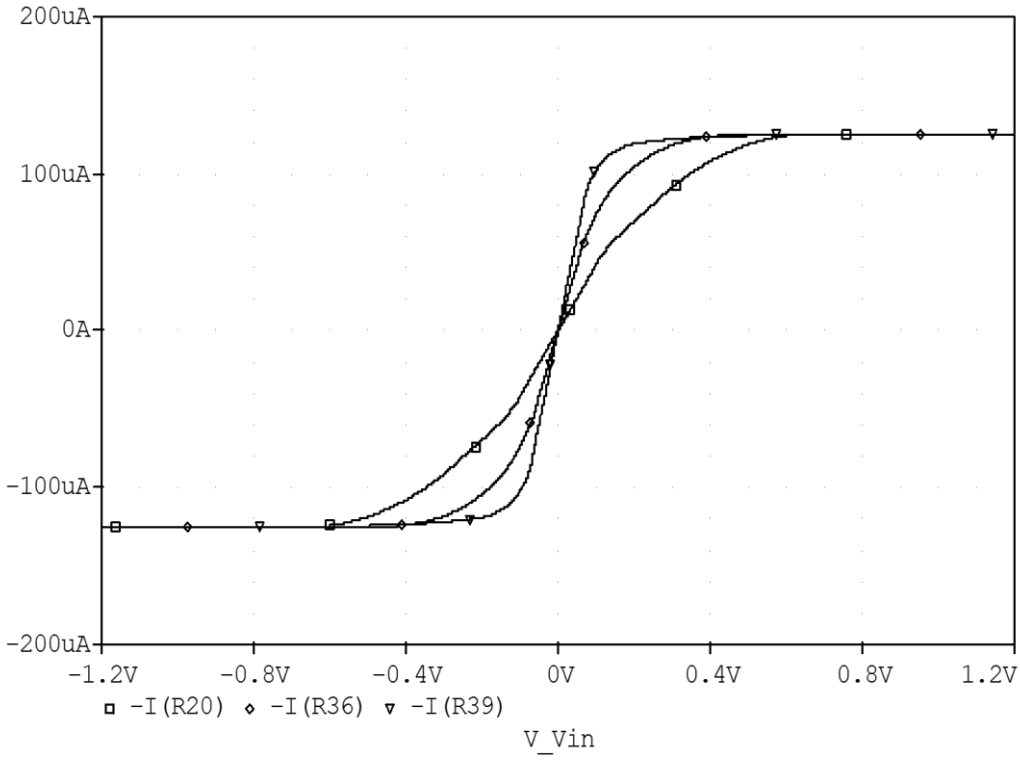


Figure 3.5: Simulation of the Controllability Property of the CCCIIs by Adjusting different biasing currents I_B = 22, 120, and 220 μA.

3.3 Proposed Circuit Realization

The proposed analog function synthesizer realization is based on the nonlinearity nature of the translinear class-AB CCCII, shown in Fig. 3.2. Assuming that a nonlinear function can be represented as the sum of several tanh functions, then

$$\begin{aligned} I_z &= I_s \sum_{n=1}^{N} a_n \tanh nx \\ &= I_s \times \{a_1 \tanh x + a_2 \tanh 2x + a_3 \tanh 3x + \cdots\} \end{aligned} \tag{3.9}$$

Where the parameters are defined as follows:

- I_z is the synthesized function current resulting from adding CCCIIs output currents.
- I_s is a scaling current factor from SPICE simulation.
- a_n is an arbitrary current gain.
- N is the number of the CCCIIs used in the analog function synthesizer.
- n is a constant integer: 1, 2, 3, 4, …
- x is a normalized input voltage.

Each tanh function in Eqn. (3.9) can be realized using the circuit shown in Fig. 3.2. This kind of function described in equation (3.9) can synthesize any nonlinear functions, and as the number of HT harmonics term increases, many complex nonlinear functions can be realized and approximated.

The methodology designed to achieve this approach is as follows:

1) Approximate input-output nonlinear characteristics of the translinear CCCII with the mathematical well-known Hyperbolic-Tangent ($\tanh nx$) function.
2) Generating as many as possible of harmonics of the approximated function by changing the bias current I_B, so that each CCCII realizes one harmonic of the HT function such as $CCCII_n \cong \tanh(nx)$, where $n = 1, 2, 3, 4, \ldots$ is the number of CCCIIs
3) Using the traditional class-AB current-mirror amplifier, shown in Fig. 3.6, with arbitrary current gains to weigh the approximated HT functions.
4) Add weighted approximated HT functions together with different harmonics and weights to synthesize interesting and useful arbitrary nonlinear functions as illustrated in Fig. 3.7.

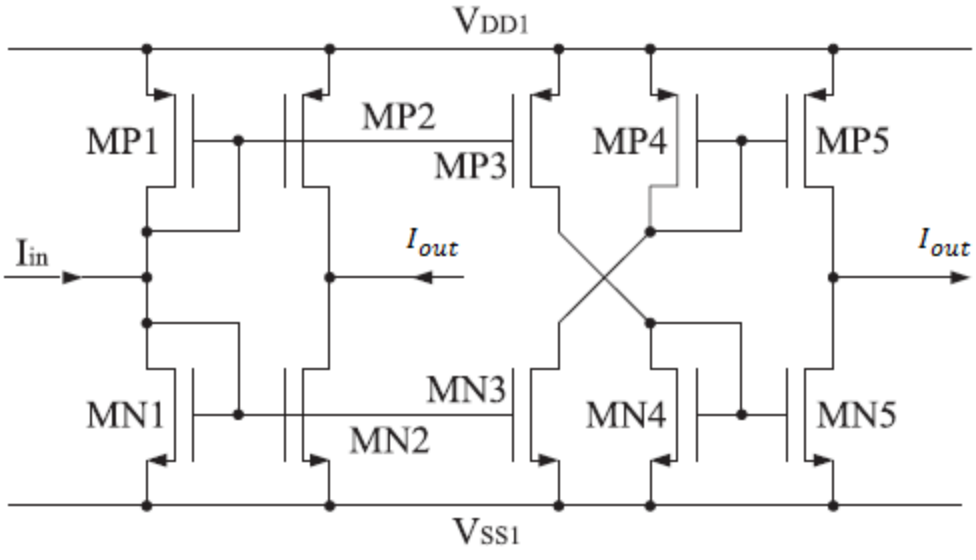


Figure 3.6: Standard Class-AB inverting and non-inverting Current Mirrors.

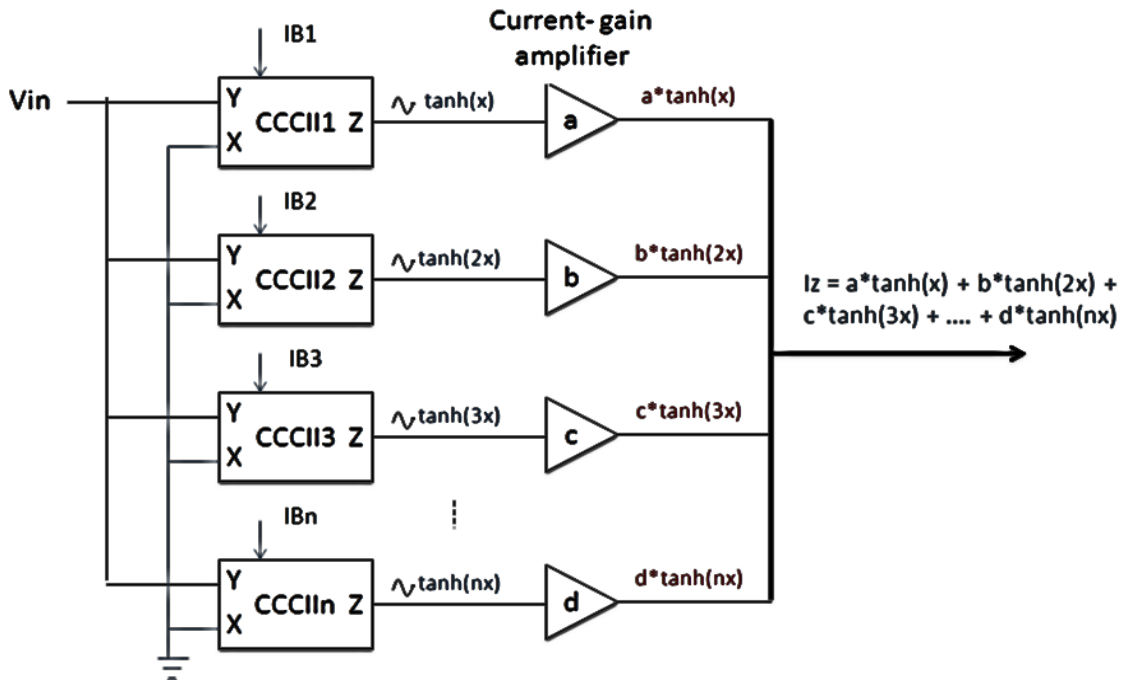


Figure 3.7: Block Diagram of the Proposed FS Based on translinear CCCIIs, where x is the normalized input voltage $x = \frac{V_{in}}{V_B}$.

3.4 Simulation Results and Discussion

To investigate the accuracy of the approximation of the hyperbolic tangent function and the proposed function synthesizer, the circuits of Figs. 3.8, and 3.9 were simulated with the SPICE using BSIM3 TSMC Level-49 0.18 μm CMOS process parameters technology (Appendix-A), and MOS transistor aspect ratio W/L shown in Table 3.3, where W and L are the effective channel width and the effective channel length, respectively, of the MOSFET transistors. The supply voltages $V_{DD} = -V_{SS} = 0.75\,V$, the bias currents $I_B = 22\,\mu A, 120\,\mu A, and\ 220\,\mu A$, and the output currents through load

resistance $R_L = 1.5\,k\Omega$ were monitored. With the input voltage changing between $-0.6\,V$ and $+0.6\,V$.

To measure the accuracy of the approximated results, Relative Root Mean Square (RRMS) technique was used for each approximated function. RRMS equation used is given by:

$$RRMS = \sqrt{\frac{\sum_{n=1}^{N}\left(\frac{y_{sim}-y_{cal}}{y_{cal}}\right)^2}{N}} \tag{3.10}$$

Where,

N is the total number of points used to be compared.

n is an arbitrary number.

y_{sim} is a simulated point by PSPICE.

y_{cal} is a calculated point simulated by MATLAB.

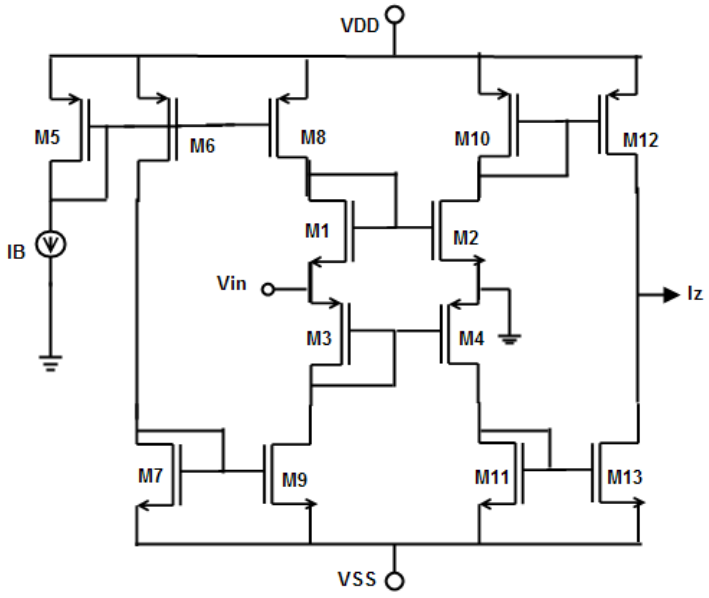


Figure 3.8: Schematic Implementation of the CCCII.

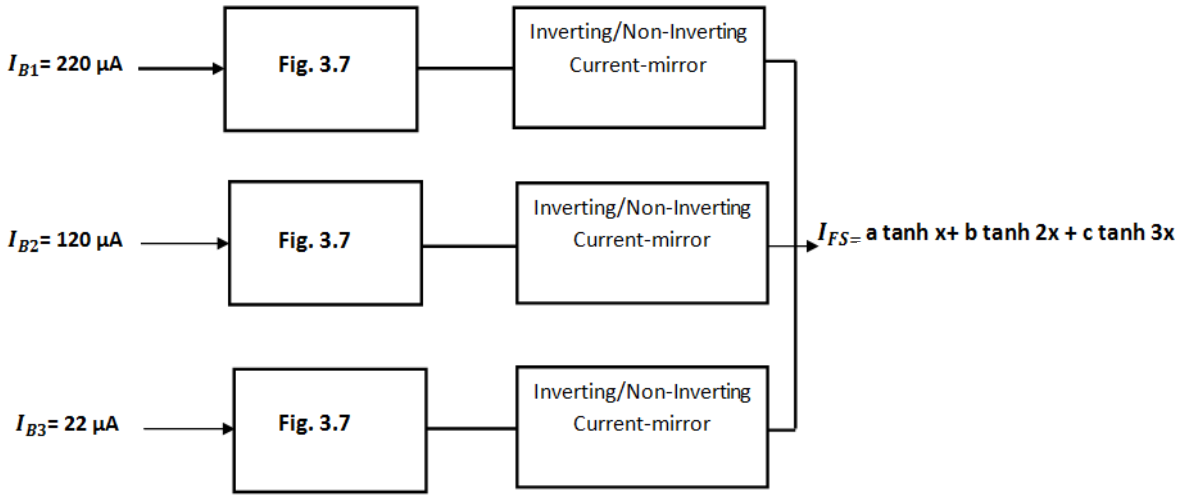


Figure 3.9: Block Diagram of the Simulated Circuit Implementation where I_{FS} is a synthesized function current.

Table 3.3: Dimensions of MOS devices for CCCIIs 1, 2, and 3 of Fig. 3.7

Transistor	W/L
$M_{(1,2,3,4,5,6,8)_{n,p}}$	$0.8\ um/0.5\ um$
$M_{(7,9)_{n,p}}$	$3\ um/2\ um$
$M_{(10,12)_{n,p}}$	$1\ um/1\ um$
$M_{(11,13)_{n,p}}$	$1.5\ um/0.5\ um$

The simulation results for hyperbolic tangent function generator using CCCIIs, and several arbitrary nonlinear functions synthesized by the proposed function synthesizer are reported and discussed in the next sections.

3.4.1 Hyperbolic-Tangent Function Approximation by a CCCII

The CCCII described in Fig. 3.8 was simulated with three bias currents $I_B = 22\ \mu A, 120\ \mu A, and\ 220\ \mu A$ and their results shown in Figs. 3.10, 3.11, and 3.12, respectively. As shown in Table 3.1, with $I_B = 220\ \mu A$ $\tanh x$ function can be approximated with excellent level of accuracy compared to the calculated HT function, with maximum error of 3.2 %, and Relative RMS error equal to 2.74 %. With bias current $I_B = 120\ \mu A$ $\tanh 2x$ generated and exhibiting max. error of 4.7 % and 2.84 % RRMS error. At $I_B = 22\ \mu A$ $\tanh 3x$ was approximated with 5.2 % and 2.42 %, max. and RRMS errors, respectively. As it appears from the results, the circuit can work to approximate very large extended normalized input voltage which is applicable for $-4 \leq x \leq 4$.

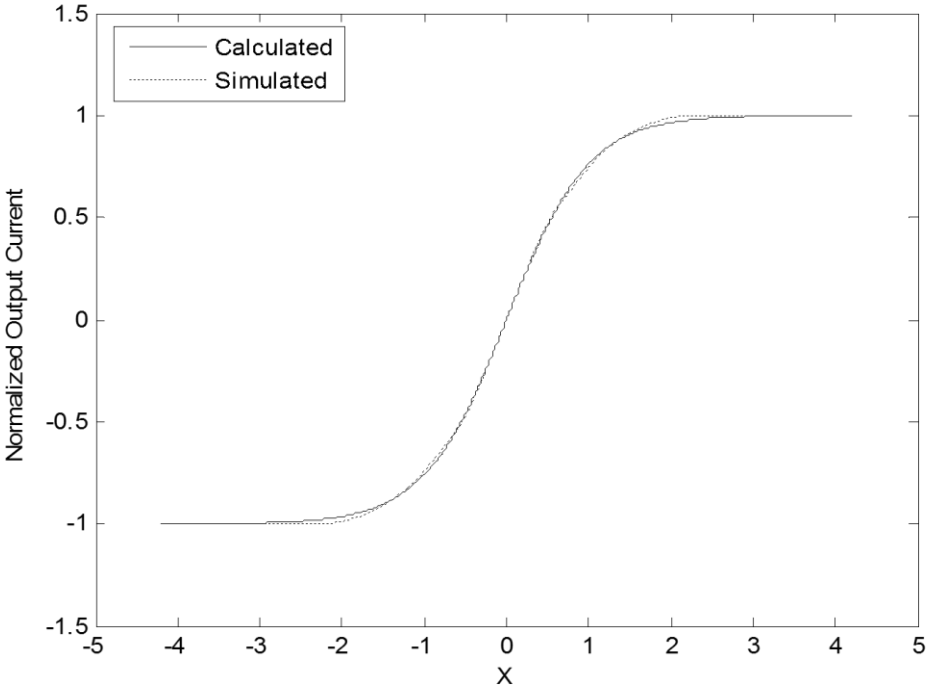


Figure 3.10: Simulated and Calculated $tanh(x)$ with RRMS = 2.74 % error.

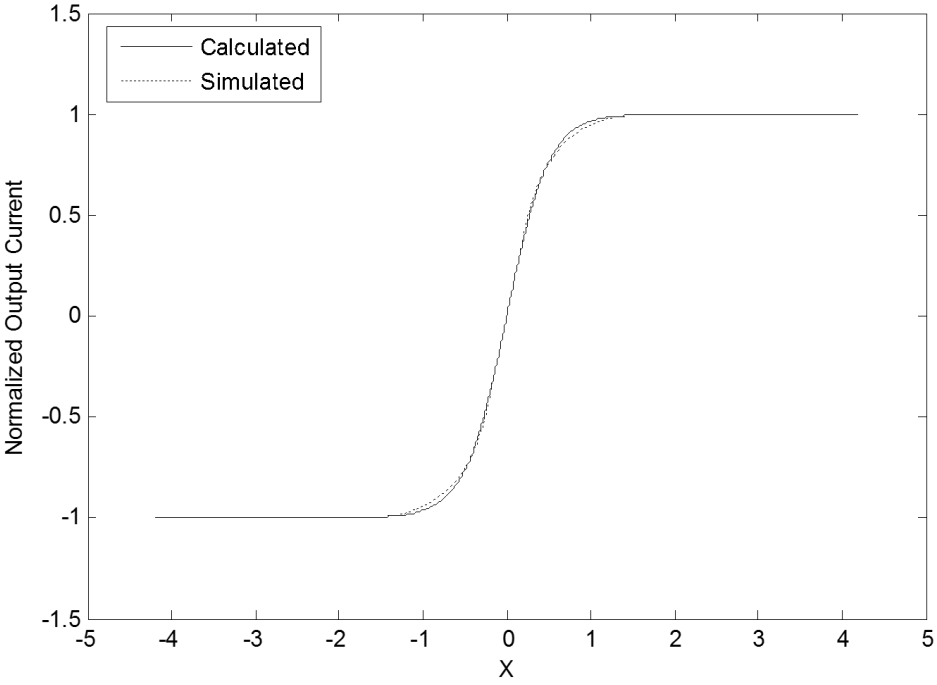


Figure 3.11: Simulated and Calculated $tanh(2x)$ with RRMS = 2.84 % error.

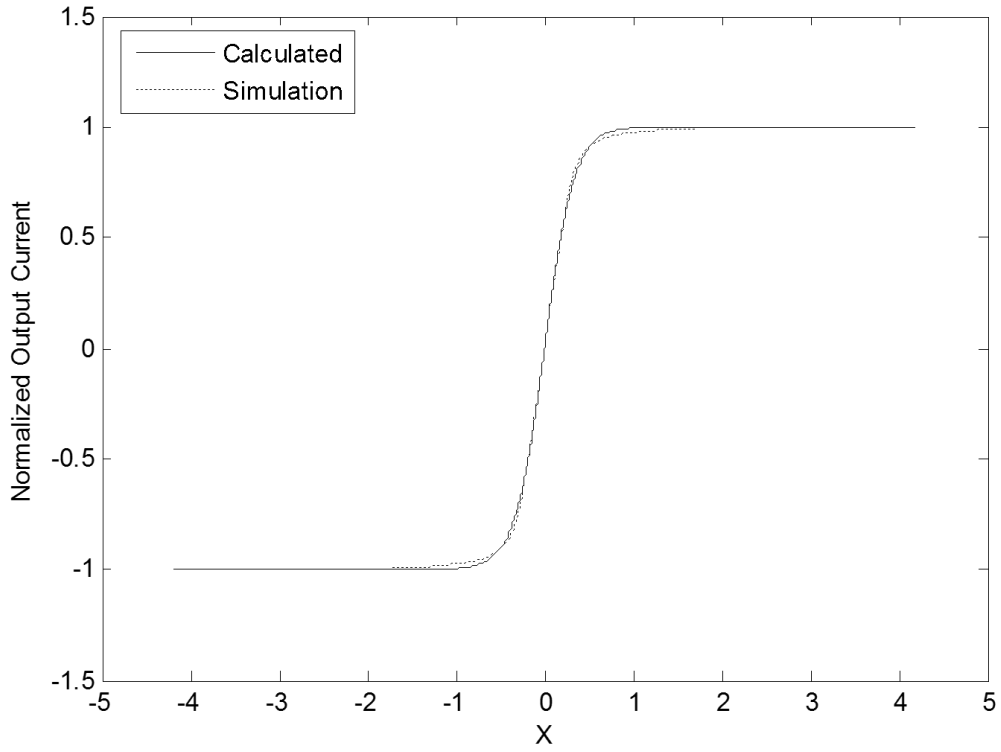


Figure 3.12: Simulated and Calculated $tanh(3x)$ with RRMS = 2.42 % error.

To illustrate the accuracy of the simulated results of Fig. 3.8, a summary of the results given in Table 3.4 showing the level of accuracies for each simulated hyperbolic tangent function.

Table 3.4: Maximum and Relative Errors Approximation.

Realized Function	**Approximation Performance**	
	Maximum Error	**Relative RMS Error**
Fig. 3.9: $\tanh x$	3.2 %	2.74 %
Fig. 3.10: $\tanh 2x$	4.7 %	2.84 %
Fig. 3.11: $\tanh 3x$	5.2 %	2.42 %

3.4.2 Comparisons between Proposed HT Function based on CCCII and Corresponding Digital Implementation Approaches

This section includes comparisons between the last CCCII tanh function approximation approach and the ones proposed in the literatures using digital implementation approaches. The most concerns parameters of comparisons are occupied area by the chip and the speed of operation. These two factors can be improved by analog approach that has been proposed in this research as can be illustrated in Table 3.5. This table summarizes the performance factors (max. error, silicon area, and speed) between the proposed tanh function based on CCCII circuit and other digital approaches described in literatures [51, 52, 53, 54, and 55].

Table 3.5: Comparisons between Analog Hyperbolic-Tangent Function generated by CCCII and others generated by Digital Implementation Approaches.

Ref.	**Technology**	**Max. Error**	**Area** $(\mu m)^2$	**Speed** (MHz)
Proposed	0.18 μm	3.2 %	18.3	1761
[55]	0.18 μm	0.0378	695.22	1052.6
[54]	0.18 μm	0.0401	954.67	478.47
[53]	0.18 μm	0.0361	3646.83	432.9
[52]	0.18 μm	0.0365	9045.94	465.11
[51]	0.18 μm	0.043	32069.83	1.107

This table shows clearly that analog tanh function, generated by CCCII, affords better performance factors than digital approaches, presented in [51-55] in terms of area and speed.

3.4.3 Nonlinear Function Synthesizer simulation

In this section, the proposed analog function synthesizer circuit was investigated in order to confirm its functionality and accuracy. Three arbitrary nonlinear functions were realized and simulated, using the three generated outputs of Figs. 3.10, 3.11, and 3.12. After that, these were weighted with arbitrary gains using three current-mirror circuits of Fig. 3.6. These arbitrary gains are -0.6, -1.2, -2, 0.16, 0.2, and 0.8. The arbitrary nonlinear functions to be simulated are:

$$I_{FS1} = 118 \times (-0.6\tanh(x) + 0.8\tanh(2x) + 0.2\tanh(3x))\ uA \qquad (3.11)$$

$$I_{FS2} = 118 \times (-2\tanh(x) + \tanh(2x) + 0.16\tanh(3x))\ uA \qquad (3.12)$$

$$I_{FS3} = 118 \times (-1.2\tanh(x) + \tanh(2x) + 0.2\tanh(3x))\ uA \qquad (3.13)$$

Where 118 μA is SPICE scaling current. The results are shown in Figs. 3.13, 3.14, and 3.15.

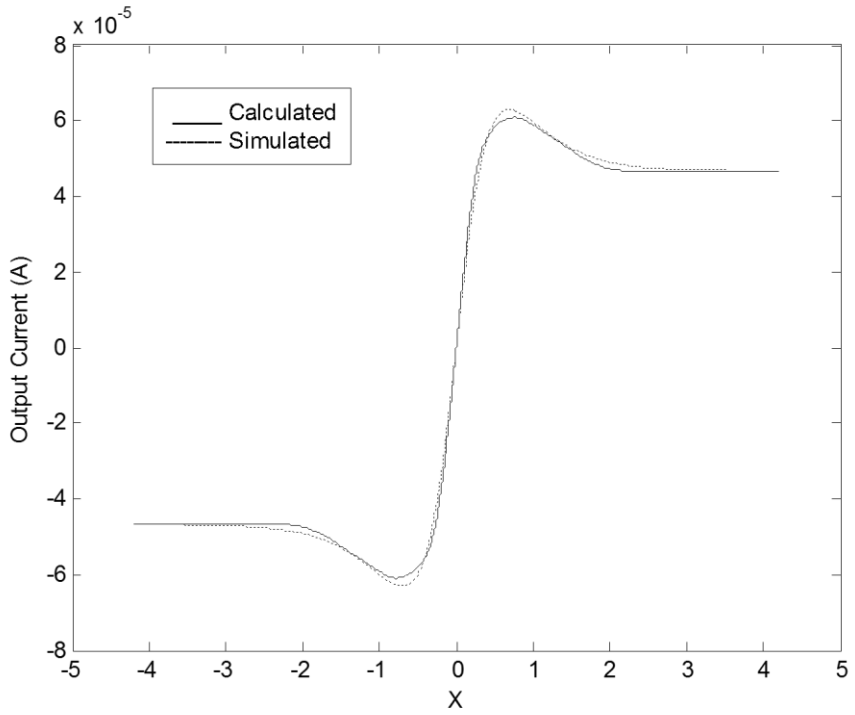


Figure 3.13: Simulated and Calculated Function (3.11) with RRMS = 4.25 % error, where 118 μA is SPICE scaling current.

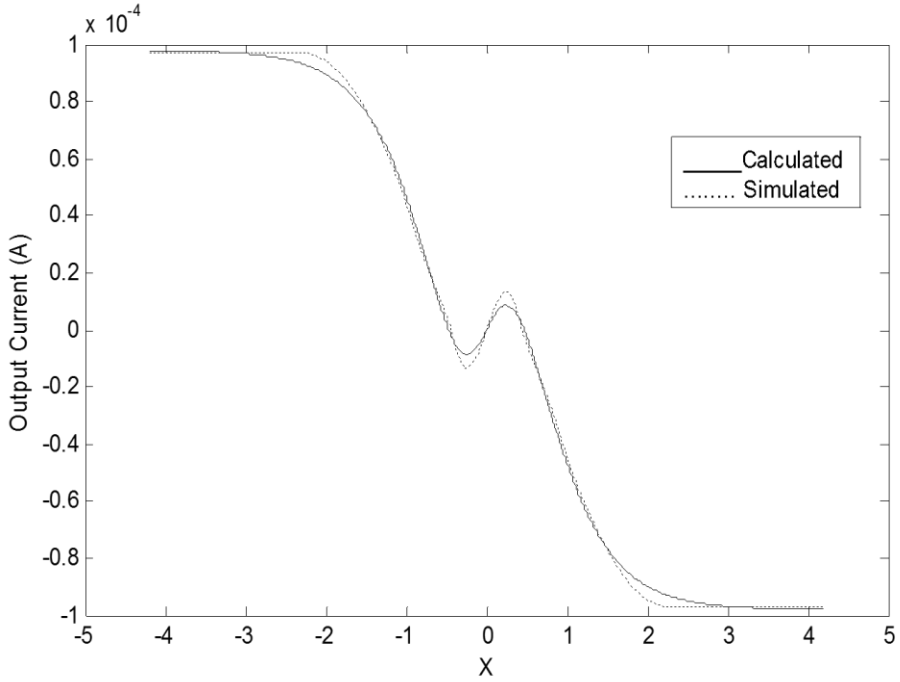


Figure 3.14: Simulated and Calculated of Eq. (3.12) with RRMS = 11 % error.

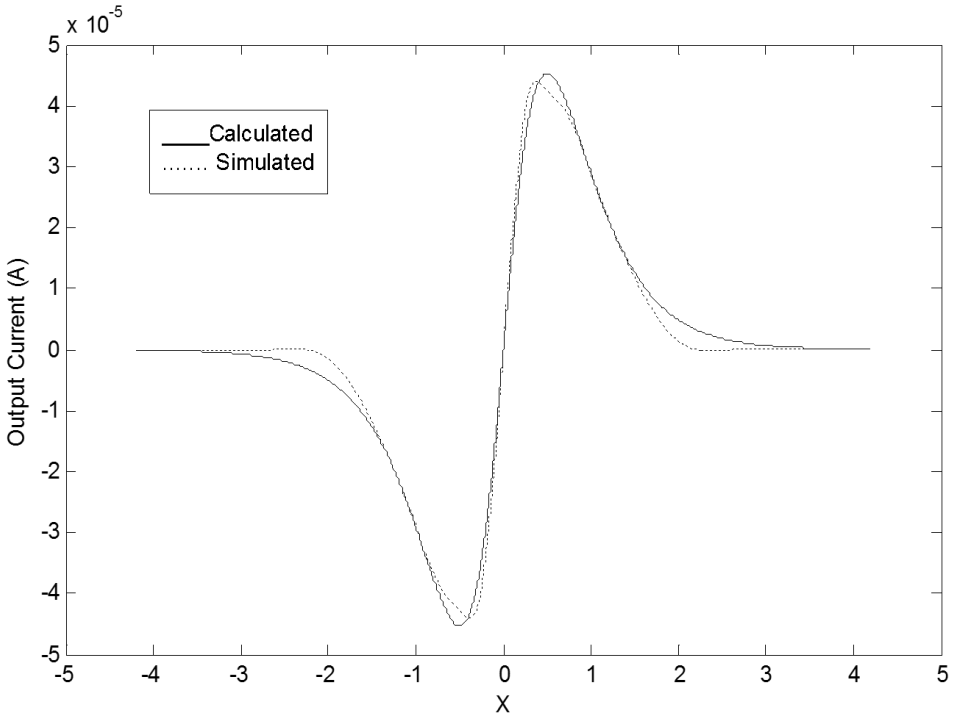


Figure 3.15: Simulated and Calculated Function (3.13) with RRMS = 9.5 % error.

The approximation results in figure 3.13 are good in general with less than 4.25 % RRMS error for full dynamic range -3.5 < x < 3.5. Regarding figure 3.15, the approximation is very good with 9.5% RRMS error for limited dynamic range of -1.6 < x < 1.6. However, this is not the case the results in Fig. 3.14, which produce 11 % RRMS error with dynamic range of -2.5 < x < 2.5. In fact, we can reduce the dynamic range of our function synthesizer to gain very good approximation accuracy.

The results above are affected by two main sources of errors. First, errors come from the CCCII current-mirror circuit. Second, errors introduced by the traditional class-AB current-mirror current-gain amplifier exploiting a nonlinear input-output transfer characteristic. This is because the linear dynamic range of the current gain amplifier is

limited to few 10's of micro-amperes for the input current. This contributes nonlinearities in the analog function synthesizer circuit.

The circuit has around 25 MHz frequency bandwidths, and consumes approximately 5.144 mW of dissipated power. A single CCCII occupied 18.3 $(\mu m)^2$, while the total estimated FS Circuit area is around 458.1 $(\mu m)^2$ as illustrated in Table 3.5.

Table 3.6: Proposed FS Circuit Performance Summary.

Specification	Performance
Process	0.18 μm
Power Supply	$\pm 0.75\ V$
Dynamic Range	Full Range
Power Consumption	5.144 mW
CCCII Bandwidth	1.76 GHz
FS Bandwidth	25 MHz
Total Area	458.1 $(\mu m)^2$

3.5 Monte-Carlo Simulation

To examine the performance of the proposed nonlinear function synthesizer, a Monte-Carlo simulation was carried out. The performance of the arbitrary function $I_{FS} = 118(-0.6\ \tanh x + 0.8\ \tanh 2x + 0.2\ \tanh 3x)\mu A$ for change in temperatures was investigated. The results in Fig. 3.16 show that the performance of the circuit is highly affected by variations in temperature from $15℃\ to\ 35℃$. The difference between

the value of the function at 15℃ and its value at 27℃ is 6.45 μA, which corresponds to 17.45 % of the nominal value at 27℃.

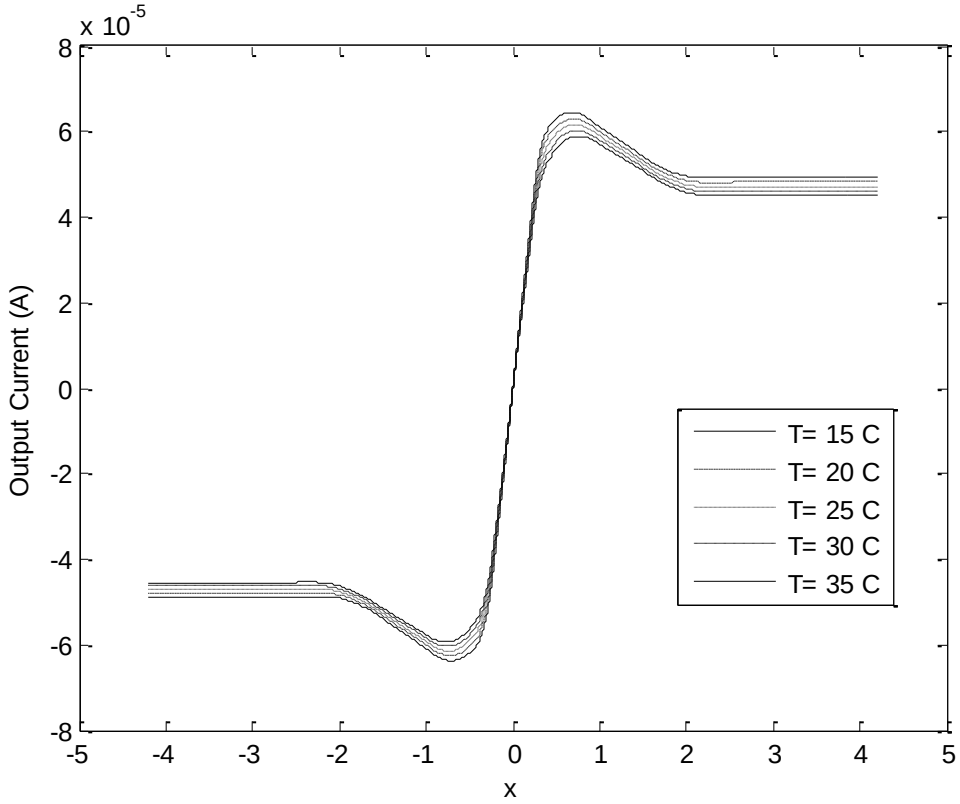


Figure 3.16: Variation of the function in Eq. (3.11) with Temperature.

Inspection of Fig. 3.17 shows that the performance of the arbitrary function given by Eq. (3.11) is excellent and almost not affected by variations in the mobility μ of the transistors when ± 5 % of variations applied.

Fig. 3.18 shows the performance for the same function for changes of ± 5 % in the parameter C_{ox} for all transistors. The results show an excellent performance with variations in this parameter.

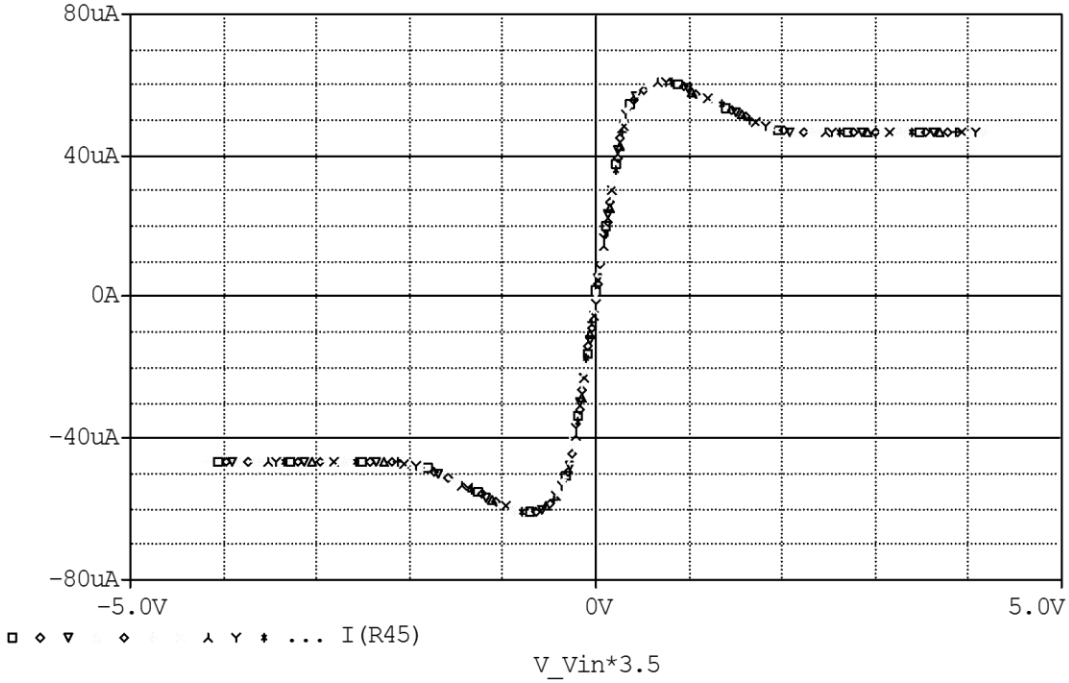


Figure 3.17: Monte-Carlo Simulation of the function in Eq. (3.11) with ± 5 % change in μ of all transistors.

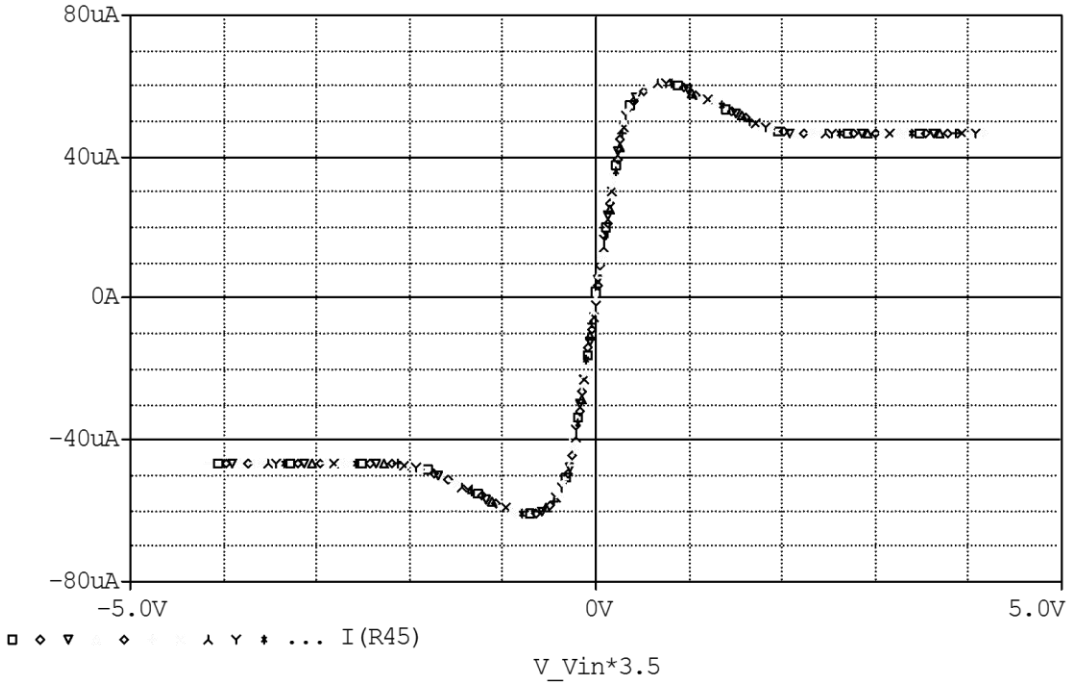
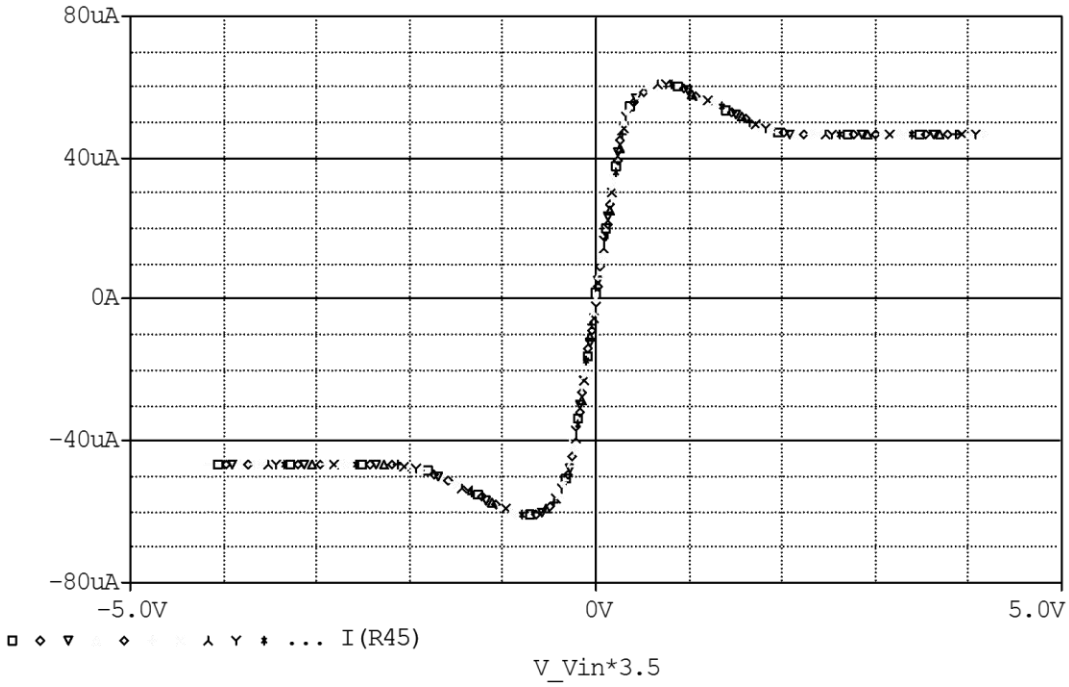


Figure 3.18: Monte-Carlo Simulation of the function in Eq. (3.11) with ± 5 % change in C_{ox} of all transistors.

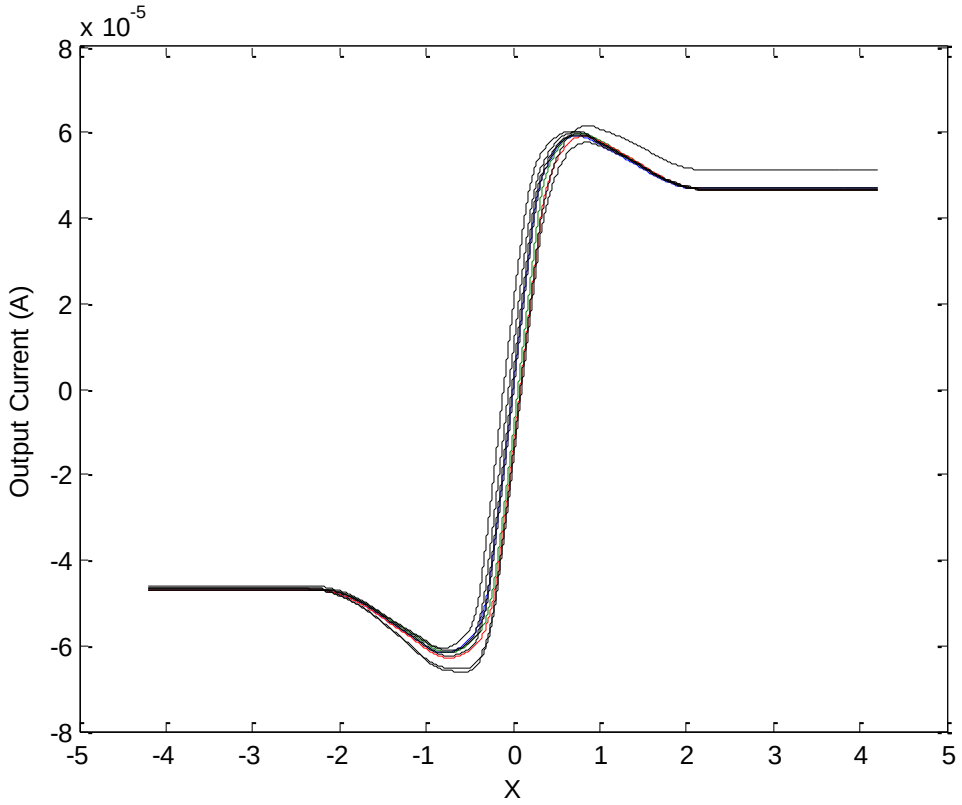
Fig. 3.19 shows that the performance of the same function is excellent and almost not affected by variations in the threshold-voltage V_{th0} of all transistors when $\pm 0.5\, mV$ of variations applied.



3.19: Monte-Carlo Simulation of the function in Eq. (3.11) with $\pm 0.5\, mV$ change in V_{th0} of all transistors.

The performance of the same function for change of ± 5 % in the aspect ratio W/L of all transistors was investigated. The results, shown in Fig. 3.20, show that the maximum error of change is approximately 20.8 %, and this large error was expected because the CCCII circuit is highly sensitive to any small variations of the transistors geometries.

This kind of errors can be minimized by careful designing of the transistor sizes, and by maximizing the supply voltage.



3.20: Monte-Carlo Simulation of the function in Eq. (3.11) with ± 5 % change in W/L of all transistors.

Table 3.6 summarizes the proposed FS in this thesis with most recent published FS and their results.

Table 3.7: Comparison between the proposed and the previously presented FS.

Ref.	**CMOS Tech.**	**Power Supply**	**Power Consmp.**	**Chip Area** $(\mu m)^2$	**BW** (MHz)	**# of Functions**
Proposed FS	$0.18\ \mu m$	$\pm 0.75\ V$	$5.144\ mW$	458.1	25	Multi
[1]	$0.18\ \mu m$	$1\ V$	---	7.56	< 10	Single
[18]	$0.18\ \mu m$	$\pm 0.9\ V$	---	99.76	344	Single
[19]	$0.18\ \mu m$	$0.9\ V$	$< 1\ mW$	> 1152	4	Single
[21]	---	$\pm 2\ V$	---	126	25	Multi
[22]	$0.5\ \mu m$	$\pm 1.5\ V$	$> 5.4\ mW$	12200	< 25	Multi

The proposed FS circuit features competitive advantages in comparison with the reported ones published in [1, 18, 19, 21, and 22]. Table 3.7 shows that the proposed FS in this research affords low voltage power supply when compared with [21, 22], much less occupied area than the work in [22], less amount of power consumption, and almost the same speed of operation. In addition, the accuracy of the proposed FS is over full input range which is not the case in [1, 18, 19, 21, and 22] affording accuracy over very limited input ranges.

CHAPTER 4

CONCLUSION

A new CCCII-based nonlinear analog function synthesizer was proposed. The nonlinear behavior of CCCII was utilized to approximate multi harmonics of hyperbolic tangent functions in order to realize complex nonlinear mathematical functions. The function synthesizer consists of three CCCIIs which can approximate three harmonics of hyperbolic tangent functions ($tanh(x), tanh(2x), and\ tanh(3x)$). In addition, the circuit uses three Current-Mirror current-gain amplifiers used to weight the generated hyperbolic tangent functions by arbitrary gains.

PSPICE simulation was used to implement the proposed circuit and to investigate the performance. The circuit was simulated with $\pm 0.75\,V$ power supply, and 0.18 μm CMOS process technology. The approximated functions $tanh(x), tanh(2x)$, and $tanh(3x)$ have RRMS errors of 2.74 %, 2.84 %, and 2.42 %, respectively. Furthermore, three arbitrary combinations of the approximated functions were simulated in Fig. 3.11, 3.12, and 3.13 and produce RRMS errors of 4.25 %, 11 %, and 9.5 %, respectively.

The main sources of errors are coming from the approximation that is from CCCII block itself and from the Current-Mirror current-gain amplifier nonlinearity. However, the majority of errors were produced by the Current-gain Amplifiers because of their limited linearity range.

The proposed analog function synthesizer has several advantages over the available ones in literatures which are the simple implementation structure of CCCII and Current amplifier wide normalized input range of -3.5 < x < 3.5, low power supply of $\pm 0.75\ V$.

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