# CONFIGURABLE ANALOG BUILDING BLOCKS FOR FIELD PROGRAMMABLE ANALOG ARRAYS

BY

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OF PETROLEUM & MINERALS

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*To My Family*

# Acknowledgment

All praise and glory is to almighty Allah who gave me courage and patience to carry out this work, and peace and blessings of Allah be upon prophet Mohamed.

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# Thesis Abstract

**Name**: OSAMA OGLAH FARES

**Title**: CONFIGURABLE ANALOG BUILDING BLOCKS FOR FIELD PROGRAMMABLE ANALOG ARRAY

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In this dissertation, the design of configurable analog blocks for field programmable analog arrays is presented. The configurable blocks are capable of performing integration, differentiation, amplification, log, and anti-log functions. The realization of these functions depends on differential continuous-time current-mode translinear loop techniques. To maintain high frequency operation, programmability and configurability of the blocks are achieved by modifying the block's bias conditions digitally. The analog signal processing part of the blocks is designed using BJTs. To get compatibility with digital, the controlling parts of the blocks are designed using CMOS. Simulation results for the presented circuits and for examples of analog signal processing systems formed using them are also introduced.

Keywords: Configurable analog blocks, field programmable analog array, analog signal processing, continuous-time current-mode circuits.

# خلاصة الرسالة

الأسم : أسامة عقله فارس

عنوان الرسالة: وحدات بناء تناظرية قابلة للتشكيل لحقول المنظومات التناظرية المبرمجة

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تقدم هذه الأطروحة تصميم وحدات بناء تناظرية قابلة للتشكيل لحقول المنظومات التناظرية المبرمجة. هذه الوحدات قادرة على تنفيذ دوال التكامل والتفاضل والتظخيم واللوغاريتم والدوال الأسية. يعتمد تحقيق هذه الوحدات البنائية على الدوائر العبر خطية المتباينة ذات الزمن المتصل. للمحافظة على الأداء عالي التردد تتم عمليات التشكيل والبرمجة لهذه الوحدات بواسطة تعديل شروط تهيئة الوحدات رقميا. تم تصميم معالج الأشارات التناظري لهذه الوحدات بوساطة (BJT) ترانزستورز. للحصول على تواص متناغم مع التقنيات الرقمية، تم تصميم اجزاء التحكم الرقمية لهذه الوحدات بوساطة (CMOS) ترانزستورز. تم كذلك تقديم نتائج المحاكاة لهذه الوحدات ولأمثلة لنظم معالجة تناظرية تم بناءها بهذه الوحدات.

جامعة الملك فهد للبترول و المعادن
مايو 2004م

# CHAPTER 1

# INTRODUCTION

Over the past several years and since they were invented, Field Programmable Gate Arrays (FPGAs) have made an important success in many areas of applications ranging from simple functions to complex dynamically reconfigurable systems. FPGAs are Programmable Logic Devices (PLDs) that consist mainly of a large number of modules and interconnections allowing arbitrary configurations of combinational and sequential logic. Designs using such FPGAs have numerous advantages over discrete techniques. Examples of such advantages include; high integration density, high reliability, fast turn-around design cycle time, lower mass, volume and power consumption [1-5].

In many fields of applications, e.g. mobile and remote applications, analog design can offer superior performance to its digital counterpart in terms of reduced power consumption, higher operating speed, lower area, and lower cost [6, 7]. This is in part because analog systems do not require analog to digital (A/D), digital to analog (D/A) converters, and anti-aliasing filters which are essentials in digital systems. However,

going directly to the component level in implementation needs years of experience to solve even a simple problem in the analog domain. The ability to implement such systems using general purpose programmable analog or mixed-signal arrays would be advantageous in all respects analogous to the advantages gained using FPGAs. This was a very motivating factor towards research in the Field Programmable Analog Arrays (FPAAs), the analog counterpart of the FPGAs [1-52].

FPAAs are programmable devices that are intended to provide analog designers with the same level of in-system configuration flexibility as digital designers nowadays take for granted with FPGAs. The power of a FPAA is that it is an ideal device for quick reconfiguration due to its software support, allowing for easy design, debugging and implementation of various analog functions [8]. Thus, using FPAAs, minimal design work is needed to produce fully programmable analog building blocks which were painstaking when designed and built using discrete analog techniques at the component level.

FPAA devices consist of Configurable Analog Blocks (CABs), routing network, peripheral input/output blocks, digital control unit, and Computer Aided Design (CAD) tools. The CABs are analog processing cells that are connected via the routing network to perform a desired function [8, 9]. Each CAB is able to execute a small but powerful set of mathematical functions and can be digitally programmed and interconnected to solve problems at the equation level [6]. CABs are considered as the heart of the FPAA, and special attention must be paid in designing them. The main aim of this research is to develop CABs circuitry with higher frequency ranges

and lower power supply voltages for FPAAs. Peripherals to the CABs and the routing network are the input/output blocks which interface with signals external to the FPAA. A conceptual FPAA is shown in Figure (1-1) [10]. Included are the CABs, interconnection network, input/output blocks, and configuration bit string.

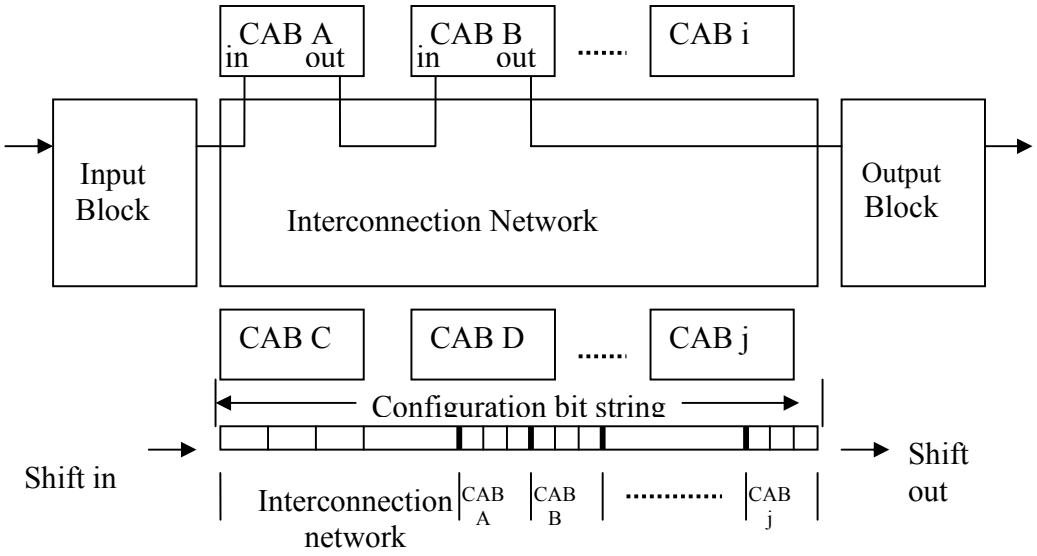



**Figure 1-1** Conceptual FPAA Diagram

## 1.1 Dissertation Overview

This dissertation consists of five chapters that deal mainly with problems associated with the design of configurable analog blocks that could be used to build a complete FPAA.

- This first introductory chapter is focused on literature review of the main FPAAs of both commercial and academic origin that already exist is concluded. Possible markets and applications of such circuits are also pointed out. The chapter concludes with the motivation toward developing CABs with lower power supply voltages and larger frequency ranges.
- The second chapter starts with an introductory to the general architecture of a FPAA and the units forming it. A brief description of the techniques used in building existing CABs is also introduced. The proposed approach in building the CABs, which is the continuous-time current-mode approach, is then stated. Advantages of this approach over other possible approaches are also discussed. The chapter ends with a brief look at the possible technologies that could meet the functional requirements of the proposed CABs.
- Chapter three discuses the circuit design of the adopted CAB cell. In this chapter, the design of the integrator, the differentiator, the log and the anti-log circuits are all presented. Both circuit description and Pspice simulation results are included.
- Chapter four introduces some of the possible applications that can be achieved when connecting the proposed CABs in FPAA architecture. As a first

example two different topologies of building a universal filter using the proposed CABs are tested. In the second example, a power factor generator circuit is built. The final example is an AM modulator/demodulator system. Functional description and simulation results for all these examples are also included. The chapter concludes with summary of other possible applications these CABs can be used to build.

- In chapter five, we conclude our work by summarizing the results obtained throughout this research and provides possible directions for future work.

## 1.2 Literature Review

As semiconductor techniques advance rapidly, many companies and research groups enter the FPAA domain. Following is a brief review of the CABs of different existing FPAA architectures of both educational and industrial origin.

### 1.2.1 Educational CAB Designs

#### 1.2.1.1 Early CAB Designs

An early conceptual FPAA design is the Proto-chip developed by Sivilotti [56]. The Proto-chip's CABs are designed at the transistor level, and the interconnection network is based on a tree structure. Its target application was prototyping of analog neural networks. An early successful physical design was the one reported by Lee and Gulak [32]. It uses CMOS operating in sub-threshold regions and operates below 100

kHz frequencies. The CABs of this configuration were built from other sub-blocks that are connected to each other via pass transistors activated by a set of configuration bits. However, this approach is not appropriate for linear analog circuit applications due to the parasitic effects of the pass transistors. The CABs of that FPAA got their configurability by controlling the various switches and/or multiplexers within the CAB itself. Its target application was hardware implementation of neural networks. The advantage of using the sub-threshold technique was that the currents used are extremely low, leading to very low power consumption. However, the operating bandwidth of such designs is very limited.

Another early design for configurable blocks is the one presented by Brook *et al* in [50]. These CABs were designed at transistor level using MOSFETs to function as either constant multipliers, summers or integrators. These basic functions were assumed to be sufficient to implement any linear function once it is represented in the state-space form.

#### 1.2.1.2 University of Toronto Research Group

In addition to the FPAA based on MOSFETs working in subthreshold, which have been mentioned earlier [32], the current University of Toronto research group has presented two other FPAAs. The first FPAA consists of fully-differential continuous-time CMOS transconductor-based CABs operating in the 100 kHz range [15, 16]. This FPAA was targeted toward signal processing applications in the audio range. The CABs of this FPAA contain an op-amp as well as switchable feedback

capacitors, and can also be used to implement a comparator by turning off the compensation capacitor, (Figure 1-2a). In this design, switches in the interconnection network are implemented using the transconductor, which acts as a programmable on/off switch, polarity change switch, and variable resistor, Figure (1-2b). The transconductor is also used to realize a four quadrant multiplier.

Gaudet and Gulak presented another FPAA that is based on current conveyors [17, 29, and 30]. This FPAA is targeted toward applications in the video frequency range (10 MHz). Each CAB of the FPAA consists of a second generation current conveyor CCII and a bank of programmable resistors and capacitors. The function set adopted for these CABs includes integration, differentiation, and amplification.

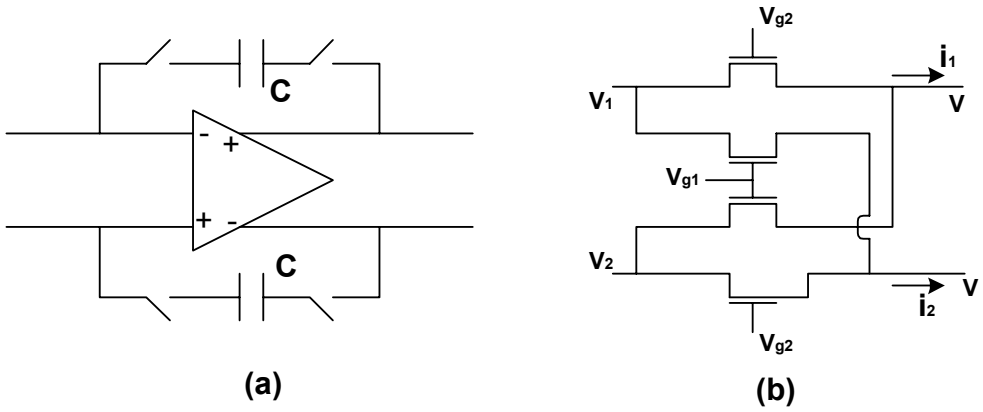



**Figure 1-2** a) Schematic diagram of the adopted CAB, and b) The four-transistor differential transconductance used as on/off switch, polarity change switch and variable resistor.

#### 1.2.1.3 Portland State University Research Group

The research group of Portland State University presented a bipolar current-mode continuous-time OTA-based FPAA [12, 25, 39, and 40]. The architecture of this FPAA has a matrix-like topology that consists of current-mode processing CABs interconnected to each other using a two levels routing network; local and global. This FPAA is mainly targeted toward continuous, fuzzy, and multi-valued logic applications. Each CAB can be programmed to perform one of the functions included in Table 2-1. The frequency range of this FPAA is up to 10 MHz. Figure (1-3) shows the functional block diagram of one individual cell of the proposed FPAA. The cell works in one of two modes: passive-control mode and active-control mode. In the passive control mode only the analog blocks of the cell perform signal processing functions. The control circuit determines the parameters and configuration of the analog blocks of the cell, but is otherwise not involved in the signal processing. In the active-control mode, the control circuitry additionally takes part in some signal processing functions. One of the most important configurable blocks forming this cell is the current-mode integrator/amplifier configurable circuit. This CAB is based on OTA-C technique in which the configuration is done using biasing currents rather than switches. However, the capacitors used in this design are floating capacitors making the circuit subject to parasitic effects. The block diagram showing this configurable block is shown in Figure (1-4).

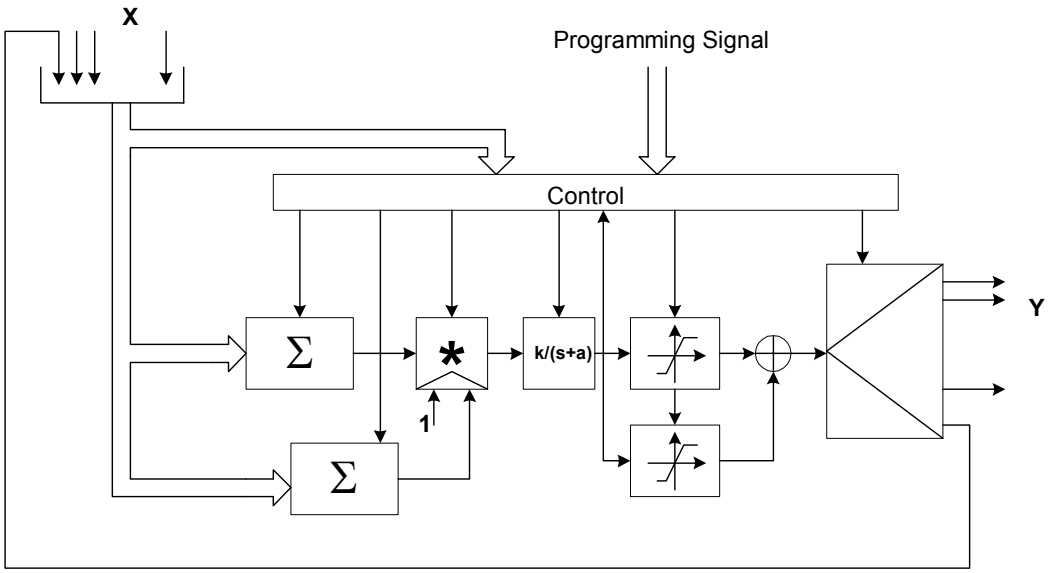
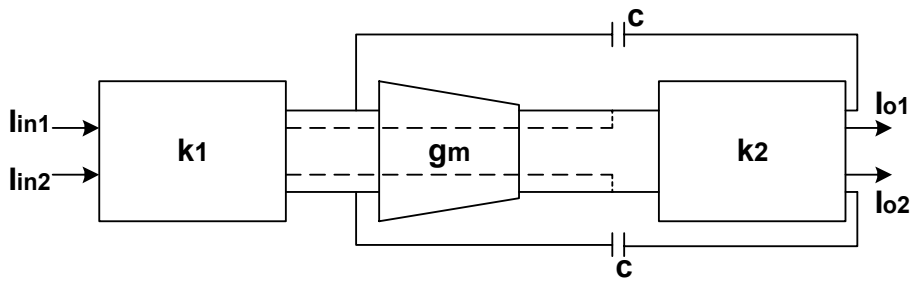
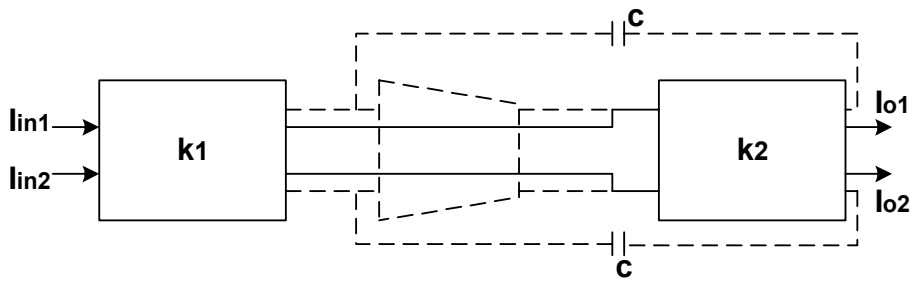



**Figure 1-3** Functional block diagram of one CAB of the proposed FPAA in [12, 25, 39, and 40].




**(a)**




**(b)**

**Figure 1-4** Block diagram of the current-mode integrator/amplifier proposed in [12, 25, 39, and 40]: (a) Integrator, (b) Amplifier.

#### 1.2.1.4 Johns Hopkins University Research Group

A research group at Johns Hopkins University has developed a space-qualified Field Programmable Mixed-signal Array (FPMA) circuit (Field Programmable Mixed-Signal Array; an IC that contains a FPAA and a FPGA linked together by configurable converter blocks) [1, 2]. The FPMA analog module contains an operational amplifier, four programmable resistors, eight programmable capacitor array (6-bits resolution) and 32 CMOS switches. All these resources are connected to each other via a routing network. Figure (1-5) represents one side of the differential architecture of the CAB.

In order to minimize the effects of interconnection resistance, a new technology, M2M, was used. This new technology can give radiation-tolerant switches with an ON resistance in the range of 15 to 25Ω. The analog module design of this FPAA includes the following resource; operational amplifier, programmable resistors, programmable resistor arrays and CMOS switches.

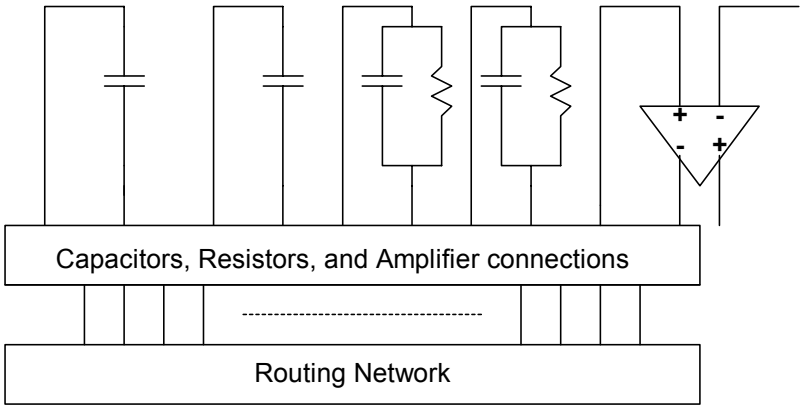



**Figure 1-5** One side of the differential architecture of the CAB proposed in [1, 2]. The complete CAB architecture consists of another side similar to the shown part.

#### 1.2.1.5 Texas A&M University Research Group

Texas A&M research group proposed a current-mode FPAA that consists of a modular array of CABs [43, 44]. Each of the CABs includes three sub-cells: a Configurable Analog Cell (CAC), a Programming Register (PR), and Programming Logic (PL). The CAC is designed so that it can be configured to perform one of three functions: an integrator, an amplifier, or an attenuator. The programmability for both the functionality and the parameters can be achieved by activating and deactivating certain branches forming the CAC itself. A schematic diagram of this CAC is presented in Figure (1-6). A deactivated branch has all its transistors turned OFF where any transistor needed to be OFF will have its gate connected to the proper rail. All branches are by default, deactivated. Simulation results of this FPAA demonstrate a bandwidth of tens of kHz up to a few MHz.

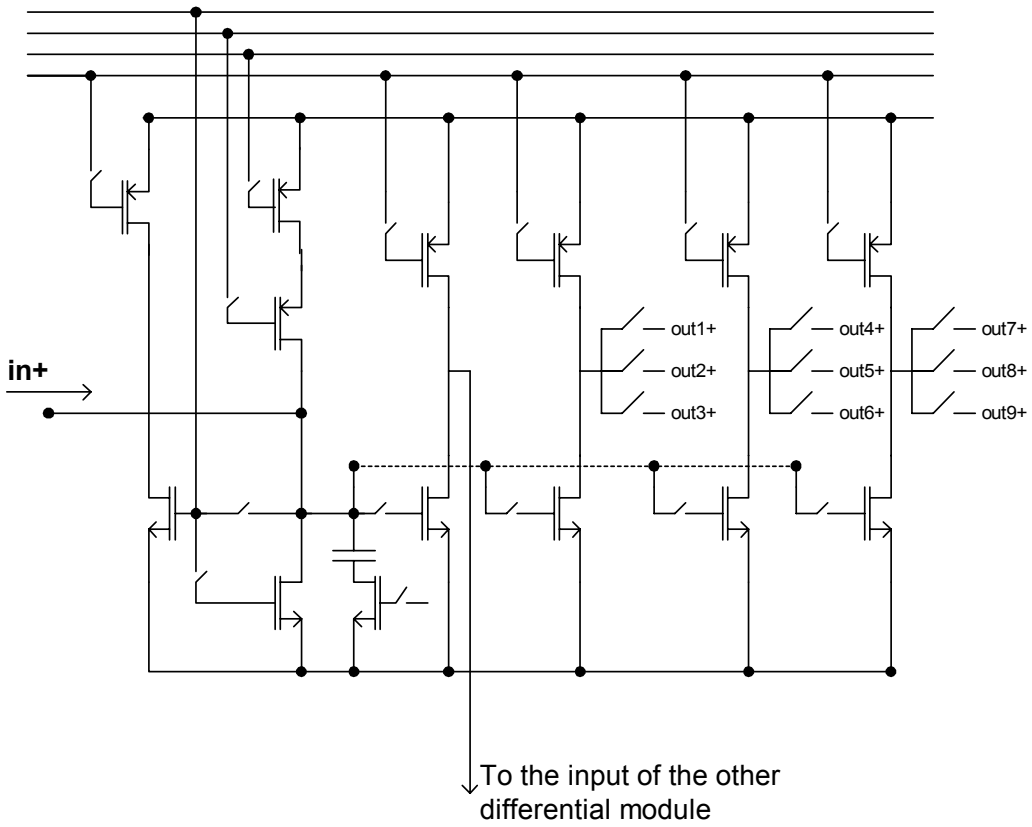



**Figure 1-6** Circuit schematic of the Configurable Analog Cell (CAC).

#### 1.2.1.6 Technical University of Gdansk, Poland, Research Group

This research group presented a general CAB that consists of six signal terminals (A-F), a fully differential programmable OTA, two programmable grounded capacitors working as one floating capacitor, and a set of MOSFET switches [26, 27]. The programmable capacitor consists of five grounded capacitors and five switches. Programming the CAB is done by a control word of 22 bits. Simulations and experimental results show that filters with frequencies from several kHz to a few MHz can be realized based on this CAB configured in a matrix-like FPAA.

#### 1.2.1.7 Other Research Groups

There are several other university research groups that are interested in developing CABs for FPAA and FPMA. A group in Cimirly Lyon, France is working on a current conveyor-based FPAA [31]. A group at the University of Nottingham, UK, is working on a switched-current design [42]. Also, there has been work published from groups at the SDC-Alba center of Scotland [8], University of Illinois [14], Deemed University, India [28], and University of Manchester, England [45].

Table 1-1 shows a list of most of the CABs proposed in the literature.

**Table 1-1** List of most of the CABs in the literature.

| CAB | Technique | Prog. & Config. | Bandwidth | Notes |
|---|---|---|---|---|
| Lee & Gulak [32] | Subthreshold | Pass switches & variable voltage sources | Below 100kHz | V. low power dissipation. Neural net. app. |
| Lee & Gulak [15, 16] | Op-Amp based. | Variable transconductance & switches | Around 100kHz | Limited linearity and bandwidth. |
| Gaudet & Gulak [17, 29, 30] | CCII-Based | Banks of programmable R's & C's | 10 MHz | Large area |
| Edwards et al [1, 2] | Op-Amp Based | Banks of programmable R's & C's | | Space applications |
| Quan et al [43, 44] | Current-mode transistor-based. | Switches and programmable voltage sources. | ~10KHz ➔ ~1MHz | continuous signal processing |
| Pankiewicz [26, 27] | OTA-based | Prog. OTA, prog. C's, & switches | Several kHz to a few MHz | continuous signal processing |
| Permont et al [31] | CCII conveyor based approach | Tunable resistors and capacitors. | Several kHz to a few MHz | continuous signal processing |
| Kutuk & Kang [14] | S/C | S/C | 2KHz-260KHz | continuous signal processing |
| Pierzchala [12, 13, 25, 39, 40]. | Transistor-based current-mode | Programmable biasing currents | 10's of KHz up to 10MHz | continuous, fuzzy, and multi-valued logic |
| Loopy & Lyden [8] | Op-amp Based | Programming switches | Up to 1MHz | continuous signal processing |
| Anderson et al [38] | S/C | S/C | Up to 100KHz | continuous signal processing |
| Ray, B. [28] | OTA-Based | Biasing currents and switches | 100's of MHz | continuous signal processing |

### 1.2.2 Commercial CAB Designs

#### 1.2.2.1 Motorola MPAA020

In 1997 Motorola Inc. released a CMOS switched-capacitor FPAA design called the MPAA020 [9, 33]. The CABs of this FPAA are organized in a matrix-like architecture. The FPAA includes four rows each of five CABs and is programmed using a 619-bit string. Each CAB can realize a first–order filtering functions. A CAB can be connected to its immediate neighbors through the local inputs and local outputs. It can also be connected to its other neighbors via a global bus accessed through the global bus input and global outputs. The clock frequency is 1 MHz, limiting bandwidths to around 200 kHz. A PC-based CAD tool accompanies the MPAA020 to ease its programming which is done via serial port. Due to the complete withdrew of Motorola from the FPGA and FPAA markets; the MPAA020 is no longer commercially available.

#### 1.2.2.2 Anadigm

Anadigm has recently resurrected Motorola's FPAA [19, 20]. The FPAA chip can be reprogrammed as many times as desired so designers can try out as many circuits as they like. There are twenty usable analog CABs on the chip. Each CAB contains an op-amp and five programmable feedback capacitors. Each capacitor is actually made up of a bank of 255 capacitors that can be switched ON or OFF, allowing for one of 255 different values. The capacitor values are set using static switches. There are also dynamic switches on the chip that handle the dynamic switching that makes a

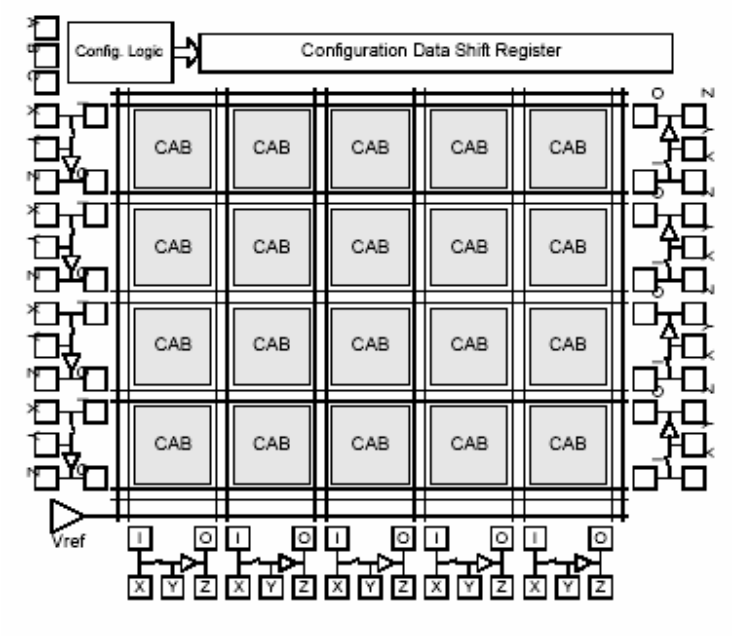
capacitor function as if it were a resistor; S/C technique. There are also dynamic switches that switch with respect to the phase of the input signal. Numerous other static switches that allow the capacitors and op-amp within each analog zone to be connected in various ways also exist.

AnadigmDesigner is the PC hosted design system that gives designers access to the chip. This CAD tool presents the user with a simplified view of the FPAA chip. It includes also a simulator to simulate a circuit before being downloaded on to the associated chip.

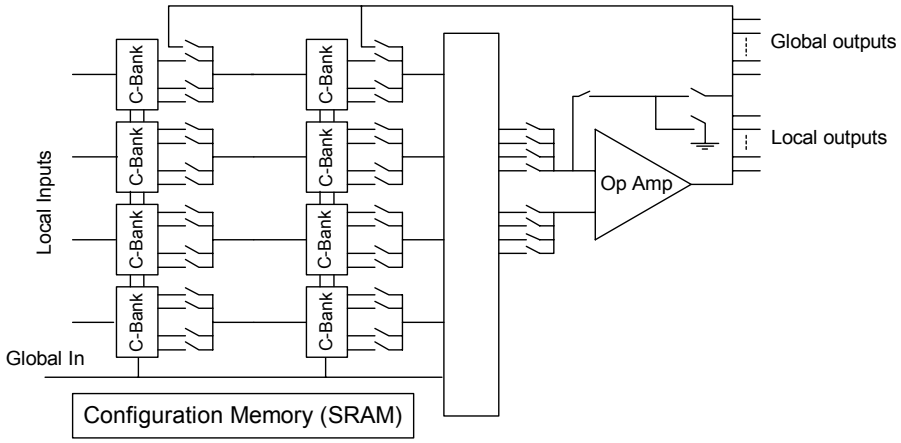
AnadigmDesigner's IPmodule library is composed in part of switch settings that set up the internal connectivity of the op-amps and capacitors of one or more zones. AnadigmDesigner handles all of the details so that user does not have to learn about all of the internal switches. The only thing a user has to do is select the IPmodules he wants to use, connect them with "wires", adjust each IPmodule's parameters using a pop-up menu, download the data to the chip and see the results on the oscilloscope. IPmodule library consists of functions that can be implemented using either one CAB or two CABs. Examples of such functions are inverting and non-inverting comparators, low and high $Q$ biquadratic filters, inverting and non-inverting integrators, gain stages, and many others.

Figure (1-7) shows both a block level view of the Anadigm AN10E40 FPAA and a block level view of the basic CAB. The AN10E40 comprises a 4x5 array of CABs, enmeshed in clocking, switching, local and global routing resources. The Configuration Logic and the Shift Register work together whenever chip

configuration is in process. The array of CABs is surrounded on three sides by programmable analog input/output cells, 13 in all, with two spare uncommitted op-amps. The lower region of the chip also contains a programmable reference voltage generator. Each CAB of the AN10E40 is an op-amp surrounded by capacitor banks, local routing resources, local switching and clocking resources, and global connection points. This collection of hardware enables the CAB to perform many of the functions that could be achieved using an op-amp and conventional passive components.




(a)




(b)

**Figure 1-7** a) Block level view of the Anadigm AN10E40 FPAA and b) Block level view of the basic CAB.

#### 1.2.2.3 Fast Analog Solutions Totally Reconfigurable Analog Circuit

Fast Analog Solution's (FAS) FPAA, called the TRAC020 (Totally Reconfigurable Analog Circuit), consists of 20 continuous time log-domain bipolar CABs operating up to 4 MHz [6, 21, 23, 37]. Each of these CABs can accomplish one of the following functions: ADD, NEGATE, PASS, LOG, ANTILOG, RECTIFY, AUX and OFF. These CABs are organized in two string-like rows of 10 CABs. The TRAC is programmed using a PC-based CAD tool. This CAD tool includes a simulator to simulate a circuit before being downloaded onto the FPAA IC.

Figure (1-8) shows an example of how to use this FPAA to build a four quadrant (4-q) multiplier. In a 4-q multiplier both the multiplier and the multiplicand, X and Y respectively, can assume positive or negative polarity. However, the CABs of TRAC FPAA can support only positive polarities. Thus, to achieve 4-q multiplication, a positive reference DC voltage is added to X and Y. Assuming all signals to be normalized, both signals (X + 1) and (Y + 1) are introduced as inputs to two log-stages. The outputs of these two log-stages are then added together and the result is then fed as the input to an anti-log stage. This results in $(X + 1)(Y + 1) = XY + X + Y + 1$. To get the final result which is XY, the signals X and Y and the normalizing factor, here it is 1, are all subtracted from the output of the anti-log stage. The DC reference voltage used at the first stage of the circuit is used as a multiplication factor to achieve temperature compensation.

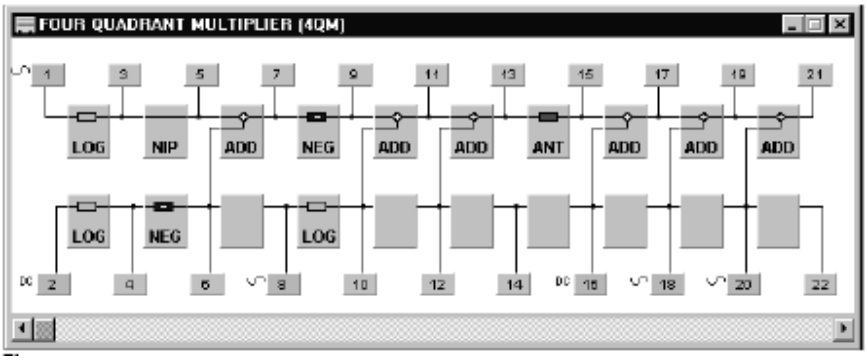



**Figure 1-8** Example of using TRAC CAD tool to built a four quadrant multiplier

#### 1.2.2.4 LATTICE Semiconductor Reconfigurable Analog Circuits

Over the last few years Lattice Semiconductor Corporation has presented a family of reconfigurable analog circuits, namely ispPAC10, ispPAC20, ispPAC30 and ispPAC80/81 circuits [53].

The ispPAC10 consists of four programmable analog macrocells called PACblocks, each emulating a collection of operational amplifiers, resistors and capacitors. Requiring no external components, it flexibly implements basic analog functions such as precision filtering, summing/differencing, gain/attenuation and integration. Each PACblock contains a summing amplifier, two differential input instrument amplifiers, and an array of feedback capacitors. The capacitors, combined with a fixed value feedback element, provide more than 120 programmable poles between 10kHz to 100kHz with an absolute accuracy of 5.0 percent. Variable gain input instrument amplifiers make it possible to program any PACblock gain in integer steps between ±1 and ±10. More complex signal processing functions are performed by configuring additional PACblocks in combination with each other to achieve a variety of circuit functions. Configuring an ispPAC10 is accomplished using PAC-Designer, a Windows-based design environment. Figure (1-9) shows a typical application diagram of the ispPAC10 circuit.

The ispPAC20 circuit is similar to the ispPAC10 circuit except that the chip contains two PACblocks rather than four.

The ispPAC30 device integrates nearly all the essential analog front-end functions for a typical data acquisition/conversion application with a bandwidth of operation up to

1.5 MHz. It consists of 4 programmable gain instrumentation amplifiers, 2 Multiplying Digital to Analog Converters (MDAC), and 2 configurable output amplifiers with rail-to-rail outputs. This device provides functions such as programmable gain, offset and filtering.

The ispPAC80/81 devices are the latest members of Lattice Semiconductor's ispPAC programmable analog device family. These two devices enables designer to implement tens of thousands of in-system programmable continuous-time 5th order low pass filters with corner frequencies ranging from 50 kHz to 750 kHz for the ispPAC80 and from 10 kHz to 750 kHz for the newest ispPAC81. These devices can implement filters in Butterworth, Chebychev, Elliptical, and other topologies.

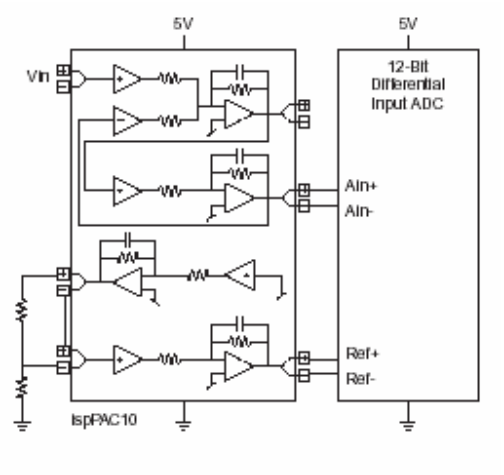



**Figure 1-9** Typical application diagram of the ispPAC10 circuit.

## 1.3 Applications

FPAAs are continuously covering new fields of applications ranging from audio frequencies up to video ranges. Besides implementing basic building blocks such as amplifiers, filters and oscillators, FPAAs can be used to implement complete systems. Filters are considered to be the most important application of FPAAs [22, 35]. This is because filters are required in almost every analog circuit design. One programmable analog IC that is targeted toward filters implementation is the one manufactured by Lattice Semiconductors [18, 24, and 53]. LATTICE FPAA (ispPAC80) encompasses all the necessary components on-chip to implement every popular type of continuous-time fifth-order low-pass topology with programmable gains of 1, 2, 5, and 10. A single ispPAC80 can implement fifth-order Butterworth, Bessel, Chiebychev, Legendre, elliptical, Gaussian, and linear low-pass filters with programmable corners from 50 to 750 kHz. The filter chip is supported by an integrated design environment called the PAC-Designer. It includes a filter configuration data base that offers every popular response in a pre-defined click-and-use format.

Another commercially available FPAA that is capable of implementing filters is ANADIM FPAA [20]. Due to its switched-capacitance dependence, the range of operating frequencies is a little bit less than the ispPAC80. Also, the frequency range of this FPAA depends on the circuit functions being implemented. Typically, the entire array can handle signal frequencies from DC to 500 kHz making it ideal for filtering, medical, automotive and low-to-medium frequency communication markets.

Zetex's TRAK FPAA is another FPAA that is successful in a wide range of applications [21]. As an illustrative example of the versatility of such FPAA, a full AM receiver was built and tested in [23]. Another illustrative example is the universal single-chip programmable tone detector for telecommunication applications [37].

FPAAs are used also in aerospace applications, neural networks, and continuous, fuzzy, and Multi-Valued Logic (MVL) [1, 2, 16, and 25].

## 1-4 Motivation

The ever-presented demand on high frequency operation at lower power supply voltages is the main requirement that affecting the design of the configurable analog blocks of any field programmable analog array. However, the existing FPAAs, except the one presented in [12], can not satisfy these requirements. In general, voltage-mode circuits will always suffer from the need of higher power supply voltages to maintain reasonable dynamic ranges. Device-based CABs will also suffer from limited upper frequency range. This is mainly due to either the limited bandwidth of the device used, such as the case when using op-amps, or due to the relatively large number of switches needed to program the CABs when using capacitor and resistor banks for programmability. Not to mention also the relatively large silicon area needed by such capacitor and resistor banks.

The analog part of the CABs of the FPAA presented in [12] is formed of current-mode circuits to realize weighted summer, multiplier, integrator, amplifier, and

limiter. In order to achieve high frequency operation, no switches were used in the signal path and programmability and configurability were achieved by modifying cell's bias conditions digitally.

In this research, the use of the current-mode technique is extended to realize CABs for a new set of functions including log, anti-log, integrate, amplify, and differentiate. Using this set of functions, wider range of applications can be covered. To maintain high frequency operation, programmability and configurability of these CABs is also achieved by digitally modifying the biasing conditions.

# CHAPTER 2

# PROBLEM FORMULATION AND PROPOSED APPROACH

The proposed research is aimed at developing key circuits of configurable analog blocks used to build field programmable analog arrays for high frequency operations under low voltage power supplies. Due to the many advantages the continuous-time current-mode techniques have, these techniques are to be used in designing the proposed CAB's circuits. A brief discussion of these examples is presented in the following sections. As CMOS technology has advantages over BJT technology in terms of lower power consumption, higher integration density, and compatibility with existing digital technologies, this technology can be considered as a first choice for the designers. However, the higher bandwidth, the higher transconductance, the lower noise, and the easier implementation of nonlinear functions (such as Log and Anti-log functions) make BJT transistor the most suitable candidate to implement the CAB's circuits. To achieve compatibility with digital technologies, the digital controlling

parts of the CABs are designed using CMOS. Following is a general description of the main issues concerning the design.

## 2.1 FPAA Architecture

As mentioned before, a FPAA consists of CABs that form the main signal processing units in conjunction with routing networks that connect the CABs together and CAD tools to ease their programmability. Following is a description for these main basic and common parts of any FPAA.

### 2.1.1 The Configurable Analog Blocks

The Configurable Analog Blocks (CABs) are analog processing cells that form the heart of the FPAA. The CABs can be realized at different functionality levels, including transistor, sub-circuit, building block, macro-block, or even sub-system level [11]. Choosing the functionality level is quite flexible and partially depends on the applications toward which the FPAA is targeted. CABs may be also either homogeneous or heterogeneous. In homogeneous structures, all CABs are identical and programmable to implement a set of functions. In heterogeneous structures, CABs are distinct for different circuit functions [9].

In majority of cases, CABs are required to be able to perform a relatively small but strategically critical set of analog functions that are capable of sitting alongside a much larger set of other more complex functions [12]. Choosing these functions is a very important characteristic to be decided by the designer of an FPAA. Among the factors that affect the choice of these functions are:

1. Applications toward which the FPAA is targeted. The chosen set of functions must be able to represent and cover a wide range of possible applications.
2. FPAA's Topology. The choice of the set of functions is also partially dependent on the topology chosen for the FPAA. Generally, there are two main topologies; the matrix-like topology and the string-like topology. In the matrix-like topology, the CABs are ordered in rows and columns forming a matrix where all CABs can be connected to any other CAB using a local and a global routing network. In string-like topologies, the CABs are arranged in strings and they can be connected only to the following CABs in a feed-forward manner. Examples of these topologies is given in Section
3. These functions must also be suitable for easy translation into electrically equivalent functional blocks hardware that must have programmable parameters to accommodate the range of user's applications.

Great deals of thought and experimental work done in how to choose this set, but still there are no standards for such functions [6, 8-22, 54, and 55].

One example of such set of functions is the one presented in [6, 21, and 46]. This set consists of the following functions; ADD, NEGATE, LOG, ANTILOG, DIFFERENTIATE, and INTEGRATE. Add and negate functions are obviously of fundamental importance since these operations can be considered as the most fundamental for any mathematical operation. The use of logarithmic functions provides a convenient and eminently practical element of providing multiplication, division, and raising to the power. Differentiate and integrate functions are

fundamental for many signal processing systems specially for filtering application. These two functions provide the designer with the basic blocks needed to realize any transfer function presented in the **s**-domain. In practice, wide range of processing tasks can be described mathematically in a form that can be expanded and expressed using these six operands.

Another example of a possible set of functions is the one presented in [12, 13], shown in Table 2-1. The cells of this design are assumed be part of a matrix-like structure. In this FPAA, all cells are identical and can be programmed to implement any of the functions specified in Table 2-1.

One other example of these set of functions is the one adopted by Lee and Gulak [15, 16]. This set of functions was basically oriented towards neural network applications and is formed of addition, threshold operation, coefficient multiplication, and signal multiplication.

**Table 2-1** Selected functions of a single CAB adopted in reference [12, 13].

| |
|---|
| 1. $y = k \cdot \frac{\sum_i w_i x_i}{\sum_i w_i} \cdot \frac{\sum_j w_j x_j}{\sum_j w_j}$, $k$ and $w_i$ are constants |
| 2. $y = k \cdot \frac{\sum_i w_i x_i}{\sum_i w_i}$ |
| 3. $y = k \cdot x_i \cdot x_j$ |
| 4. $y = k \cdot x_i^2$ |
| 5. $y = k \cdot \min(x_1, ....., x_n)$ |
| 6. $y = k \cdot \max(x_1, ....., x_n)$ |
| 7. $y = k \cdot y_{1-6} \cdot \frac{1}{s+a}$, $a$ is a constant |
| 8. $y = a \cdot sign(y_{1-7})$ |
| 9. $y = b \cdot U(y_{1-7})$, U is the step function , $b$ is a constant. |
| 10. $y = k \cdot \lvert y_{1-7} \rvert$ |
| 11. $y = x_i$ (identity) |

### 2.1.2 Routing Network

In general, the FPAA gets its configurability from the routing network which allows the user to control the flow of signals between available analog active resources and thus to build more complex systems. These networks can take the form of a tree, crossbar, or data path [8]. In FPAAs, switches regularly take the form of pass-transistors [11]. However, this is not optimal for FPAAs since pass transistors introduce circuit nonidealities that limits linearity of analog circuits. Instead, circuit techniques such as switched-capacitor circuits or transconductors are used [11, 14-17].

A fundamental problem in the design of an accurate FPAA is thus to eliminate errors due to resistive voltage drop in the switches routing the signals between the diverse sources and load impedances of active function blocks. This interconnection resistance also influences the signal delay and is probably the most likely reason for the rarity of FPAA parts commercially available [1, 2].

CMOS switches are the most suitable candidate to fulfill the requirements of FPAA interconnects. These switches are easy to be configured digitally and have a relatively simple dominant parasitic, the ON resistance $R_{ON}$ [17]. Switch resistance across such devices is typically in the range of 1000 to 5000Ω. Modern Metal-to-Metal (M2M) anti-fuse technology achieves resistances as low as 15 to 25Ω per anti-fuse [1, 2]. The use of such advanced technologies will surly improve the accuracy and bandwidth of the routing networks which will improve the overall accuracy and bandwidth of the FPAAs and thus opening new markets for these devices.

Routing networks generally have two interconnection levels, local and global. The local network connects the CAB cells with their neighbor cells, while the global network connects a cell with any other cells on the FPAA. The use of global network results in more flexibility, but also leads to excessive long signal interconnections. This introduces phase errors and cross-talk problems detrimental to the circuit operation at high frequencies [6]. Fortunately, in contrast to the global network, which is just used for special implementations, the local network is fundamental for realizing a wide range of applications.

### 2.1.3 Computer Aided Design Tools

Designing using Field-Programmable devices is automated through the use of Computer Aided Design (CAD) tools. These tools synthesize circuits from schematic, high level, or behavioral descriptions into usable hardware. Automated CAD-tools reduces the need for detailed design expertise in developing working hardware and provides the power and convenience enjoyed by digital designers. As a consequence, CAD makes hardware analog design open to a greater number of consumers. With accompanying easy-to-use CAD programs and windows-based integrated design environments (IDEs), engineers can now define complete analog functionality on a PC screen, view the results instantly and download the circuitry on to the associated chip by only clicking a button [18-24, 53].

## 2.2 Technology Considerations

Accuracy and bandwidth are considered as the main critical parameters when specifying the design of a CAB. In general, a compromise of one of these parameters while optimizing the other is to be done. In order to achieve this goal, both the continuous-time and the discrete-time techniques have been used in designing to-date CABs for general purpose FPAAs. Following is a brief description of these two approaches.

### 2.2.1 Continuous-Time Approach

CABs of continuous-time FPAAs are typically designed using differential MOS transconductances as programmable resistors. In such designs, the CAB achieves its programmability by varying the values of these transconductances. Examples of such FPAAs are presented in [15, 16]. In these FPAAs, the configuration transconductor is part of the transfer function. Thus, there is no loss due to switch resistance $R_{ON}$. However, the overall transfer function is dependent on the transconductance which is sensitive to both environmental and manufacturing variations. Also, the allowable dynamic range ( The input range within which the accuracy is better than a limit decided by the user, e. g. 5% margin) of the overall CAB will be limited by transconductance linearity.

Another possible method of designing continuous-time CABs is by using device-based building blocks. This method proofs to have higher performance and higher signal swing than the former method. In this technique, CABs can be op-amp based,

current conveyor based, or operational transconductance amplifier (OTA) based circuits. Examples of OTA-based CABs were presented in [26-28]. The programmability of the CABs is achieved by changing the biasing currents of the OTAs used in the circuits. Examples of Op-amp based FPAAs can be found in references [6] and [8]. CABs of such FPAAs have a relatively low operation bandwidth limited by that of the op-amp. The programmability of the CABs is obtained by using banks of resistors and capacitors in conjunction with static switches. Current conveyor based FPAAs were presented in [11, 17, 30-32]. The programmability of the CABs of such FPAAs is obtained by using either tunable resistors and capacitors, or by adjusting the biasing currents of the current conveyors. Due to the features of current conveyors, these designs promise to have larger bandwidths than structures based on op-amps. Figures (2-1), (2-2), and (2-3) show examples of CABs based on OTA, op-amp, and current conveyors, respectively.

The region of operation of the transistors is another major factor of determining the overall performance of the CAB circuits. While sub-threshold circuits techniques offers advantages in terms of low power consumption, the speed and dynamic range of these circuits are quite poor making them less attractive. A sub-threshold based FPAA was presented in [15]. This analog array consists of a collection of homogeneous CABs that are capable of handling special functions needed for neural network applications.

More description of these FPAA designs is given in the literature review at page 19.

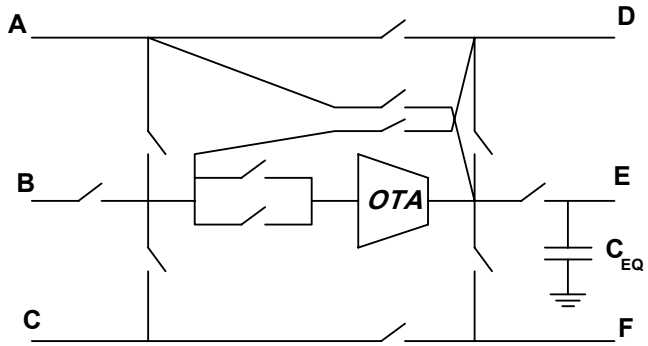



**Figure 2-1** Example of OTA-based CAB cell [26, 27]. The cells of this configuration get their configurability from the set of switches shown in the circuit diagram. The capacitor is formed of bank of capacitors of fixed values with switches to give the circuit its programmability.

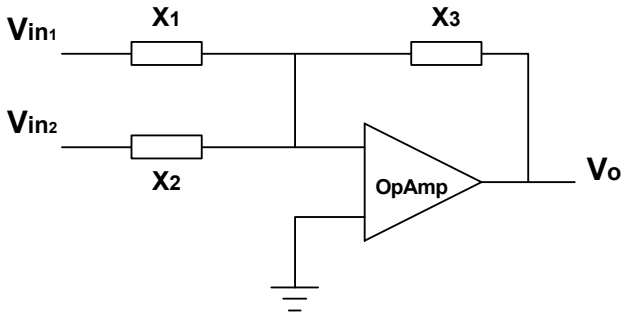



**Figure 2-2** Example of op-amp based CAB cell [6]. The cell gets its configurability from the elements X1, X2, and X3 which can be programmable resistors, programmable capacitors, or even diodes.

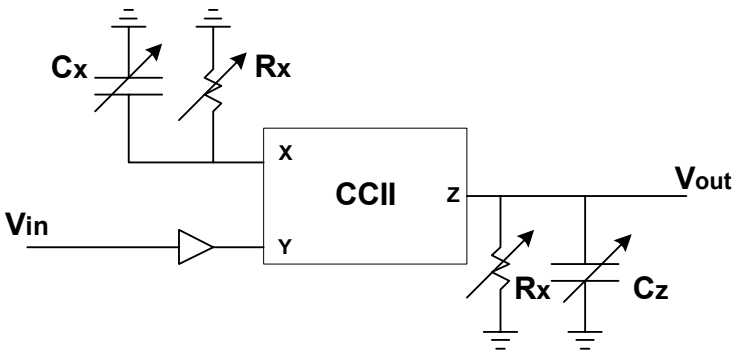



**Figure 2-3** Example of current-conveyor based CAB cell [29]. The cell gets its configurability from the variable resistors and capacitors. As in Figure (1-2), the variable capacitors are formed of banks of capacitors with fixed values and switches.

### 2.2.2 Discrete-Time Approach

Discrete-time approach can be considered as an intermediate category between analog and digital. This is because in discrete-time systems the signal is presented by continuous amplitude of an electrical quantity, just like in analog, but only at discrete time instances, as in digital. Discrete-time designs are basically based on either Switched Capacitor (S/C) or Switched Current (S/I) techniques [14, 19, 20, 22, 38, and 43]. Using these techniques, circuits can be fabricated utilizing standard digital MOS technology, and hence, these circuits can be placed on the same chip with digital circuitry. The programming and reconfiguration of the CABs are done using clock phases. S/C CABs usually consists of an op-amp surrounded by switched capacitor feedback network and routing resources.

In discrete-time circuits, the signals are transmitted as charges which are not subject to loss due to switch resistance. This gives this technique an advantage over the continuous-time technique in terms of enhanced performance. Another advantage of discrete-time circuits is that these circuits can be tuned accurately by adjusting the ratio of capacitors, which can be easily achieved in a CMOS process. This technique has also advantages in terms of wider programming range of its parameters over their continuous-time counterpart.

However, discrete-time circuits have serious disadvantages. The sampled-data nature of discrete-time circuits require pre- and post-processing filters for anti-aliasing and reconstruction (smoothing) respectively. Such circuits are also limited to signal frequencies significantly lower than the clock frequency. This makes the bandwidth

of these circuits 5 to 10 times lower than that of a continuous-time equivalent circuit. Another disadvantage of such technique is that the values of the parameters of a CAB are dependent on the used clock frequencies. If these frequencies changed due to any reason, the CAB parameters will be subject to change [11-14, 19, 20, and 23].

The Anadigm FPAA and IMP EPAC are examples of commercial discrete-time FPAAs with bandwidths of 500 kHz and 150 kHz respectively [19, 20, and 22].

## 2.3 Continuous-Time Current-Mode Design Technique

Analog circuits are always requested to work at high frequencies where digital signal processing (DSP) faces difficulties with implementation. In particular, recent increasing needs of wireless communications, such as W-CDMA (Wide-Band Code Division Multiple Access) [57], BLUETOOTH [58], and ITS (Intelligent Transportation Systems) [59], require analog circuits which process signals in a Giga-hertz frequency range. In addition to this very important requirement, an increased emphasis on improved performance specifications in such applications is also needed. Continuous-time current-mode analog circuits seem to be the most promising solution to pursue these requirements [60, 61]. Continuous-time current-mode analog design techniques have a lot of very important advantages that justify this trend. Among these advantages are the following;

- Given that the semiconductor technologies advance rapidly, high-frequency can no longer be defined in terms of numbers, but rather as

an attribute of an electronic circuit to operate at or near to the transition frequency $f_T$ [12]. The transition frequency is the maximum signal frequency supported by a given technology. Considering current-mode techniques, high impedance nodes are not present in current-mode circuits, and therefore their bandwidth approaches the device $f_T$ [62].

- The growing market of portable devices and the technology scaling are deriving the supply voltages of digital circuits down to 1.2v by the year 2004 and to 0.9v by the year 2008, according to the Semiconductor Industrial Association roadmap [63]. At the same time, the migration toward System-on-Chip- (SoC) adds pressure on analog circuits to follow this trend [64]. However, threshold voltage is not proportionally reduced for scaled down technologies [61]. Thus, the reduction in power supply voltages extremely restricts voltage-signal swings making it difficult to design voltage-mode analog circuits with high linearity and wide dynamic range. Since the current-signal swings are not restricted by the power supply voltages, current-mode circuits are more suitable for such designs and can handle such requirements.
- In contrast to discrete-time circuits, continuous-time current-mode circuits are realizable with scaled low voltage digital IC technologies, i.e. CMOS and/or BiCMOS processes, without floating precision

linear capacitors. This makes such circuits more compatible with digital systems.

- Using continuous-time techniques instead of discrete-time ones results in smaller chip size and lower power consumption. This is mainly due to the absence of the need for anti-aliasing and reconstruction filters in continuous-time systems.

In summary, continuous-time current-mode circuits are capable of implementing high frequency and high performance systems under low power supply voltages. These systems can also be fully compatible with digital processes making it possible to fabricate field programmable analog and digital arrays on the same chip.

## 2.4 Proposed CAB Approach

The proposed CAB architecture is based on a regular pattern of cells interconnected locally for high frequency performance. Unlike the global (matrix-like) routing, the local routing allows only feed forward connections. This is to assure maximum possible bandwidth. Programming of the functions and the parameters of the analog cells are to be basically achieved by modifying the cell's biasing conditions. This can be achieved using OTA-based circuits, current conveyor based circuits, or even at transistor level. In order to be able to get the maximum possible bandwidth of these cells and in order for the design not to depend on the used device bandwidth but on the transistor's $f_T$, these cells are designed on the transistor level utilizing the

TransLinear Principle (TLP) [65]. In order not to degrade their frequency performance, the use of switches in programming these CABs is also restricted to the extreme extent.

What is considered a single cell is to some degree an arbitrary decision. A cell in one programmable device might be considered as a collection of cells, or a macro-cell, in others. However, it is convenient to think of a single cell as a unit capable of performing some elementary mathematical functions which can be used to fully express wide variety of desired system. In this research, the adopted set of functions consists of seven elementary mathematical functions, namely; ADD, NEGATE, AMPLIFY, DIFFERENTIATE, INTEGRATE, LOG, and ANTI-LOG functions. These same functions were adopted by the TRAC FPAA and were realized based on op-amps surrounded by banks of capacitors and resistors. The programmability of TRAC cells are achieved using an extensive number of switches. The integrate and differentiate functions were implemented using external capacitors. The use of op-amp based realization of the CABs limits the bandwidth of these circuits to a range of frequencies of several 10s of kHz up to nearly 4 MHz. The extensive use of switches in programming the circuits also enforces limitations on the performance of the CABs.

The proposed circuits in this research are continuous-time current-mode transistor-based circuits that depend on the BJT translinear principle TLP.

The following subsections present a more detail look at the CAB's architecture and the method of design used in realizing the circuits representing the adopted functions.

### 2.4.1 Functional Requirements

The inclusion of addition and negation to the functions set is fairly obvious. These two functions can be considered as the most basic elementary functions. The implementation of such functions in current domain is a rather easy task. Adding two currents can simply be realized by connecting the branches of these currents to the same node. Negation is necessary to perform subtraction and it can be realized using cross mirroring. As these two operations can be done at the routing network itself when connecting the output of one CAB to the input of another one, no special circuit is presented for them.

Integration and differentiation are another two basic linear processing operations that are required in nearly any analog system. It is easy to implement integrators and differentiators if some kind of electronic switches, such as MOSFET pass transistors, are available. These switches can be used to program the unity-gain frequency by connecting or disconnecting a number of capacitors. However, the extensive use of switches and capacitors will result in parasitic time-constants which can severely degrade the frequency response of the circuit [12]. Thus, switchless current mode integrators and differentiators with tunable characteristics are highly recommended.

A number of designs for continuous-time transistor-based integrators can be found in the literature. Examples of these designs can be found in references [39, 66-78]. One very attractive design of integrators for high frequency applications is the one presented by Seevinck [67], Figure (2-4). The integrator presented was a class AB differential integrator that consists mainly of two translinear loops and two grounded

capacitors. The unity-gain bandwidth of the integrator is limited only by the used transistor's $f_T$ and is tunable by the DC bias current $I_o$ according to the following relation;

$$f_{ug} = \frac{I_o}{2\pi C V_T} \tag{2-1}$$

where $f_{ug}$ is the unity-gain bandwidth of the integrator, $C$ is the used grounded capacitor, and $V_T$ is the thermal voltage, 0.026 V at room temperature. However, the circuit in its present form is not suitable for CABs applications since it is not switchable. Also this circuit is useful only for very high frequency application. To clarify this point, suppose $C$ = 20 pF, for $f_{ug}$ = 5 MHz we need $I_o \approx 15$ $\mu$A. If $f_{ug}$ needs to be lower, the biasing current will be very small and it will be heavily affected by the base currents of the other transistors resulting in non-accurate results. In Chapter three a new integrator circuit that depends mainly on Seevinck integrator is presented but with these two problems solved.

Ideas used in realizing the integrator circuit are also used to realize the differentiator circuit presented in Chapter three.

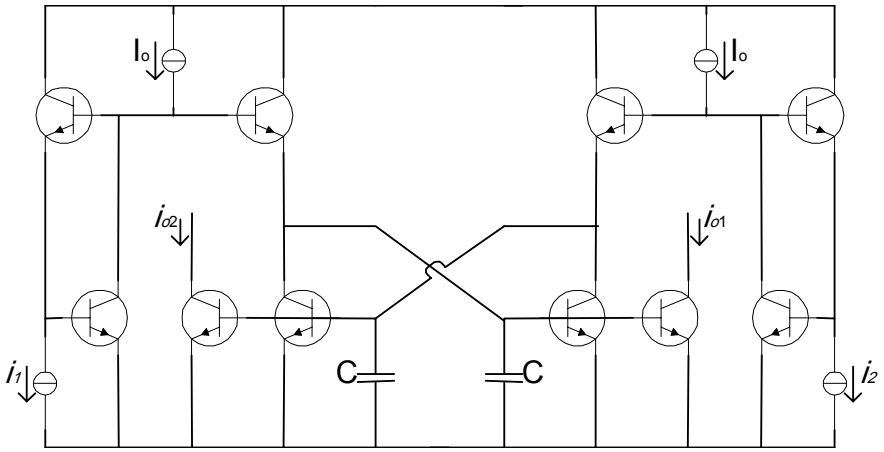



**Figure 2-4** The class AB differential current-mode integrator proposed by Seevinck. $i_{in} = i_1 - i_2$, and $i_o = i_{o1} - i_{o2}$ [67].

The logarithmic and anti-logarithmic (exponential) functions are other very fundamental and basic functions. Representing numbers by their logarithms brings much greater potential to the computational problem. The multiplication of two numbers is reduced to simple addition of their respective logarithms, division becomes subtraction, and raising to power can be achieved simply by multiplying of the logarithm by the required exponent. These circuits can find wide applications also in areas such as instrumentation, telecommunication, and neural network. This justifies the continuing interest in developing log- and anti-log circuits manifested by the relatively large number of publications in this area, see for example references [79-98].

Traditionally, log/anti-log function circuits can be realized in bipolar technology by exploiting to advantage the inherent exponential characteristics of the pn junction [79, 81-83, 91-93]. In a similar way, such circuits can be realized in CMOS technology with MOSFETs working in the subthreshold region. This approach, however, is not very attractive as it results in circuits with very limited bandwidth. Alternatively, pseudo-functions can be implemented using MOSFETs working in the saturation region [80, 84, 86-90, 94-96]. Although this technique results in circuits working at higher frequency ranges than the previous one, the dynamic range of these circuits is very limited. On the other hand, current-mode circuits enjoy the attractive features of wide bandwidths and wide current signal dynamic range even with low power supply voltages.

Recently, two bipolar current-mode exponential function generator circuits have been reported [91, 92]. The first circuit [91], can realize an exponential function of the form

$$I_{out} = C_1 \exp(C_2 I_{in}) \qquad (2\text{-}2)$$

where $C_1$ and $C_2$ are constants, $I_{out}$ is the output current and $I_{in}$ is the input current. However, in this circuit $I_{in}$ must be positive. Thus, the circuit can not realize a true exponential function circuit where the input current can attain arbitrary positive or negative values. The second circuit [92] approximates equation (2-2) by an exponential function plus a term linearly proportional to the input. If this linear term can be ignored, the circuit in [92] can approximately realize the exponent function.

In order to realize equation 2-2 without approximation, a current-mode bipolar circuit is developed in chapter three. In this circuit, not only $I_{in}$ can have arbitrary value but also the constant $C_1$, making the circuit the most general among the others with the maximum dynamic range. A switching feature is added to the circuit to make it suitable to be part of the designed CAB.

Another circuit to realize the log function is also presented in Chapter three. This circuit has the same features as that of the exponential circuit except that it has no switching capability. In order to suit this circuit to be part of the designed CAB, either a Pass circuit or a simple switch can be added to it as discussed in chapter three.

### 2.4.2 Supplementary Circuits

In order to configure and program the CAB's functions and parameters, supplementary circuits are needed. These supplementary circuits consist mainly of two parts; the digital controlling part and the digitally programmed current sources.

The digital controlling part is basically an interface between the user CAD tool and the CABs. This interface can be considered as a serial (or of course parallel) port that provides the controlling word resulting from the CAD tool to a memory cell. One example of a possible memory cell is simple D-latchs. The digital control word is divided into two parts, the configuration part and the programming part. The configuration part is formed from three digits which are the inputs of a Decoder responsible for determining the functionality of the CABs. These three digits are sufficient to cover all functions. The programming part is the input to the flip-flops responsible of controlling the values of the other programmable biasing currents sources.

A number of possible programmable current sources can be found in the literature; see for example the ones presented in [99-105]. However, and as the main objective here is just to use these current sources to facilitate the investigation of the performance of the CABs when configured as a FPAA, the simple current source presented in [104] that directly converts the digital word into its equivalent analog current is used. This current source will be discussed in more details in Chapter three.

## 2.5 Implementation Technology Considerations

Continuous-time CABs can be implemented using CMOS, Bipolar or BiCMOS technologies. In spite of its high cost, there is no doubt that BiCMOS in theory covers the needs most comprehensively, considering analog and digital content together with soft programmability. The analog content is fundamental, and the requirement for a logarithmic element clearly favors bipolar. In addition, linear voltage-to-current conversion is also important, and this too, is more readily achieved in bipolar technology due to the availability of resistors [6].

Aspects on the digital side are largely concerned with programmability and power consumption. Whilst bipolar processes can offer analog and digital mixed signal capability, CMOS has clear advantages in static power consumption. In addition, there are CMOS processes that allow the implementation of non-volatile memory, albeit at a significant increase in processing complexity and consequent cost. There is also the need for a good quality switch to connect the on-chip components in circuit. An appropriate switch element is much easier to be implemented in CMOS technology rather than in bipolar [6, 106].

In this research, the main circuits forming the CABs are designed assuming bipolar technology. However, due to the need for digital programmability, other supplementary circuits such as the programmable current source, the routing network and the control circuitry are all assumed to be implemented using CMOS.

# CHAPTER 3

# PROPOSED CAB CIRCUITS ARCHITECTURE

This chapter presents the proposed circuits architectures used in building a single configurable analog block (CAB). The proposed circuits are based on current –mode translinear-principle (TLP) approach. Programmability of the functions and the parameters of the analog sub-cells are achieved by modifying cell's biasing conditions. Use of switches in programming the operation-mode of these CABs is restricted to the extreme extent in order not to have any of them in the signal path and thus to maintain the frequency performance of these CABs underrated.

In this research, the adopted set of functions each CAB is capable to perform consists six elementary mathematical functions, namely; ADD, NEGATE, DEFERENTIATE, INTEGRATE, LOG, and ANTI-LOG functions.

The inclusion of addition and negation to the functions set is fairly obvious. These two functions can be considered as the most basic elementary functions. The implementation of such functions in the current domain is a rather easy task. Adding

two currents can simply be realized by connecting the branches of these currents to the same node. Negation is necessary to perform subtraction.

Circuit implementation of the integral function is presented in the first following section. Simulations and discussion of the performance of this circuit is also presented in the same section. The second section presents a circuit architecture that realizes the differentiation, pass, and exponential functions. The operation mode of this circuit depends on switching ON or OFF some current sources. The third section discusses the implementation of the natural logarithm function.

In all proposed implementations, the output current is taken as the difference between two sub-output currents. This is to ensure the reduction of signals injected from the clocks and the power supply and thus making them suitable for mixed VLSI implementations. Having the output as the difference between two sub-output currents has the advantage of doubling the maximum output swing.

## 3.1 Integrator Circuit

The general transfer function of a lossy integrator can be given as

$$T(s) = \frac{a}{s+b} \tag{3-1}$$

where ***a*** and ***b*** are constants. The constant ***b*** represents the cutoff frequency of this integrator. Setting this constant to zero results in a lossless integration operation.

Following is a fully-differential circuit realization of the transfer function given in equation (3-1).

### 3.1.1 Circuit Description

Exploiting the current-mode integrator proposed by Seevinck [67] and shown in Figure (2-4), the Integrator circuit shown in Figure (3-1) is developed. This figure shows the proposed current-mode fully differential Integrator circuit. As in Seevinck's Integrator, this circuit consists mainly of two translinear loops (TLL) and two matched grounded capacitors. The first translinear loop is formed from $Q_1$, $Q_2$, $Q_3$, $Q_4$, $Q_5$, $Q_6$, $Q_7$, and $Q_8$ *or* $Q_9$, and the second is formed from $Q_{11}$, $Q_{12}$, $Q_{13}$, $Q_{14}$, $Q_{15}$, $Q_{16}$, $Q_{17}$, and $Q_{18}$ or $Q_{19}$. Depending on the first translinear loop, we can write

$$I_{in1} \cdot I_A \cdot I_A = I_B \cdot I_{o1} \cdot \left[ I_{o2} + i_{c1} + I_X \right] \tag{3-2}$$

The current flowing through the collector of a BJT transistor $I_{co}$ can be represented in terms of the voltage drop between the base to emitter of that transistor $V_{be}$ as

$$I_{co} = I_s \exp\left( \frac{V_{be}}{V_T} \right) \tag{3-3}$$

or simply

$$V_{be} = V_T \ln\left( \frac{I_{co}}{I_s} \right) \tag{3-4}$$

where $V_T$ is the thermal voltage which evaluates to 25.85mV at 300k, and $I_s$ is the BJT saturation current. $V_T = KT/q$ where, $q$ is the electrical charge on an electron, $k$ is Boltzmann's constant, and $T$ is the absolute temperature in Kelvin.

Noting that the voltage drop across the capacitor is the same as the base-to-emitter voltage drop of $Q_9$, the current flowing through this capacitor can be written as

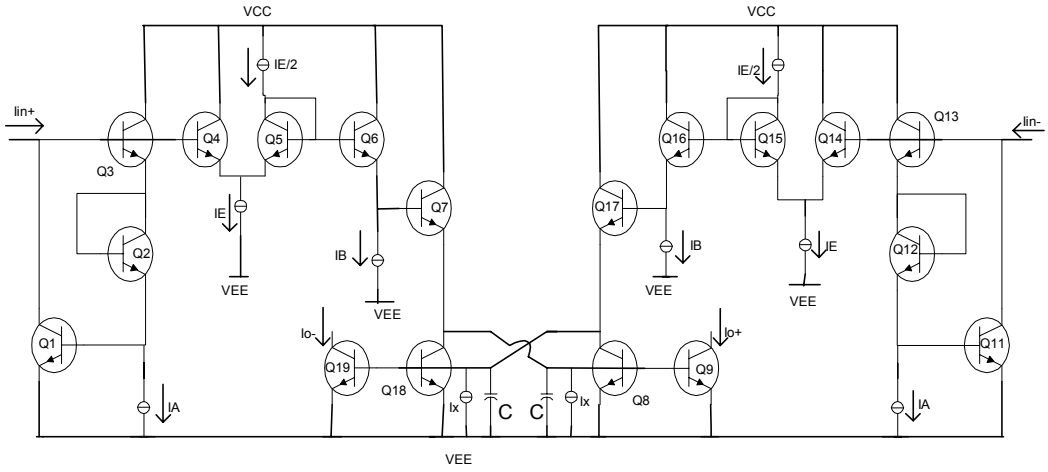



**Figure 3-1** Proposed current-mode differential Integrator Circuit.

$$i_{c1} = C\frac{dV_{c1}}{dt} = CV_T\frac{d}{dt}\left(\ln\frac{I_{o1}}{I_s}\right) = CV_T\frac{1}{I_s}\frac{I_s}{I_{o1}}\frac{dI_{o1}}{dt} \tag{3-5}$$

Substituting equation (3-5) in equation (3-2), we get

$$I_{in1}\cdot I_A{}^2 = I_B\cdot\left[I_{o1}\cdot I_{o2} + C\cdot V_T\cdot\frac{dI_{o1}}{dt} + I_{o1}\cdot I_X\right] \tag{3-6}$$

Similarly, for the second translinear network, we have

$$I_{in2}\cdot I_A{}^2 = I_B\cdot\left[I_{o1}\cdot I_{o2} + C\cdot V_T\cdot\frac{dI_{o2}}{dt} + I_{o2}\cdot I_X\right] \tag{3-7}$$

Subtracting equation (3-7) from equation (3-6) results in

$$I_A{}^2\cdot\left[I_{in1} - I_{in2}\right] = I_B\cdot C\cdot V_T\cdot\frac{d\left[I_{o1} - I_{o2}\right]}{dt} + I_B\cdot I_X\cdot\left[I_{o1} - I_{o2}\right] \tag{3-8}$$

Defining $I_{in}$ as

$$I_{in} = I_{in1} - I_{in2} \tag{3-9}$$

and $I_o$ as

$$I_o = I_{o1} - I_{o2} \tag{3-10}$$

equation (3-8) can be rewritten in the **s**-domain as

$$I_o = \frac{I_A^2}{sI_BCV_T + I_BI_X}\cdot I_{in} \tag{3-11}$$

Rearranging equation (3-11), we get

$$\frac{I_o}{I_{in}} = \frac{I_A^2/(I_BCV_T)}{s + I_X/(CV_T)} = \frac{a}{s+b} \tag{3-12}$$

Obviously equation (3-12) represents the standard transfer function of a lossy integrator (equation 3-1). The constant ***a*** is tunable via the biasing currents $I_A$, $I_B$, and the constant ***b*** is tunable via the current source $I_X$.

In this implementation and in order to have correct biasing conditions for all transistors, the input current must contain in addition to the AC component, a DC one. The overall quantity of this input must be of positive value. One possible representation of such inputs is as

$$I_{in}^{-} = I_k\left[1-\frac{x}{2}\right] \tag{3-13}$$

$$I_{in}^{+} = I_k\left[1+\frac{x}{2}\right] \tag{3-14}$$

and

$$I_{in} = I_{in}^{+} - I_{in}^{-} = x \tag{3-15}$$

where $I_k$ is a constant current to insure suitable biasing and $x$ is a modulation index.

### 3.1.2 Simulation Results and Discussion

As equation (3-12) suggests, the values of both constants $a$ and $b$ of the proposed integrator can be independently tuned via current sources $I_A$, $I_B$ and $I_X$. The tuning range of these parameters thus depends on the range available for the related current sources. Another very important factor that limits the tuning range of these parameters is the selected value of the grounded capacitors. Typical value of such on-chip capacitors are in the order of 10pF's. One possible value of these capacitors usually used in literature is 20pF. This needs a chip area equivalent to less than one

bonding pad. Depending on this value, the parameter *b*, which represents the cutoff frequency $f_c$ can be expressed as

$$f_c = \frac{I_X}{CV_T} = \frac{I_X}{20\times10^{-12}\times25.85\times10^{-3}} = 1.934\times10^{12}\times I_X \qquad (3\text{-}16)$$

Theoretically speaking, and as $I_X$ is not a biasing current, this current source can take any value and thus $f_c$ can be tuned to any needed frequency. However, the minimum possible $f_c$ is actually limited by the minimum possible practical value of $I_X$ without affecting the accuracy of the performance of this circuit. A close look at the circuit of Figure (3-1) indicates that the minimum possible $I_X$ is affected mainly by the base currents of transistors $Q_8$ and $Q_9$ on one side and $Q_{18}$ and $Q_{19}$ on the other side. Thus, the effective value of this current can be expressed as

$$I_{X_{eff}} = I_X + 2\cdot I_{Base} \qquad (3\text{-}17)$$

where $I_{Base}$ is the base current of either $Q_8$ or $Q_9$. Thus the minimum possible cutoff frequency depends mainly on the values of these base currents.

In order to minimize the effect of these currents, transistors with larger $\beta$ can be used. However, on one hand this will not totally eliminate the effect of these currents, and on the other hand it may impose limitations on the cutoff frequency of the BJT transistors. Adding appropriate compensation currents to the current source $I_X$ itself can force the effective current to be equal to the actual needed value and thus dramatically enhance the performance of the circuit. The value of such compensation current must equal $2I_{Base}$. However, the value $I_{Base}$ depends on the input currents and thus is expected to vary depending on the desired cutoff frequency of the integrator.

Fortunately, the variations of $I_{Base}$ around $I_{Base0}$, the base current when the input signal is zero, are of minor effects. As such choosing the compensation current to be equal to $I_{Base0}$ is expected to enhance the performance.

In order to investigate the effect of the base currents on the minimum possible cutoff frequency the gain-frequency and the phase-frequency of the integrator cell of Figure (3-1) is simulated using Pspice. In these simulations, the results were obtained assuming transistors to have the default parameters except with $\beta$ = 450. Figure (3-2) shows the obtained results for the gain-frequency and the phase-frequency characteristics respectively when taking $I_A$ = 0.1$m$A, $I_B$ = 1$m$A, and $I_E$ = 1$m$A. To compensate for the base currents, the current source $I_X$ is assumed to have negative values and thus to be the simulation parameter. The results are compared also to the target.

From these Figures one can see that by proper adjustment of $I_X$ to compensate for the base currents of $Q_8$ and $Q_9$, and $Q_{18}$ and $Q_{19}$, it is possible to decrease the range of usable bandwidth down to 10 KHz with a phase shift error of about $30^o$, and 100 KHz with a phase shift error less than $5^o$.

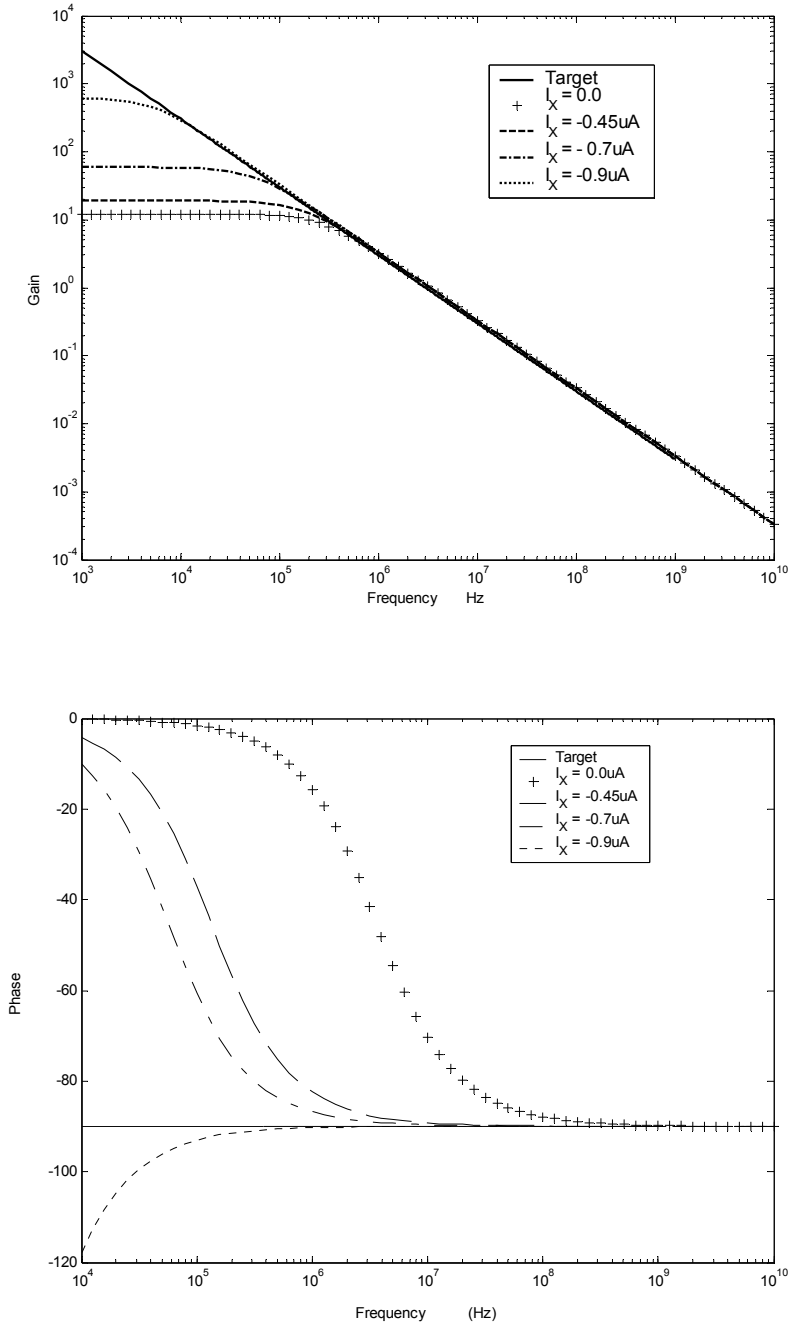



**Figure 3-2** Gain- and Phase-Frequency characteristics of the proposed integrator circuit. Default transistor parameters with $\beta$ = 450 are assumed. $I_A$ = 0.1$m$A, $I_E$ = 1$m$A and $I_B$ = 1$m$A.

In order to examine the effects of the other current sources levels on the performance

of the integrator circuit, the same simulation is repeated for different values of $I_A$, $I_B$ and $I_E$. Figure (3-3) shows the gain-frequency and phase-frequency simulation results of the integrator cell under same parameters as in Figure (3-2) but with $I_A = 0.5m\text{A}$ rather than $0.1m\text{A}$. Of course and as equation 3-12 suggests, increasing $I_A$ will result in an increase in the gain proportional to the square of $I_A$. From Figure (3-3), it can be seen that as $I_A$ increases the DC gain will increase. However, increasing the DC gain results in smaller usable bandwidth due to larger output currents that derives the circuit into saturation. The new cutoff frequency is 100 KHz with a phase shift error of around $30^o$. For phase shift error limited to $5^o$, the cutoff frequency is around 1 MHz. Increasing the voltage range of the power supply may partially solve this problem. However, it is not advisable to increase the power supply voltage because this will result in higher power consumption. Thus care must be taken when choosing the DC gain in order not to derive the circuit into saturation within the desired bandwidth. If a gain is required, a separate gain-stage can be added.

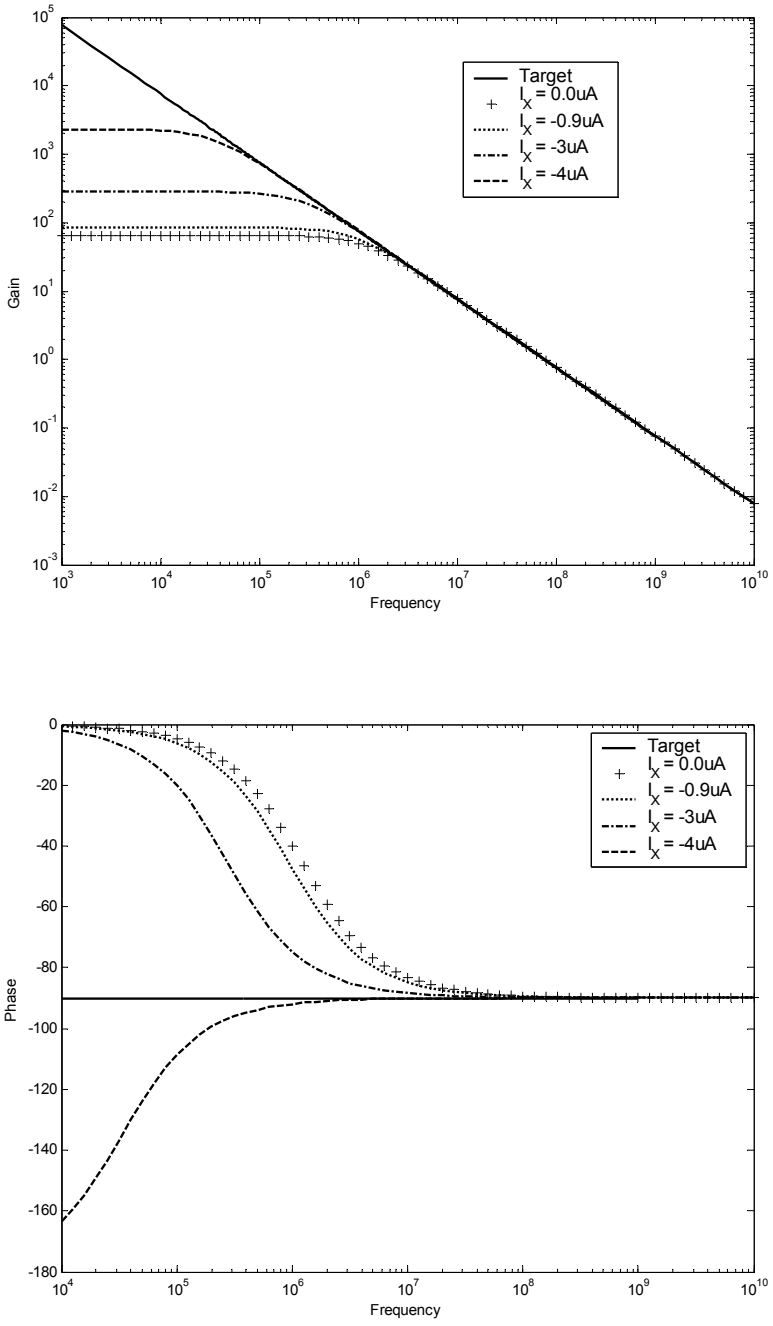



**Figure 3-3** Gain- and Phase-Frequency characteristics of the proposed integrator circuit. Default transistor parameters with $\beta$ = 450 are assumed. $I_A$ = 0.5$m$A, $I_E$ = 1$m$A and $I_B$ = 1$m$A.

Increasing $I_B$ is expected to have counter effect on the DC gain as predicted from equation (3-12). In order to study its effect, the circuit performance is simulated under the same conditions of Figure (3-3), *i.e.* with $I_A = 0.5m$A and $I_E = 1m$A, but with $I_B = 5m$A rather than $1m$A. Figure (3-4) shows the simulation results for this case. Once again we note here that it is easier to get more accurate lossless integration performance for lower DC gains. The new cutoff frequency is 20 kHz with phase error of $20^o$ and 500 kHz with phase error of $5^o$.

The current sources $I_E$ and $I_E/2$ are believed to have minor effects on the characteristics of the integrator cell due to the use of the additional transistors to bias transistors $Q_5$ and $Q_6$, and $Q_{15}$ and $Q_{16}$. Figure (3-5) shows the simulation results with $I_A = .1m$A, and $I_B = 1m$A taking $I_E$ as a parameter. From these simulations it can be seen that changing the value of $I_E$, within certain limits of course, does not have any effect on the frequency response of the integrator circuit. This behavior is expected since $I_E$ does not appear in the derivation for the transfer function of the proposed circuit. In this circuit and in all coming circuits, $I_E$ will be either ON with a value of $1m$A or OFF to disable the corresponding circuit.

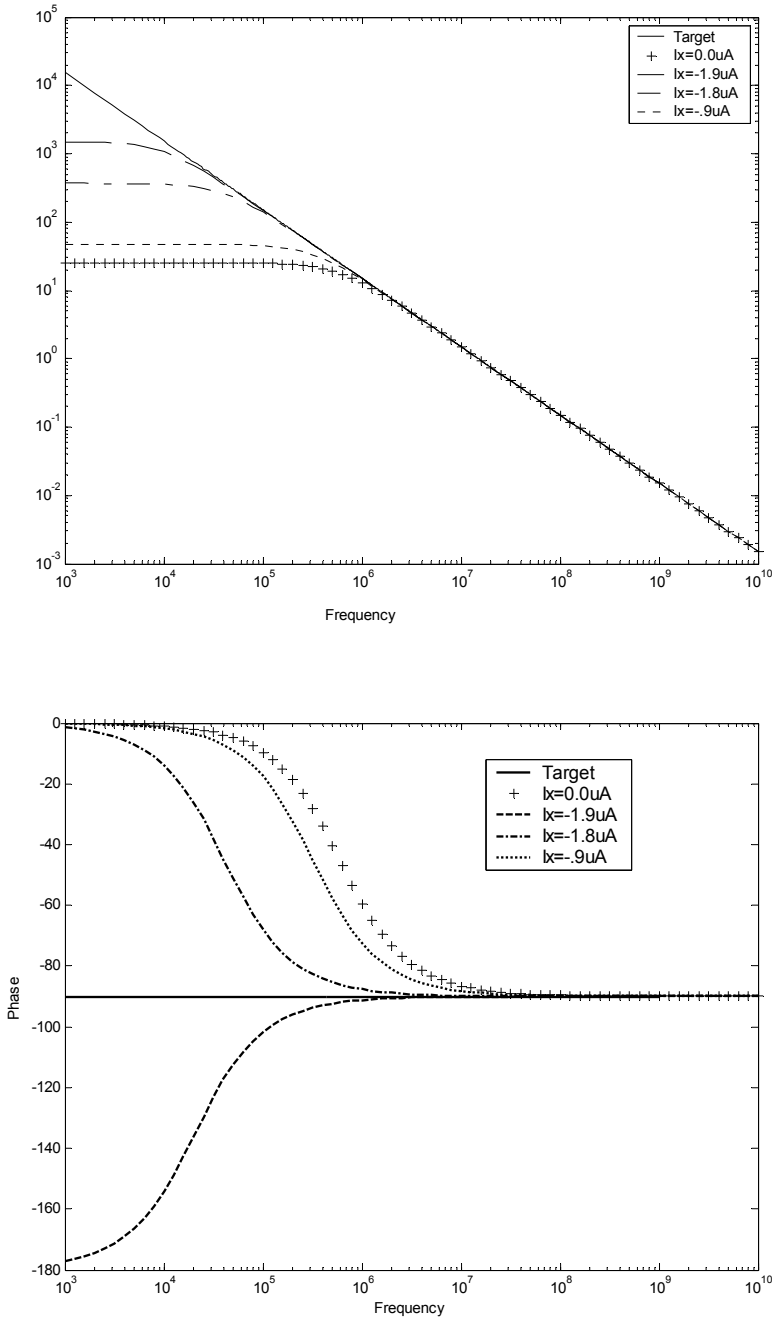



**Figure 3-4** Gain- and Phase-Frequency characteristics of the proposed integrator circuit. Default transistor parameters with $\beta$ = 450 are assumed. $I_A$ = 0.1$m$A, $I_E$ = 1$m$A and $I_B$ = 5$m$A.

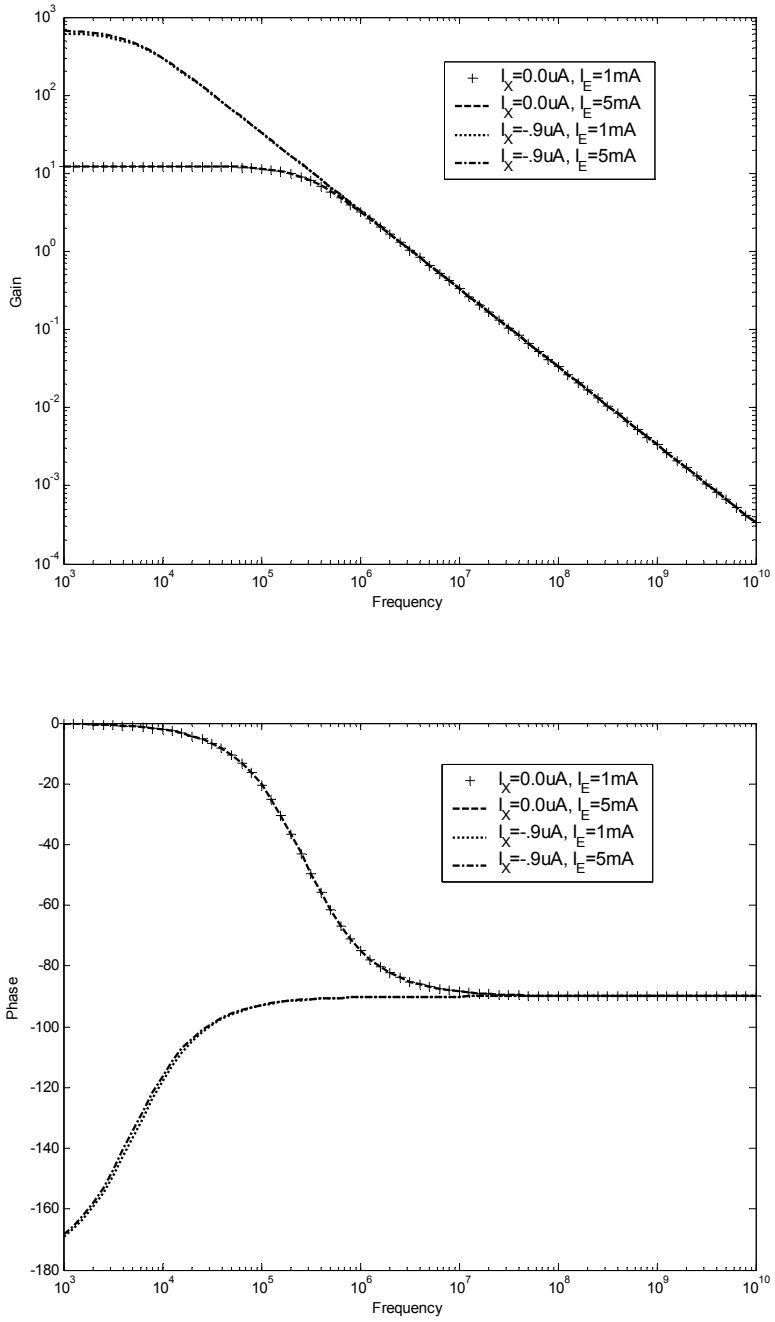



**Figure 3-5** Gain- and Phase-Frequency characteristics of the proposed integrator taking $I_E$ as a parameter. Default parameters with $\beta$ = 450 are assumed. $I_A$ = 0.1$m$A and $I_B$ = 1$m$A.

In order to investigate the performance of the proposed circuit as a lossy integrator, the circuit is simulated for different values of $I_X$. The results of these simulations are shown in Figure (3-6) for both the gain and the phase characteristics respectively. For these simulations $I_B = 1mA$, and $I_E = 1mA$. The DC gain of the integrator is adjusted to be constant via $I_A$ alone. The Figures show also the effect of applying practical transistor parameters using the BFP640 Infineon$^{@}$ which has $\beta = 450$ on the performance of the circuit. From these figures we can see good matching between the results of the two cases. However, at high frequencies, one can note some irregularities in the performance especially in the phase frequency characteristics. This is due to the non idealities of the transistor used and mainly due to the cutoff frequency of the used transistor. If transistors with larger cutoff frequency are to be used, this will surly shift these irregularities to higher frequencies.

The previous discussion shows the effect of finite $\beta$ over the performance of the integrator circuit. It also shows the possibility of using compensation currents to enhance the performance of the integrator. Another possible factor that may result in deviations in the expected performance of the proposed integrator circuit is temperature. As it can be seen from equation (3-12) the transfer function of this circuit is temperature sensitive through $V_T$.

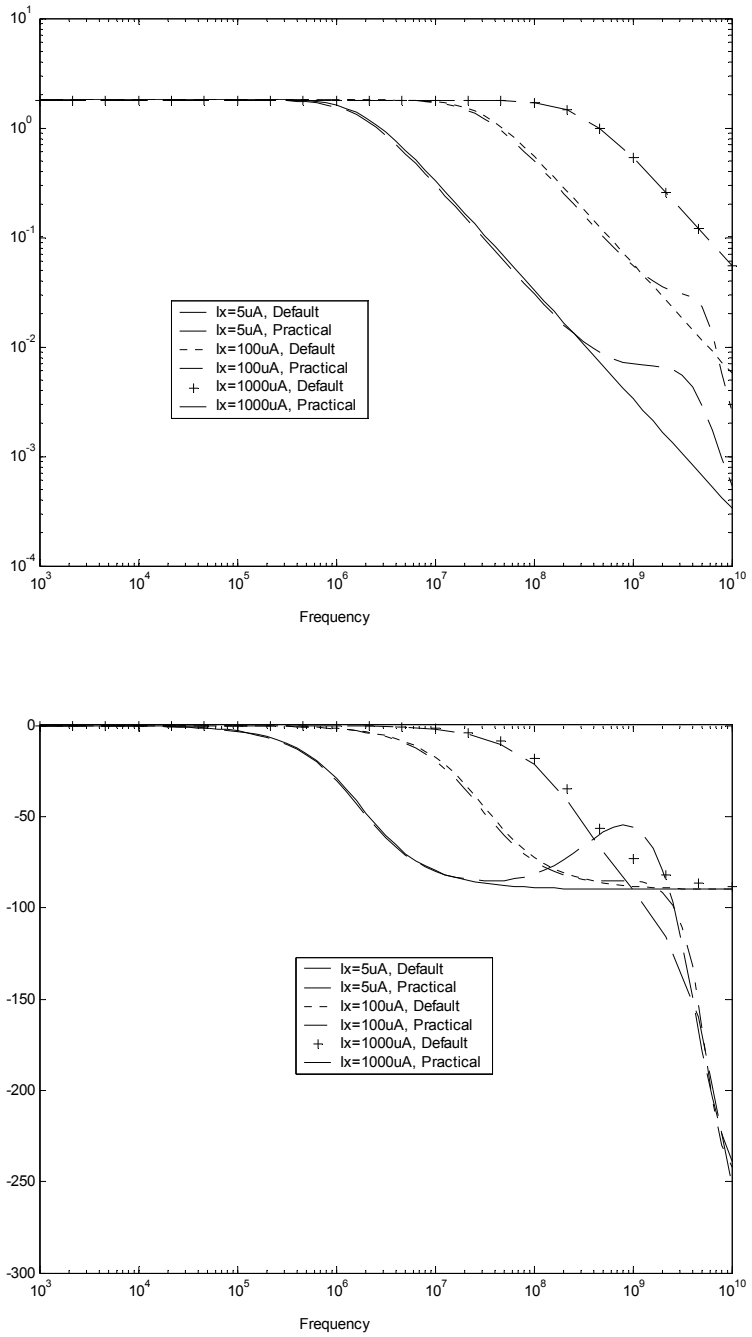



**Figure 3-6** Gain- and Phase-Frequency characteristics of the proposed lossy integrator taking $I_X$ as a parameter. Default parameters with $\beta$ = 450 compared to practical parameters.

Assuming lossless integrator, the transfer function can be rewritten as

$$\frac{I_o}{I_{in}} = \frac{I_A^2/(I_B C V_T)}{s} = \frac{a}{s} \tag{3-18}$$

One possible method to make the constant ***a*** temperature insensitive is to have one of the current sources $I_A$ or $I_B$ proportional to or inversely proportional to $V_T$ respectively.

A temperature-dependent current source that can be used here to compensate the temperature effects is the one presented by Kumwachara *et al* in [103] and shown in Figure (3-7). This current source is a low voltage bipolar translinear-based temperature-dependent source with output current given as

$$I_y = k\frac{V_T I_1}{R I_2}\ln\left[k\frac{I_3}{I_4}\right] \tag{3-19}$$

where $k = I_{sN}/I_{sP}$ and $I_{sN}$ and $I_{sP}$ are the saturation currents of NPN and PNP transistors, respectively. The currents $I_1$, $I_2$, $I_3$, and $I_4$ are constant current sources. By adjusting the currents $I_1$ and/or $I_2$ a linear tuning for the output current $I_o$ can be achieved. However, in order to cancel the effects of $V_T$ in equation (3-18), this current source can only be used instead of $I_A$. However, as $I_A$ is of second order, the transfer function will still be temperature sensitive. In order to solve this problem, the current source $I_B$ can be taken as temperature dependent. This will result in using two dependent current sources which will have a serious effect on the overall performance and power consumption of the circuit.

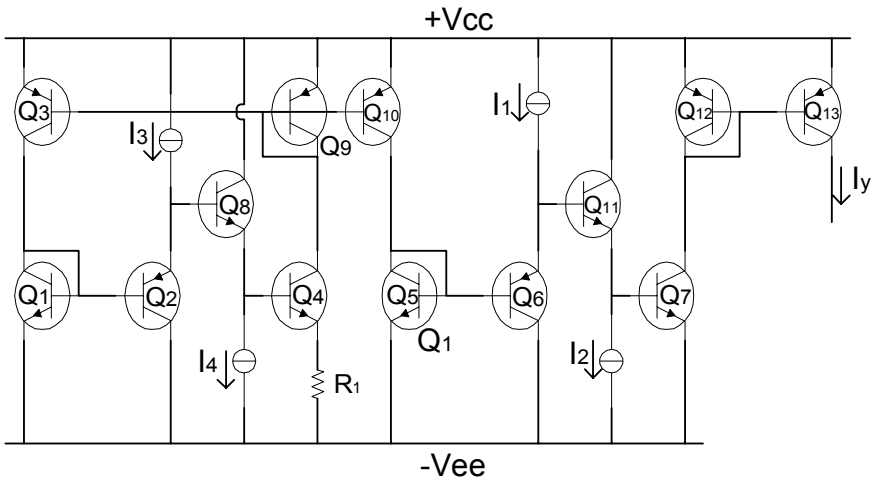



**Figure 3-7** The temperature-dependent current source presented in reference [103]

Another possible way to solve this problem is to rearrange the translinear loops in Figure (3-1) such that the transfer function in equation (3-18) becomes

$$\frac{I_o}{I_{in}} = \frac{I_A I_C /(I_B C V_T)}{s} = \frac{a}{s} \tag{3-20}$$

If this is achieved, then only $I_A$ or $I_C$ needs to be replaced by temperature-dependent current source. Figure (3-8) shows the circuit diagram with rearranged transistors. Following same terminology as in analyzing the circuit of Figure (3-1) and taking $I_X$ as compensation current results in

$$I_A \cdot I_C \cdot \left[I_{in1} - I_{in2}\right] = I_B \cdot C \cdot V_T \cdot \frac{d\left[I_{o1} - I_{o2}\right]}{dt} \tag{3-21}$$

and

$$\frac{I_o}{I_{in}} = \frac{I_A I_C /(I_B C V_T)}{s} = \frac{a}{s} \tag{3-22}$$

Figures (3-9) and (3-10) show the simulation results of this circuit under temperature variations. In Figure (3-9a), the transistors were assumed to have default values with $\beta$ = 450 and no temperature compensation. Figure (3-9b) shows the performance under the previous conditions but with temperature compensation. Figures (3-10a) and (3-10b) show the performance without and with temperature compensation but with practical BJTs parameters. In both cases, the effect of temperature compensation on the performance is shown.

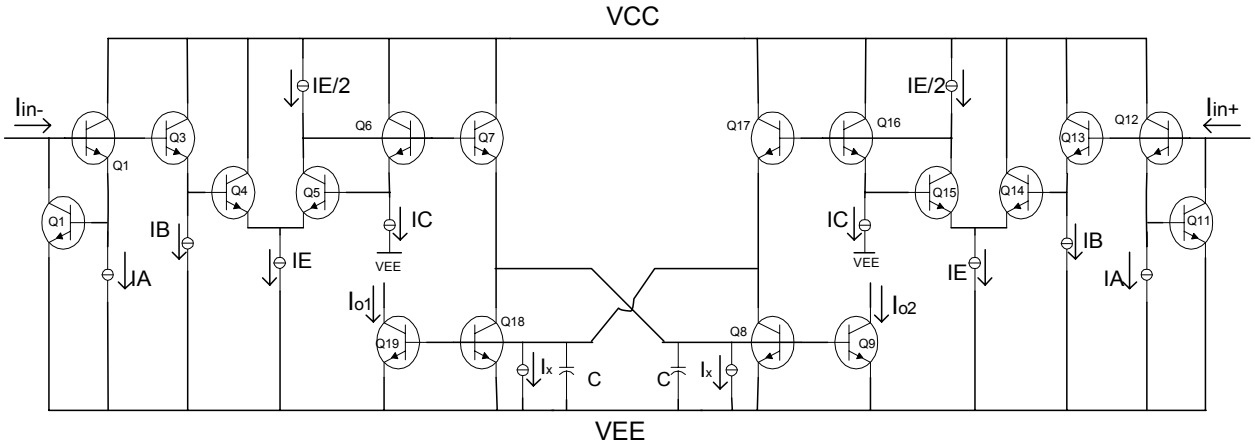
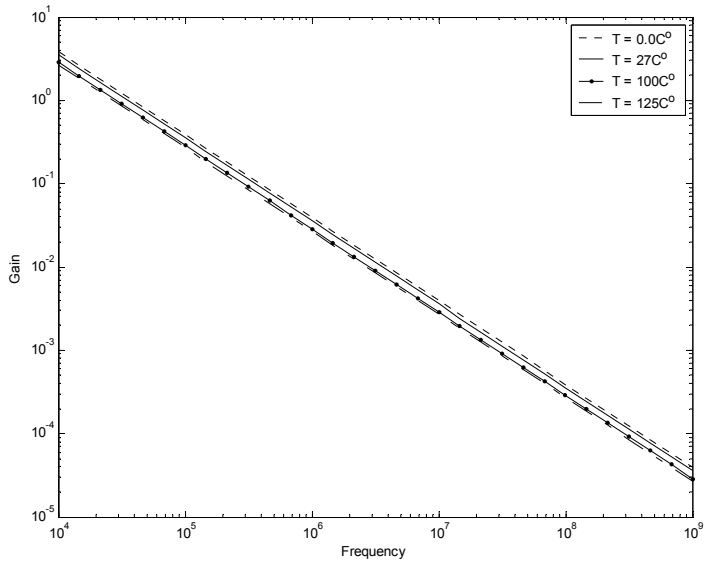
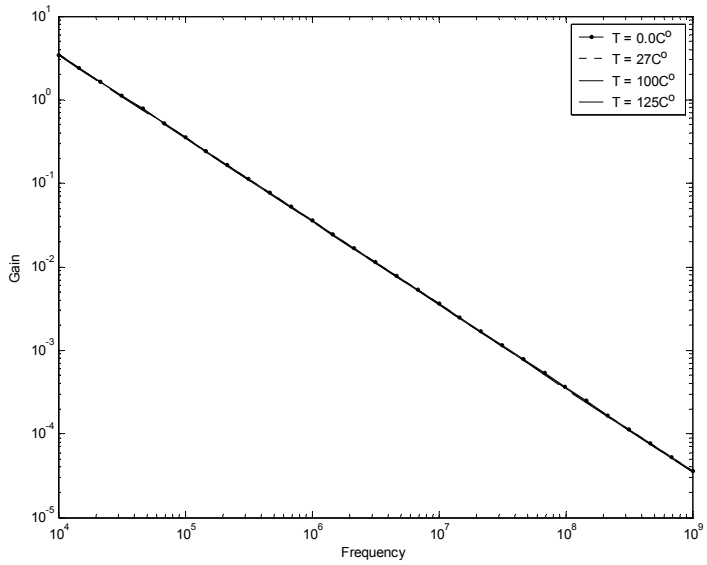



**Figure 3-8** The proposed circuit of Figure (3-1) with rearranged translinear loops to be able to use just one temperature-dependent current source for temperature compensation.

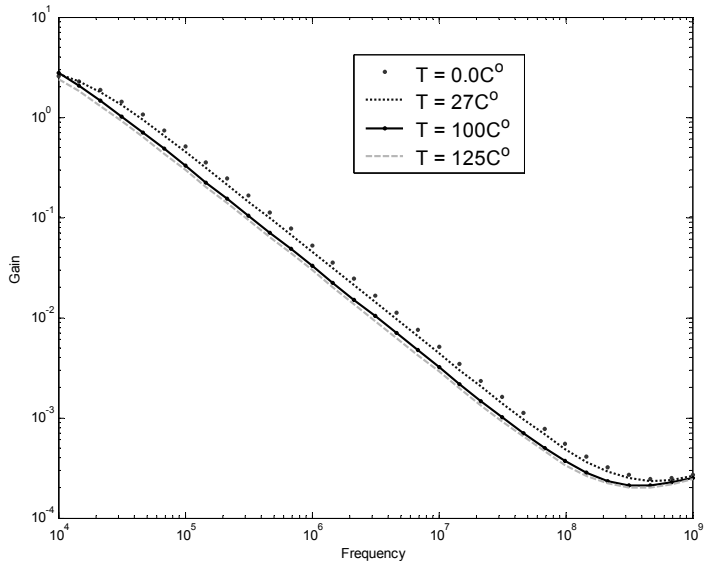



(a) Without temperature compensation

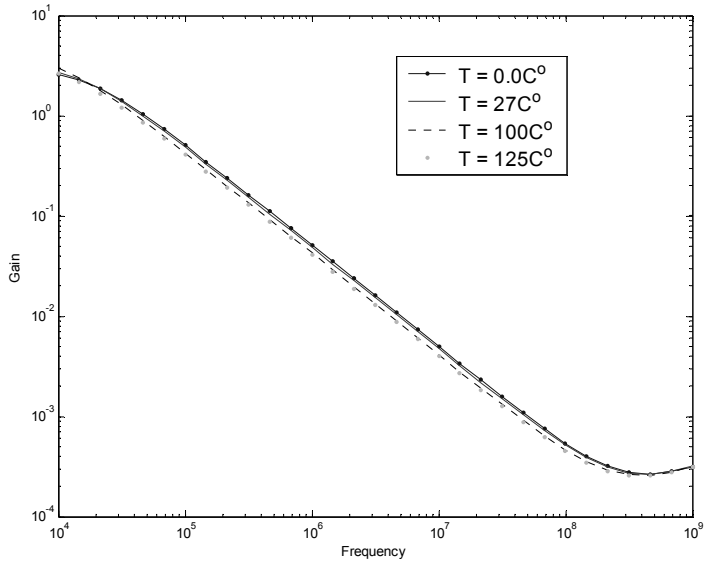



(b) With temperature compensation

**Figure 3-9a, b** Effects of temperature variations on the performance of the integrator without and with temperature compensation respectively. Default parameters with $\beta$= 450 is assumed.




(a) Without temperature compensation




(b) With temperature compensation

**Figure 3-10a, b** Effects of temperature variations on the performance of the integrator without and with temperature compensation respectively. Practical parameters with $\beta$= 450 is assumed.

## 3.2 Differentiator/Exponential-Amplifier/Pass Circuit

Figures (3-11) and (3-12) represent the basic circuit structure of the proposed Differentiator/Exponential-Amplifier/Pass circuit. This circuit structure is split into two circuit diagrams for simplicity. The operation modes of this circuit are programmed via $I_{Ea}$, $I_{Ee}$, and $I_{Ed}$ current sources. Table (3-1) shows the functional modes of this circuit.

**Table 3-1** Operation Modes of the Proposed Circuit

| **Current Source** | | | **Operation Mode** |
|---|---|---|---|
| $I_{Ea}$ | $I_{Ed}$ | $I_{Ee}$ | |
| OFF | ON | OFF | Differentiator |
| ON | OFF | OFF | Pass |
| OFF | OFF | ON | Exponential Amplifier |

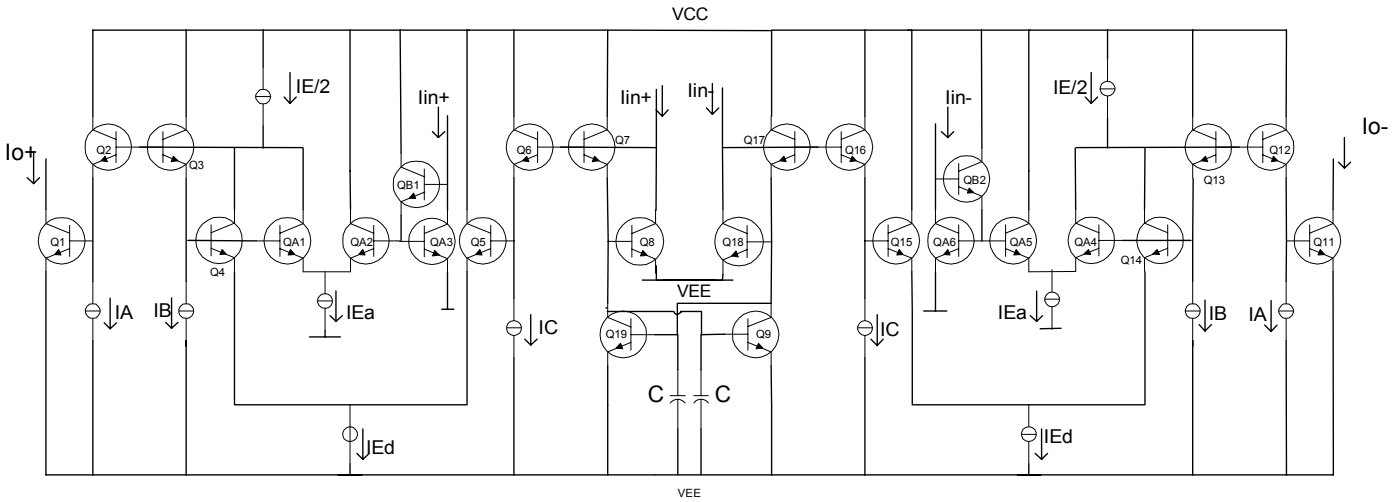



**Figure 3-11** Proposed circuit in the Differentiation/Pass mode

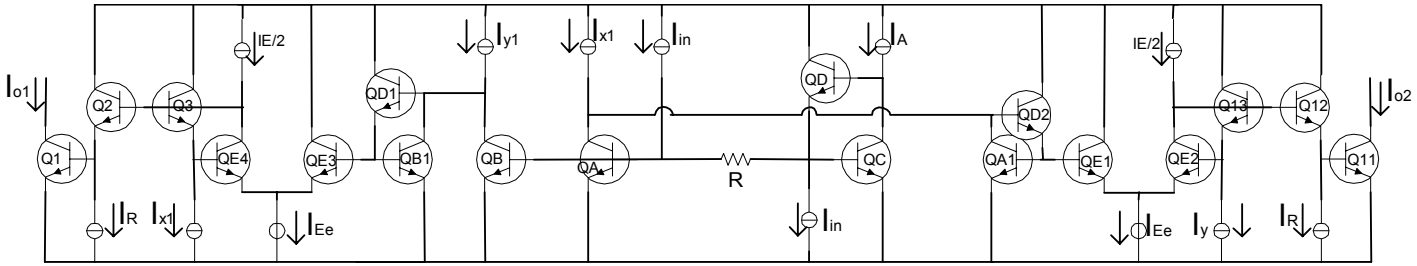



**Figure 3-12** Proposed circuit in the Exponential mode

### 3.2.1 Differentiation Mode

The functional description of the differentiation cell can be represented as follows;

$$f(x) = A \cdot \frac{dx}{dt} \tag{3-22}$$

where $A$ is a constant. In the presented implementation, both the input, $\boldsymbol{x}$, and the output, $f(x)$, are realized via differential currents.

#### 3.2.1.1 Circuit Description

With reference to Figure 3-11, as the current sources $I_{Ea}$, and $I_{Ee}$ switched OFF and $I_{Ed}$ switched ON, the circuit operate as a fully differential differentiator. Neglecting all base currents and applying the translinear principle (TLP) on the two translinear loops formed from transistors $Q_1$, $Q_2$, $Q_3$, $Q_4$, $Q_5$, $Q_6$, $Q_7$, and $Q_9$, and $Q_{11}$, $Q_{12}$, $Q_{13}$, $Q_{14}$, $Q_{15}$, $Q_{16}$, $Q_{17}$, and $Q_{19}$, we can write

$$I_o^+ I_A I_{E/2} I_C = I_B I_{E/2} I_{in}^+ I_{EQ7} \tag{3-23}$$

and

$$I_o^- I_A I_{E/2} I_C = I_B I_{E/2} I_{in}^- I_{EQ7} \tag{3-24}$$

where $I_{EQ7}$ and $I_{EQ17}$ are the currents flowing through the collectors of transistors $Q_7$ and $Q_{17}$ respectively. These currents can be expressed as,

$$I_{EQ7} = I_{in}^- + i_c = I_{in}^- + C \cdot \frac{dv_{be8}}{dt} = I_{in}^- + C \cdot V_T \cdot \frac{1}{I_{in}^+} \cdot \frac{dI_{in}^+}{dt} \tag{3-25}$$

and

$$I_{EQ17} = I_{in}^+ + i_c = I_{in}^+ + C \cdot \frac{dv_{be18}}{dt} = I_{in}^+ + C \cdot V_T \cdot \frac{1}{I_{in}^-} \cdot \frac{dI_{in}^-}{dt} \tag{3-26}$$

where $v_{bei}$ is the base-to-emitter voltage drop of transistor $Q_i$, and $V_T$ is the thermal voltage. By substituting equations (3-23) and (3-24) into equations (3-25) and (3-26), respectively, we get,

$$I_o^+ = \frac{I_B}{I_A I_C}\left[ I_{in}^+ I_{in}^- + C \cdot V_T \cdot \frac{dI_{in}^+}{dt} \right] \tag{3-27}$$

and

$$I_o^- = \frac{I_B}{I_A I_C}\left[ I_{in}^+ I_{in}^- + C \cdot V_T \cdot \frac{dI_{in}^-}{dt} \right] \tag{3-28}$$

Subtracting equation (3-28) from equation (3-27), we get

$$I_o = I_o^+ - I_o^- = \frac{I_B}{I_A I_C} \cdot C \cdot V_T \cdot \frac{d\left(I_{in}^+ - I_{in}^-\right)}{dt} = \frac{I_B}{I_A I_C} \cdot C \cdot V_T \cdot \frac{dI_{in}}{dt} \tag{3-29}$$

Rewriting equation (3-29) in **s**-domain we get,

$$I_o = \frac{I_B}{I_A I_C} \cdot C \cdot V_T \cdot s \cdot I_{in} \tag{3-30}$$

Obviously, equation (3-30) represents the operation of a standard differentiator.

As in the case of integrator circuit, the input currents must contain a DC biasing part to ensure correct biasing conditions. As such, these input currents can be defined as in equations (3-13) to (3-15).

#### 3.2.1.2 Simulation Results and Discussion

As discussed before, in order for the cell to work as a differentiator, both current sources $I_{Ea}$ and $I_{Ee}$ must be OFF, whilst current source $I_{Ed}$ kept ON. A close look at the circuit diagram shown in Figure (3-11) shows that one of the main factors that

may affect the performance of the differentiator circuit is the transistors base currents. Fortunately, the effect of these base currents can be compensated via the dc current sources added to or subtracted from the nominal values of the biasing current sources. However, the base currents of transistors $Q_9$ and $Q_{19}$ can not be simply compensated using these current sources. Taking into consideration these base currents and following the same previous mathematical manipulation, we can write:

$$I_o^+ I_A I_C = I_B I_{in}^+ I_{EQ7} = I_B I_{in}^+ \left( I_{in}^- + I_{Base9} + i_c \right) \tag{3-31}$$

$$I_o^- I_A I_C = I_B I_{in}^- I_{EQ17} = I_B I_{in}^- \left( I_{in}^+ + I_{Base19} + i_c \right) \tag{3-32}$$

substituting for $i_c$ as in equations (3-25) and (3-26), we have

$$I_o^+ I_A I_C = I_B I_{in}^+ I_{EQ7} = I_B I_{in}^+ \left( I_{in}^- + I_{Base9} + C \cdot V_T \frac{1}{I_{in}^+} \frac{dI_{in}^+}{dt} \right) \tag{3-33}$$

$$I_o^- I_A I_C = I_B I_{in}^- I_{EQ7} = I_B I_{in}^- \left( I_{in}^+ + I_{Base19} + C \cdot V_T \frac{1}{I_{in}^-} \frac{dI_{in}^-}{dt} \right) \tag{3-34}$$

Noting that

$$I_{Base9} = \frac{I_{in}^+}{\beta} \tag{3-35}$$

$$I_{Base19} = \frac{I_{in}^-}{\beta} \tag{3-36}$$

Substituting for the base currents in equations (3-33) and (3-34) and subtracting them from each other we get

$$I_A I_C \left( I_o^+ - I_o^- \right) = \frac{I_B}{\beta} \left( I_{in}^{+2} - I_{in}^{-2} \right) + I_B \cdot C \cdot V_T \frac{1}{I_{in}^+} \frac{d}{dt} \left( I_{in}^+ - I_{in}^- \right) \tag{3-37}$$

Comparing equation (3-37) to equation (3-29) shows that the base currents of transistors $Q_9$ and $Q_{19}$ could have a serious effect on the needed standard form of the differentiator cell. However, by simply connecting additional current sources in parallel with the two capacitors, we can compensate the effects of the base currents efficiently.

Figure (3-13) shows the gain-frequency and phase-frequency response of the differentiator cell with and without compensation currents. In these simulations, the transistors are assumed to have the default parameters values with $\beta$ = 450. All DC current sources were taken to be 1$m$A. The simulation results are compared also to the target ones. Out of these graphs the enhancement in performance due to the use of the compensation currents is very clear. Using compensation currents, the lower limit of the usable bandwidth lowered from nearly 500 kHz down to 10 kHz for a phase error less than $5^o$. If the phase characteristics to be ignored, then the lower limit can be reduced to 1 kHz.

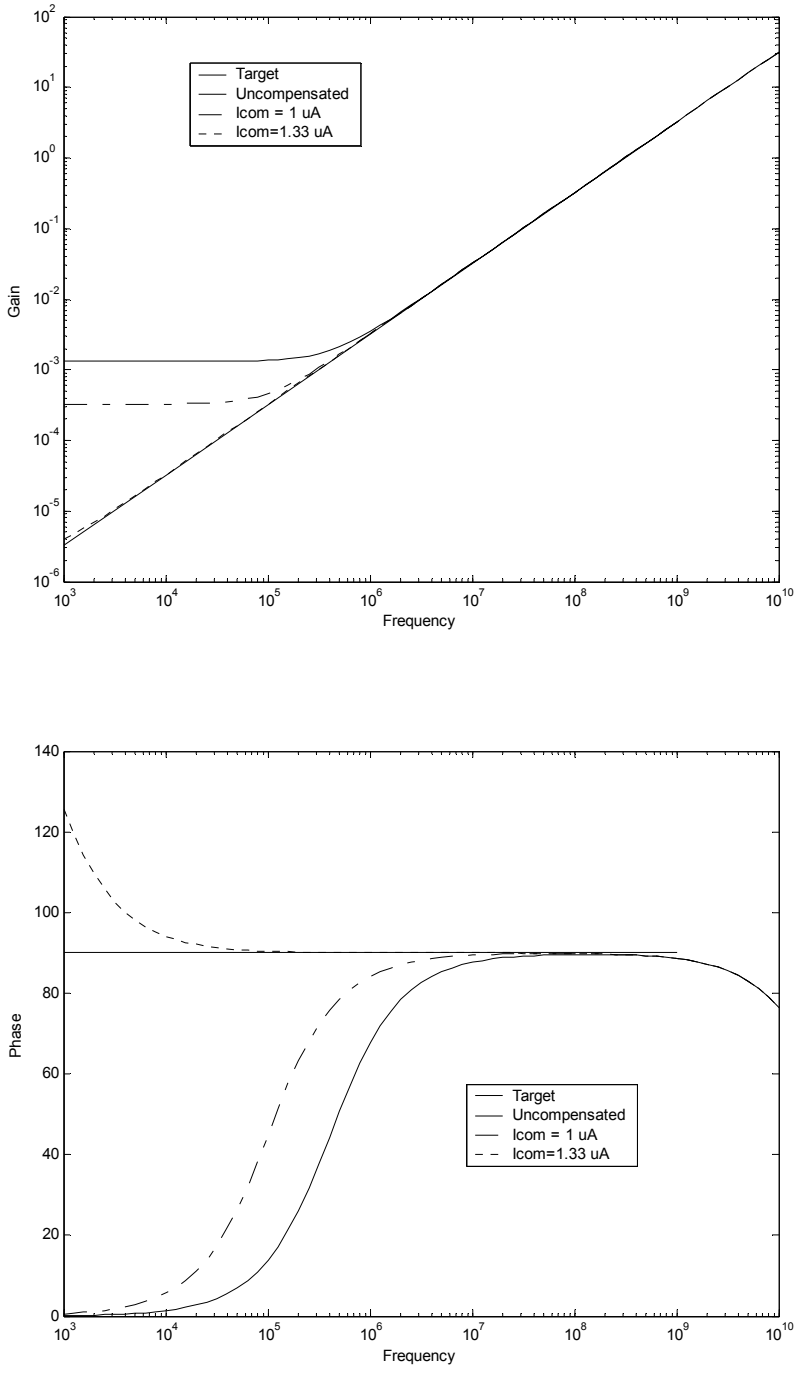



**Figure 3-13** Gain- and Phase-Frequency characteristic curve of the proposed differentiator cell. Default BJT parameters are assumed with $\beta$ = 450. $I_A = I_B = I_C$ = 1$m$A

To study the effect of the other DC current sources on the performance of the differentiation characteristics of the proposed circuit, we take $I_B$ as an example. From equation (3-29), it can be seen that by increasing $I_B$, the gain is expected to increase. Figures (3-14a) and (3-14b) show the gain-frequency and phase-frequency characteristics for different $I_B$ compared to target at a constant compensation current. All other current sources are taken to be like the previous case. It is very clear out of these Figures that increasing (decreasing) current source $I_B$ does increase (decrease) the gain without affecting the performance of the circuit.

To examine the effects of actual possible transistor parameters on the performance of the differentiator cell, the transistor model used previously in the simulations of the integrator circuit are used here to simulate the differentiator cell. Figure (3-15) shows the gain-frequency and phase-frequency characteristic curves of this cell, respectively. In getting these results, all current sources are assumed to have a value of $1mA$. It is obvious that the actual parameters degrade the performance of the cell. However, for the gain-frequency characteristics, the circuit still operates at a relatively wide bandwidth, 40 KHz up to 200 MHz with a maximum error less than 1%. For the phase-frequency characteristics, the circuit can operate with smaller bandwidth, 2 MHz-20 MHz with an error of $1^o$ and 500 KHz-50 MHz with an error of $5^o$.

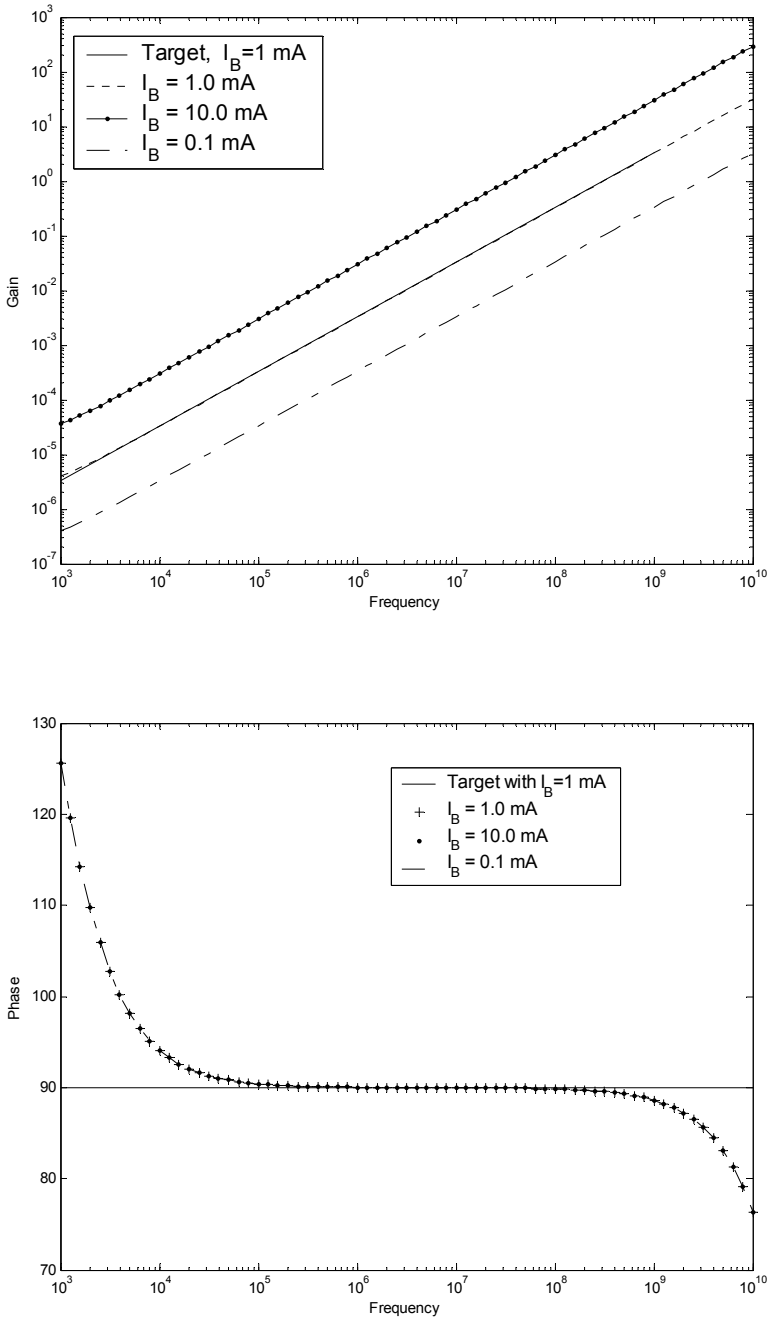



**Figure 3-14** Effect of $I_B$ on the Gain- and Phase-frequency characteristics of the differentiator cell. Default BJT parameters with $\beta$ = 450 and compensation currents are assumed. $I_A = I_C = 1$mA.

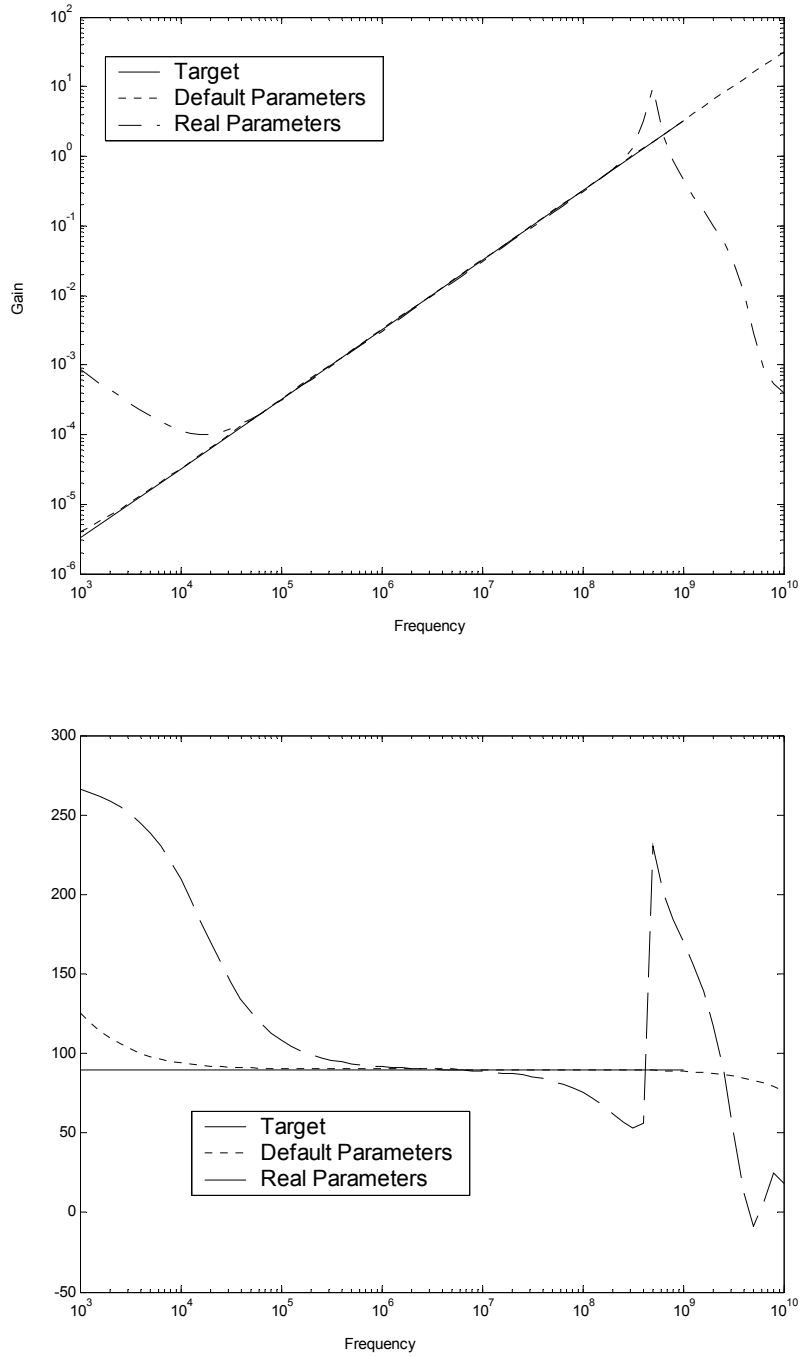
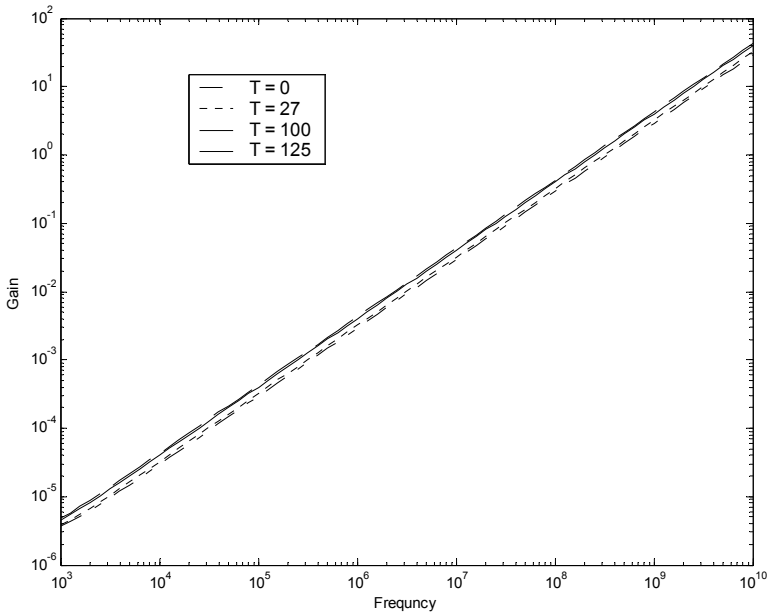


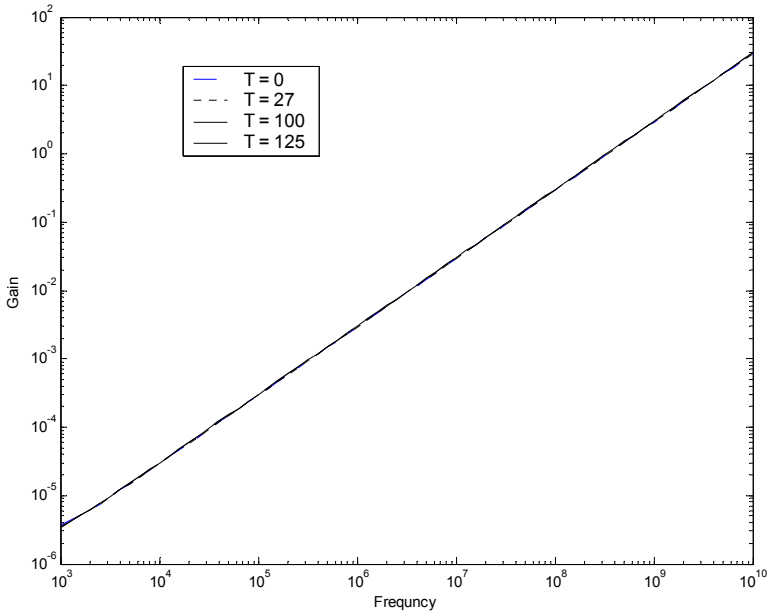

**Figure 3-15** Gain- and Phase-Frequency characteristics of the differentiator cell under real parameters and compensation currents are assumed. $I_A = I_C = 1\text{mA}$.

It is believed that since the only limitation on the bandwidth of this circuit is due to transistor parameters, using better transistor parameters (in terms of higher cutoff frequency, higher dc current gain, and lower parasitic resistances) will result in much better performance.

As the transfer function of the differentiator characteristics is temperature dependent through $V_T$ (equation (3-30)), the same temperature compensation technique used in the integrator section can be used here. For this purpose either the $I_A$ or $I_B$ can be taken as the dependent current source. Figures (3-16) and (3-17) show the simulation results of this circuit under temperature variations. In Figure (3-16a), the transistors were assumed to have default values with $\beta = 450$ and no temperature compensation. Figure (3-16b) shows the performance under the previous conditions but with temperature compensation. Figures (3-17a) and (3-17b) show the performance without and with temperature compensation but with practical BJTs parameters.

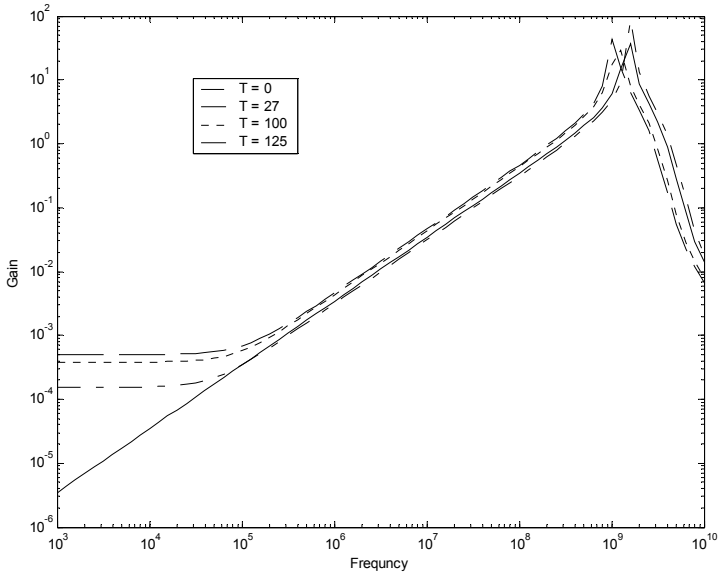



(a) Without temperature compensation

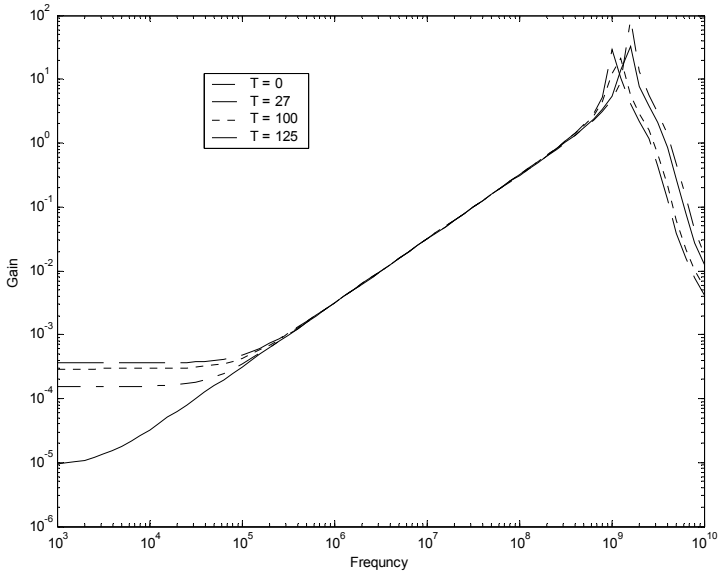



(b) With temperature compensation

**Figure 3-16a, b** Effects of temperature variations on the performance of the differentiator without and with temperature compensation respectively. Default parameters with $\beta$= 450 is assumed.




(a) Without temperature compensation




(b) With temperature compensation

**Figure 3-17a, b** Effects of temperature variations on the performance of the differentiator without and with temperature compensation respectively. Practical parameters with $\beta$= 450 is assumed.

### 3.2.2 Pass Mode

#### 3.2.2.1 Circuit Description

Switching OFF the current sources $I_{Ed}$ and $I_{Ee}$ while the current source $I_{Ea}$ is ON will change the mode of operation of the circuit into a Pass cell. Following the two translinear loops formed from $Q_1$, $Q_2$, $Q_3$, $Q_{A1}$, $Q_{A2}$ and $Q_{A3}$ and $Q_{11}$, $Q_{12}$, $Q_{13}$, $Q_{A4}$, $Q_{A5}$, and $Q_{A6}$, we can write,

$$I_o^+ I_A I_{E/2} = I_B I_{E/2} I_{in}^+ \tag{3-38}$$

and

$$I_o^- I_A I_{E/2} = I_B I_{E/2} I_{in}^- \tag{3-39}$$

Subtracting equation (3-39) from equation (3-38), we get

$$I_o = I_o^+ - I_o^- = \frac{I_B}{I_A}\left(I_{in}^+ - I_{in}^-\right) = \frac{I_B}{I_A} I_{in} \tag{3-40}$$

Equation (3-40) indicates that this cell can not only operate as a Pass cell, but also as a linear current amplifier with an amplification factor dependant on the ratio of $I_B$ to $I_A$.

#### 3.2.2.2 Simulation Results and Discussion

Figure (3-18a) shows the simulation results of this Pass cell. These two Figures compare the circuit performance when assuming the transistors with the default parameters but once again with $\beta$ = 450 to the results obtained when using the actual transistors parameters used before. It is very obvious that the only limitation on high frequency operation is the characteristic of the transistor used, *i.e.* its cutoff

frequency. Using transistors with higher cutoff frequencies is expected to give wider bandwidth of operation. As the gain of this amplifier can be simply adjusted to the desired value via the DC current sources $I_A$ and $I_B$, the base currents effects can be safely ignored.

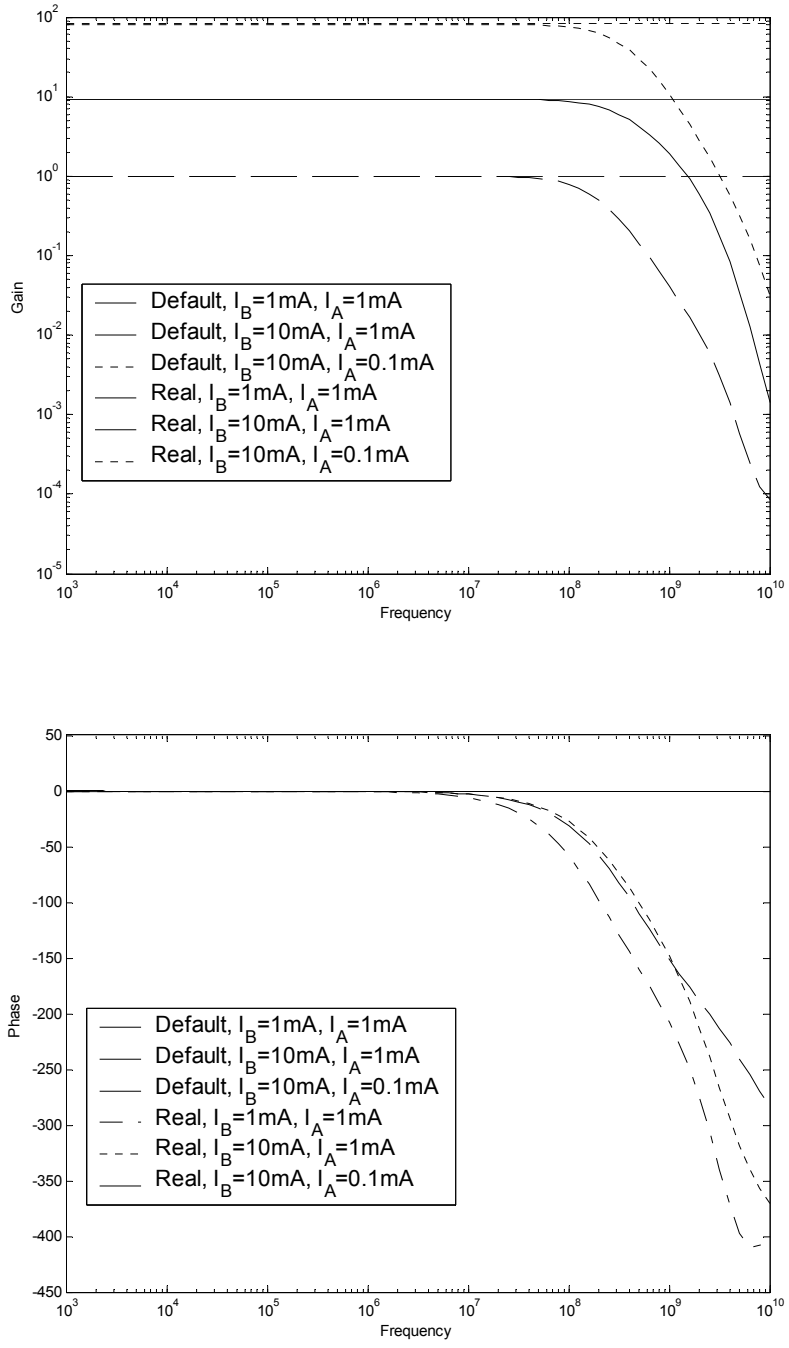



**Figure 3-18** Gain- and Phase-Frequency characteristics of the proposed circuit when configured to operate as a Pass cell.

### 3.2.3 Exponential Amplifier Mode

This subsection introduces the circuit architecture that implements the function;

$$f(x,y) = B \cdot x \cdot e^{A \cdot y} \tag{3-41}$$

where $A$, and $B$ are positive constants. In order to cover the most general case, the input arguments $x$ and $y$ are supposed to be either positive or negative quantities. The proposed circuit implements the function $f(x,y)$ by direct replacement of the variables $x$ and $y$ and the functional $f(.,.)$ with currents.

#### 3.2.3.1 Circuit Description

Switching the current sources $I_{Ea}$ and $I_{Ed}$ OFF and the current source $I_{Ee}$ ON derives the circuit shown in Figures (3-11) and (3-12) to operate as a differential current Exponential Amplifier. Once again, neglecting the base currents of all transistors, then by taking KVL at the loop formed from $Q_A$, $R$, and $Q_C$, we can write

$$V_{BE_A} = I_{in} \cdot R + V_{BE_C} \tag{3-42}$$

where $V_{BEi}$ is the base emitter junction voltage drop of the transistor $Q_i$. Noting that

$$V_{BE_i} \cong V_T \ln\left[\frac{I_{c_i}}{I_{s_i}}\right] \tag{3-43}$$

where $V_T$ is the thermal voltage, $I_{ci}$ is the current flowing through the collector of transistor $Q_i$, and $I_s$ is the respective saturation current, equation (3-42) can be rewritten as

$$V_T \ln\left[\frac{I_{x_1} - I_{x2}}{I_s}\right] = I_{in} \cdot R + V_T \ln\left[\frac{I_A}{I_s}\right] \tag{3-44}$$

Assuming all transistors to have same $I_s$, then equation (3-44) can be simplified to

$$I_{x2} = I_{x1} - I_A \cdot \exp\left(\frac{R}{V_T} I_{in}\right) \tag{3-45}$$

Applying KVL on the loop formed from $Q_B$, $R$, and $Q_C$, and following the same previous steps, we can write

$$I_{y2} = I_{y1} - I_A \cdot \exp\left(\frac{R}{V_T} I_{in}\right) \tag{3-46}$$

Use of TLP in the translinear loop formed by BJTs $Q_{A1}$, $Q_{E1}$, $Q_{E2}$, $Q_{13}$, $Q_{12}$, and $Q_{11}$ yields

$$I_{x2} \frac{I_E}{2} I_{y1} = I_R \frac{I_E}{2} I_{o2} \tag{3-47}$$

Substituting for $I_{x2}$ from equation (3-45) in equation (3-47) yields

$$I_{o2} = \frac{I_{y1} I_{x1}}{I_R} - \frac{I_{y1} I_A}{I_R} \exp\left(\frac{R}{V_T} I_{in}\right) \tag{3-48}$$

Use of TLP in the translinear loop formed by BJTs $Q_{B1}$, $Q_{E3}$, $Q_{E4}$, $Q_3$, $Q_2$, and $Q_1$ and following same steps yields

$$I_{o2} = \frac{I_{y1} I_{x1}}{I_R} - \frac{I_{y1} I_A}{I_R} \exp\left(\frac{R}{V_T} I_{in}\right) \tag{3-49}$$

Subtracting equation (3-48) from equation (3-49) gives

$$I_o = I_{o1} - I_{o2} = \frac{I_A}{I_R}\left(I_{y1} - I_{x1}\right)\exp\left(\frac{R}{V_T} I_{in}\right) \tag{3-50}$$

Assuming that

$$I_{x1} = I_k\left[1 - \frac{x}{2}\right] \tag{3-51}$$

and

$$I_{y1} = I_k\left[1+\frac{x}{2}\right] \tag{3-52}$$

where $I_k$ is a constant current to insure suitable biasing and $x$ is a modulation index, equation (3-50) can be rewritten as

$$I_o = I_{o1} - I_{o2} = \frac{I_A I_k}{I_R} x \exp\left(\frac{R}{V_T} I_{in}\right) \tag{3-53}$$

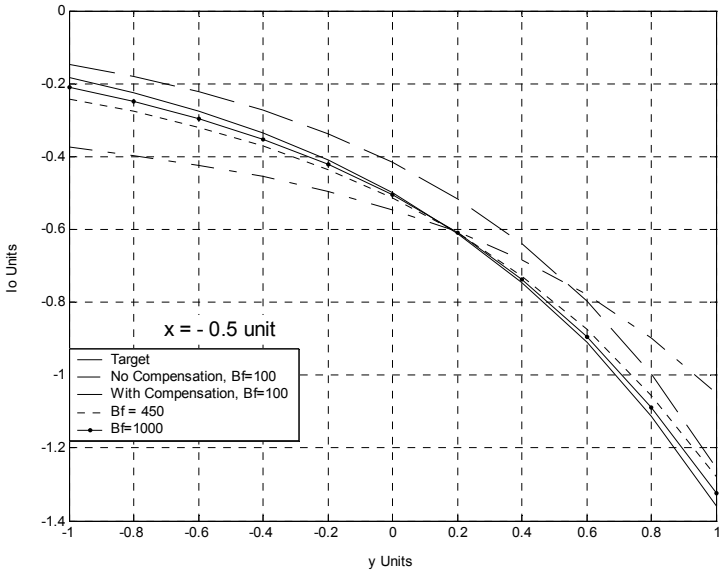
If units express an order of magnitude in amperes (e.g., $10^{-3}$A, $10^{-6}$A, etc.), and if $R$ is chosen to satisfy the relation $R/V_T$ (units) = A, then using $I_{in} = y$ (units) and $I_A I_k/I_R = B$ (units), then $I_o$ in units can be written as

$$I_o = B \cdot x \cdot \exp(A \cdot y) \qquad \text{units} \tag{3-54}$$

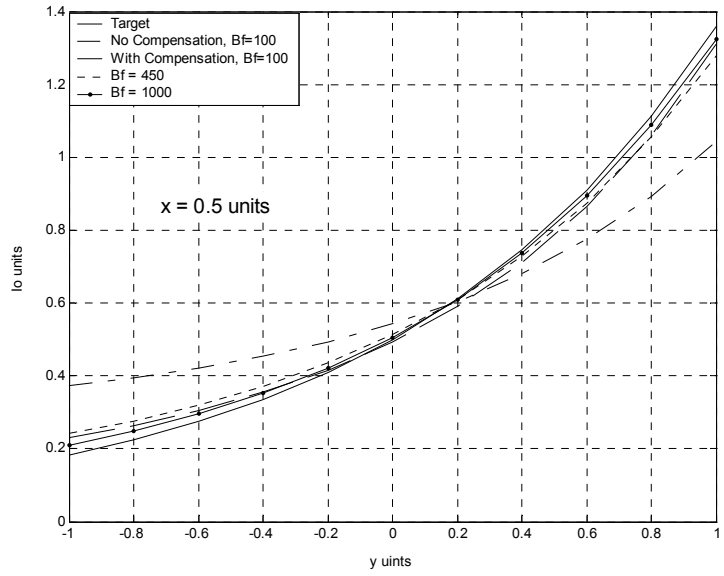
which is the desired function.

#### 3.2.3.2 Simulation Results and Discussion

Figures (3-19a) and (3-19b) present the simulation results of using the proposed circuit as an exponential amplifier. In both Figures, the modulation index $x$ is taken to




(a)




(b)

**Figure 3-19a, b** Simulation results of the performance of the exponential amplifier assuming default transistor parameters with positive and negative *x* respectively.

be constant and the output current is plotted versus the input current represented by the $y$ variable. When comparing the simulated results using default Pspice BJT parameters, where $\beta = 100$, to the target ones, a significant error is noticed. This error is mainly due to the effect of the base currents of the BJTs. The effect of these base currents is partially reduced using the biasing transistors $Q_D$, $Q_{D1}$ and $Q_{D2}$. However, a close look at the proposed circuit shows that as base currents of the transistors $Q_A$ and $Q_B$ are provided via the biasing transistor $Q_D$, the effective current flowing through the resistance $R$ is

$$I_{in_{eff}} = I_{in} - I_{BA} - I_{BB} \tag{3-55}$$

where $I_{BA}$ and $I_{BB}$ are the base currents of both transistors $Q_A$ and $Q_B$ respectively. This effective current is responsible for giving the exponential amplification.

Another effect of the base currents appears on the collector currents flowing through transistors $Q_{E1}$, $Q_{E2}$, $Q_{E3}$, and $Q_{E4}$. As suggested in the analysis of this circuit, it is assumed that the collector currents $I_{E1}$ and $I_{E3}$ must be equal to $I_{E2}$ and $I_{E4}$ respectively. However, as the current source $I_{E1}/2$ must bias transistors $Q_2$ and $Q_3$, the effective current flowing through $Q_{E4}$ is no longer $I_E/2$, it is

$$I_{E4_{eff}} = \frac{I_E}{2} - I_{B2} - I_{B3} \tag{3-56}$$

where $I_{B2}$ and $I_{B3}$ are the base currents of both transistors $Q_2$ and $Q_3$ respectively. This yields a collector current flowing through $Q_{E3}$ equals to

$$I_{E3_{eff}} = \frac{I_E}{2} + I_{B2} + I_{B3} \tag{3-57}$$

A third effect of the base currents appear at the emitter currents of transistors $Q_2$, $Q_3$, $Q_{12}$, and $Q_{13}$. In all these transistors, the effective emitter current will be the current source connected to that emitter terminal added to it another base current.

One possible solution to reduce the effect of the base currents is to partially compensate for them via the current sources themselves. For example, a current source with a value of $I_{BA} + I_{BB}$ can be added in parallel to the input current source $I_{in1}$. This current source will reduce the effect of the base currents on $I_{ineff}$, equation (3-55), and will force it to approximately equal $I_{in}$. However, these two base currents are not constants. Due to the expected symmetrical operation of this circuit (between positive and negative inputs), the best value to be chosen for this compensation current is the value of the two base currents when the input is set to zero, that is

$$I_{comp1} = I_{B2} + I_{B3} \tag{3-58}$$

where $I_{comp1}$ is the compensating current. Compensation current sources can also be added parallel to both current sources $I_{E1}/2$ and $I_{E2}/2$. Once again, and due to expected variation in both current sources $I_{x1}$ and $I_{y1}$, which are representing the modulation index, the best compensation current can be chosen to be $I_R/\beta + I_k/\beta$. $I_k$ here is the central current around which both currents $I_{x1}$ and $I_{y1}$ will vary (equations (3-51) and (3-52)).

The effect of these compensation currents can be seen on the simulation results shown in Figures (3-19a) and (3-19b). Clearly, the use of compensation currents has enhanced the performance of the circuit. One thing to remember here is that there is no need actually to add physical compensation sources. Since all current sources here

are to be programmable, the only thing needed to be done is to introduce the circuit with the suitable effective values of the current sources rather than the nominal ones.

Another possible solution for the base current effects is to use transistors with higher forward current gains ($\beta$). In order to compare the effect of higher $\beta$ to the previous results, simulation results for the same circuit but now with $\beta = 450$ (which equals $\beta$ used in all other previous simulations for the different modes of operation) is shown on the same graphs of Figures (3-19a) and (3-19b). The enhancement in performance due to higher $\beta$ is very clear.

Figures (3-20), (3-21), and (3-22) show the simulation results of the output current versus the input $x$ with $y$ taken as a parameter.

In all above simulations, all current sources are taken in units of $10^{-3}$ A's. Thus, and in order for the $y$ to be in units, the resistor $R$ is taken to be 26 ohms. If the resistor R is to be set to any other value, the normalizing unit can be adjusted through the current sources to any required value.

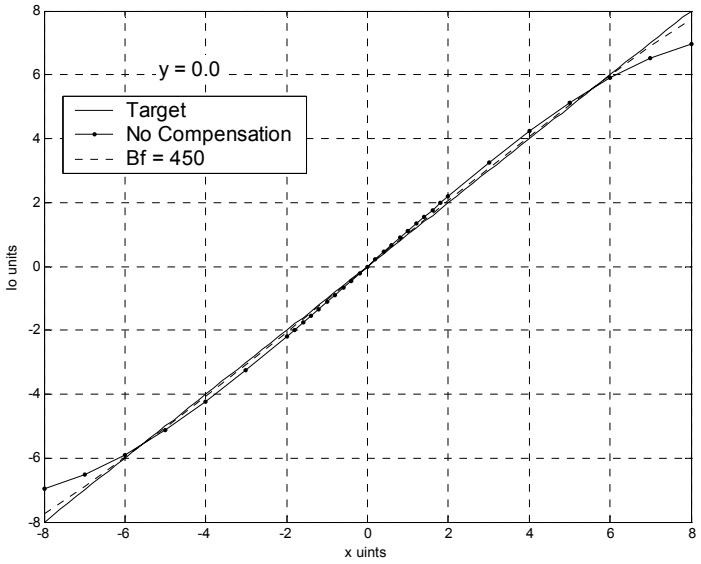



**Figure 3-20** Simulation results of the performance of the exponential amplifier assuming default transistor parameters with $y = 0$.

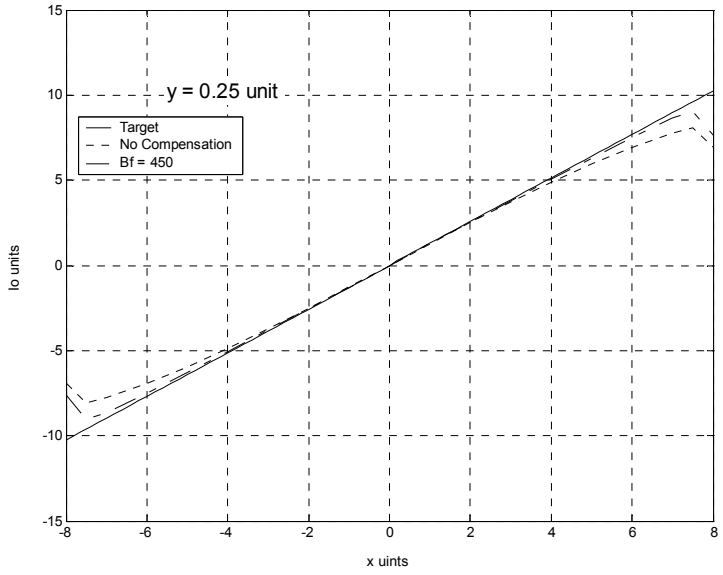



**Figure 3-21** Simulation results of the performance of the exponential amplifier assuming default transistor parameters with $y = 0.25$.

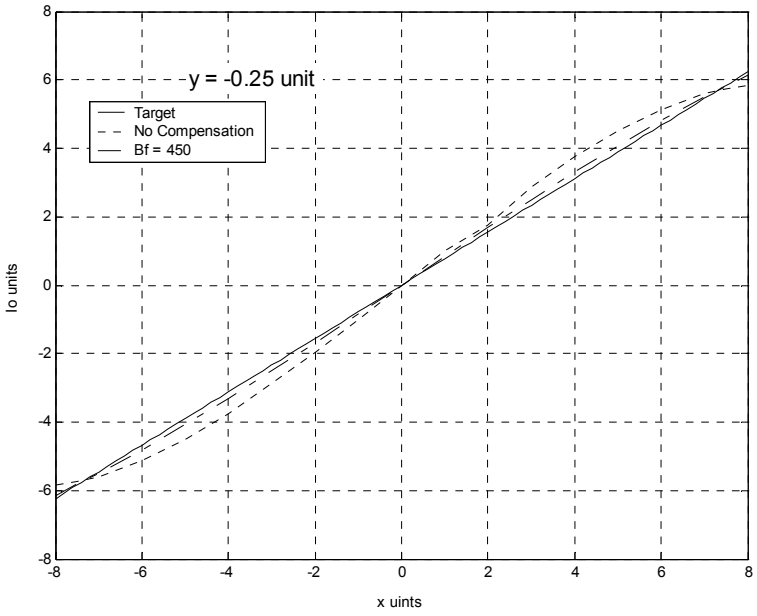



**Figure 3-22** Simulation results of the performance of the exponential amplifier assuming default transistor parameters with $y$ = -0.25.

In order to test the performance of the proposed circuit under semi-practical conditions, practical BJT transistor parameters were considered. These parameters are the same as the previous ones used in simulations of the integrator circuit (i. e. BJT BFP640 Infineon$^{@}$ with $\beta$ = 450). One main possible source of error when using such parameters is the effect of the internal resistances imposed in the transistor itself, especially those of transistors $Q_A$, $Q_B$, and $Q_C$. If it happens that these resistors have comparable values to the value of $R$, then a large error is expected. In order to reduce such error, the value of $R$ can no longer be taken as 26 ohms. Instead, the value is taken to be 260 ohms. This suggests that in order for the exponent argument to be in units, the input current $I_{in}$ should be in $10^{-4}$A rather than $10^{-3}$A. However, decreasing the value of $I_{in}$ by a factor of 10 means that the effect of the base currents of these transistors ($Q_A$, $Q_B$, and $Q_C$) will be significant. In order to minimize this effect, all current sources must be scaled down by the same factor. This implies that the range of $x$ is going to be reduced (due to reduction in the values of $I_{x1}$ and $I_{y1}$). Fortunately, this is not necessarily true simply because the ratio between the current sources $I_A$ and $I_R$ can be adjusted to give a multiplication factor other than one to increase the range of $x$. Thus $x$ becomes

$$x_{new} = \frac{I_A}{I_R} x \tag{3-59}$$

Figures (3-23) to (3-27) show the simulation results of using such transistor parameters compared to the target results. These Figures also show that using the same previous compensation method, the results enhanced.

Obviously, the constant $A$ in equation (3-54) is temperature dependent through $V_T$. Unfortunately, the temperature compensation method used in the previous sections can not be used here because there is no DC current multiplied (or divided) by $V_T$. The only possible temperature compensation method that can be used is to have the resistor $R$ as a temperature dependent resistance. However, due the very limited dynamic range of such resistances, the use of them will degrade the overall performance of the cell seriously [107].

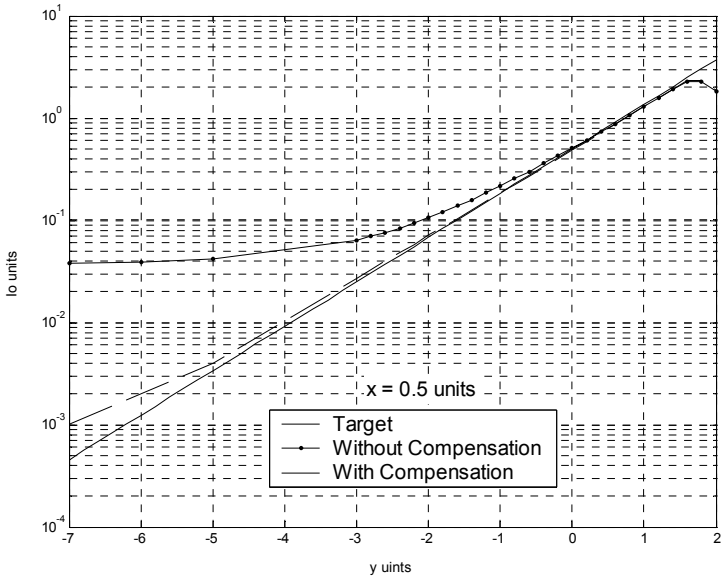



**Figure 3-23** Simulation results of the performance of the exponential amplifier assuming practical transistor parameters with $x$ = 0.5 units.

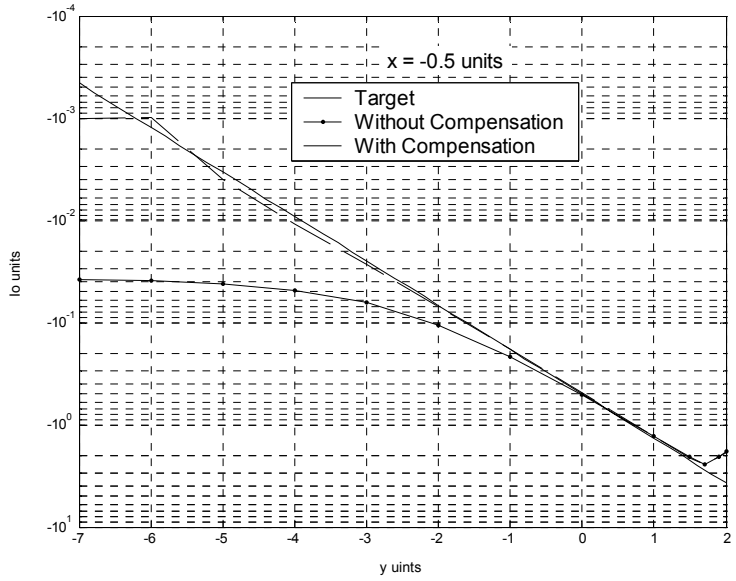



**Figure 3-24** Simulation results of the performance of the exponential amplifier assuming practical transistor parameters with $x$ = -0.5 units.

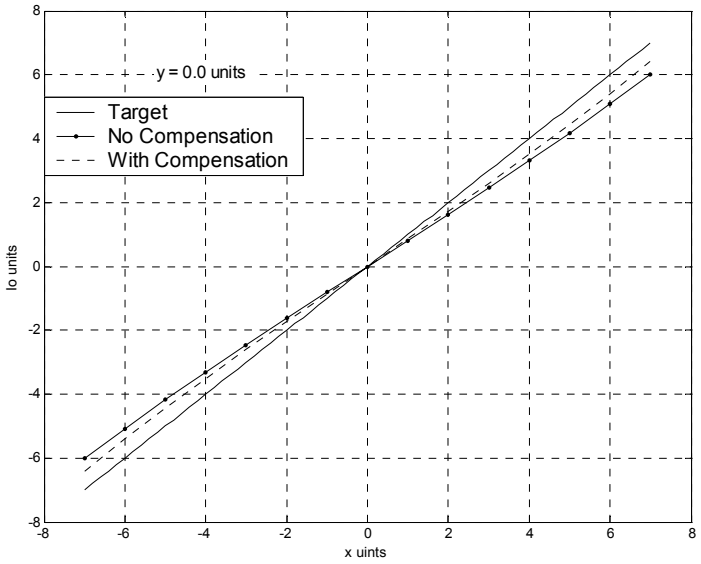



**Figure 3-25** Simulation results of the performance of the exponential amplifier assuming practical transistor parameters with $y = 0$.

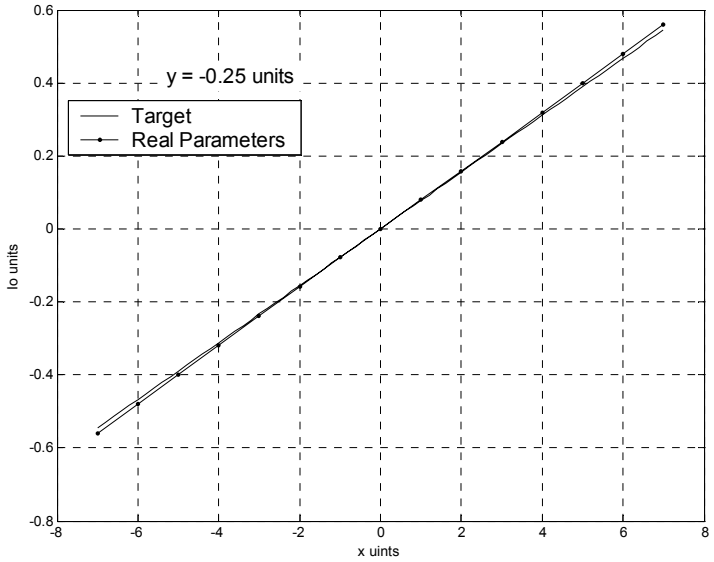



**Figure 3-26** Simulation results of the performance of the exponential amplifier assuming practical transistor parameters with $y = -0.25$.

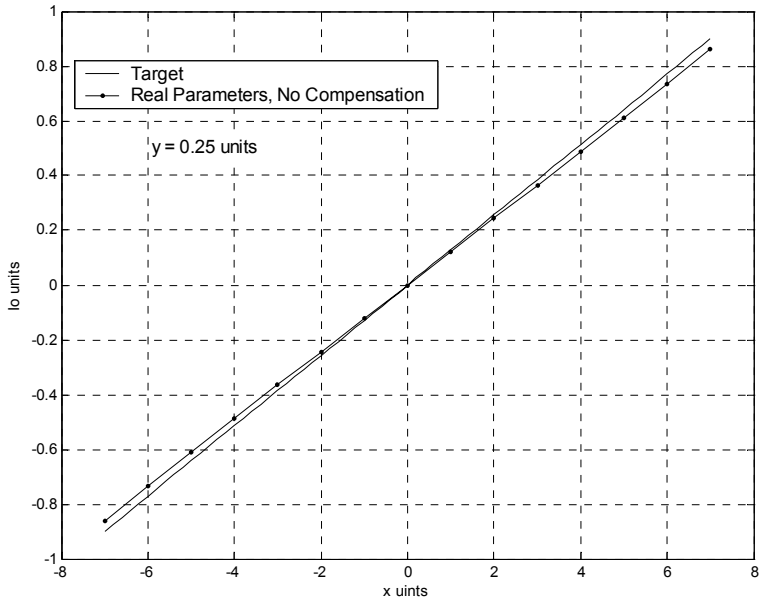



**Figure 3-27** Simulation results of the performance of the exponential amplifier assuming practical transistor parameters with $y = 0.25$.

## 3.3 Log-Function Circuit

The functional relation of the logarithmic cell can be represented as

$$g(x) = A \cdot \ln(x) + B \tag{3-60}$$

where A, and B are constants. As input *x* can be less than or greater than unity, the output *g(x)* is a bidirectional quantity. In order for this implementation to be suitable for integration, the output current is the difference between two other currents.

### 3.3.1 Circuit Description

Exploiting the inherent advantages of the TLP, that is converting an injected current into a base-to-emitter voltage and visa versa, one can develop an exponential current-mode circuit by adding a resistance to act as a voltage-to-current converter. Bearing this in mind, the circuit shown in Figure (3-28) is developed to function as Log-operator. The currents $I_x$ and $I_y$ are the input currents, and $I_o = I_{o1} - I_{o2}$ is the differential output current. As the base to emitter voltage of transistors $Q_1$, $Q_2$, and $Q_3$ are all the same, it can be assumed with very good accuracy that the collector currents of these transistors are equal. Neglecting the base currents of all transistors, these currents are equal to $I_y$. Also, the collector currents of transistors $Q_4$, $Q_5$, and $Q_6$ are assumed to be equal to $I_x$. Applying KCL at the emitter node of $Q_7$ results in

$$I_{o1} = I_y + I_x + I_R \tag{3-61}$$

Applying KCL at the emitter node of $Q_{10}$ yields

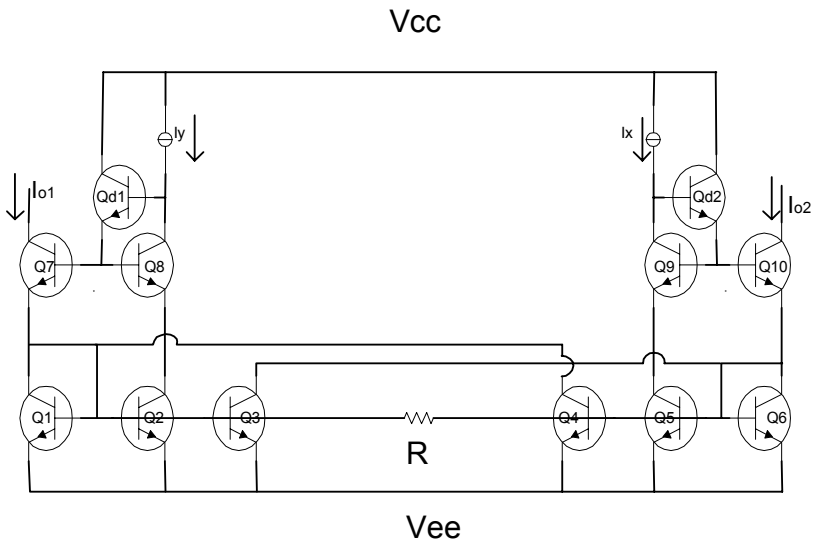



**Figure 3-28** Proposed circuit architecture realizing the natural log-function.

$$I_{o2} = I_y + I_x - I_R \tag{3-62}$$

Now, taking KVL within the loop formed from $Q_3$, the resistor $R$, and $Q_4$, we can write

$$I_R R = V_{BE3} - V_{BE4} \tag{3-63}$$

Assuming all transistors are identical, rewriting equation (3-63) in terms of the collector currents of transistors $Q_3$ and $Q_4$ yields

$$I_R = \frac{V_T}{R} \ln \frac{I_y}{I_x} \tag{3-64}$$

Subtracting equation (3-62) from equation (3-61) and substituting for $I_R$ by equation (3-64) yields

$$I_o = I_{o1} - I_{o2} = 2\frac{V_T}{R} \ln \frac{I_y}{I_x} \tag{3-65}$$

Equation (3-65) gives a direct implementation for the required function. The input $x$ here is represented as a ratio between two currents $I_y/I_x$. Taking for example $I_x$ as a reference value of one unit (e.g. 1$m$A), then taking $I_y$ as $xI_x$ will result in $I_y/I_x$ as $x$ units. In order for the output current to be expressed in units, the value of the resistance $R$ should be chosen such that the constant $V_T/R$ equals to one unit.

It is obvious from equation (3-65) that the output current is temperature dependent through the thermal voltage, $V_T = KT/q$. However, in many applications, each of such cells will be used followed or preceded by an exponential cell. Thus, and as the output of the exponential cell is also temperature dependent, the total output will be temperature independent.

As the multiplicative constant $A$ in equation (3-60) is implemented via $V_T/R$ which is untunable, this cell can be followed by a pass cell to give the required gain if needed. This will also provide a mean to switch OFF the output of this circuit once the FPAA building block is required to implement as a function other than the Log-function.

### 3.3.2 Simulation Results and Discussion

The performance of the logarithmic cell is simulated and presented in Figure (3-29). Simulations with both default Pspice BJT parameters (with $\beta$ =100) and with actual parameters with $\beta$ = 450 are presented. It can be seen from this graph that the circuit performs well even with $\beta$ = 100. In this simulation, $I_x$ was taken to be a constant reference current of 0.5 $m$A. The current $I_y$ is taken to represent the input argument $x$ multiplied by the reference current. It can be seen that this circuit performs will even with relatively small $\beta$ (100) without the need of any compensation technique on a relatively wide range of $x$. However, the range for $x < 1$ is a little bit small. This is because as $x$ becomes less than one, the current flowing through the resistance $R$ reverses its direction ($I_R$ becomes negative), and as the current $I_{o1}$ must be all the time positive, the following inequality must be satisfied (equation (3-61)),

$$I_{o1} = I_y + I_x + I_R > 0 \tag{3-66}$$

Substituting for $I_R$ by equation (3-64) yields

$$I_y + I_x > \frac{-V_T}{R} \ln \frac{I_y}{I_x} \tag{3-67}$$

Now taking $I_y$ as

$$I_y = xI_x \tag{3-68}$$

yields

$$x > \frac{-V_T}{I_x R}\ln(x) - 1 \tag{3-69}$$

Now substituting for $V_T$ as 0.026v and $R$ as 26 ohms, the same value used in previous simulation, results in

$$x > -\frac{10^{-3}}{I_x}\ln(x) - 1 \tag{3-70}$$

This suggests that the range of minimum $x$ depends on the value of the chosen reference current $I_x$. To investigate this more, Figure (3-30) represents the graphical solution for the inequality (3-70) for different values of $I_x$. From this Figure it can be seen that as $I_x$ increases, the minimum possible value of the argument $x$ decreases. To investigate this effect further, the performance of the circuit is simulated for different values of $I_x$ and is shown in Figure (3-31). In this simulation, the practical parameters for the BJT transistors are considered. It is very clear from these simulation results that the range of $x$ lower than one is increased.

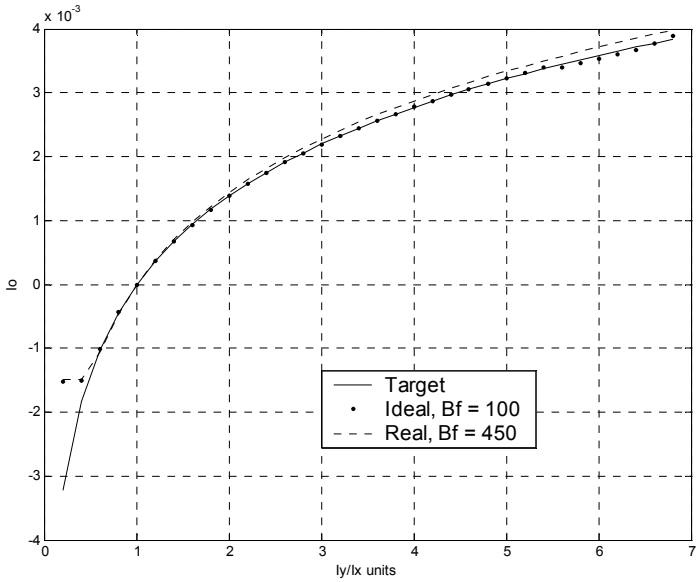



**Figure 3-29** Simulation performance of the logarithmic cell compared to target.

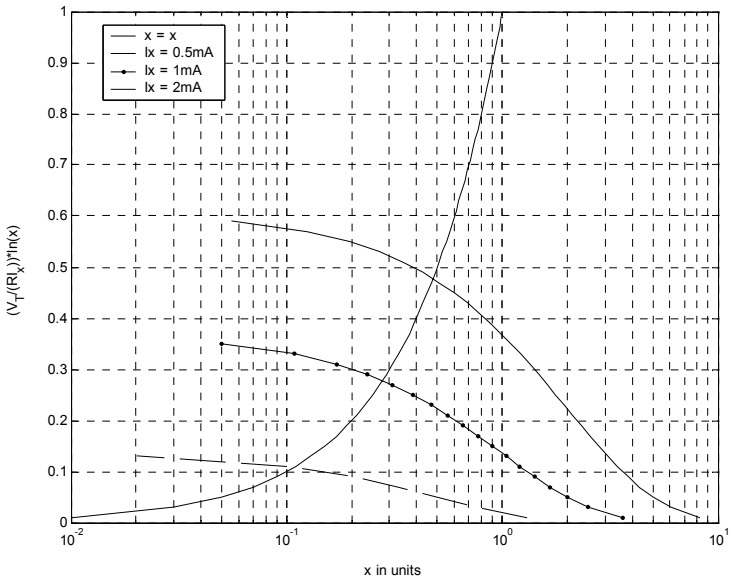



**Figure 3-30** Graphical solution of the inequality (3-70) to assign the limits of the usable range of the input argument *x*.

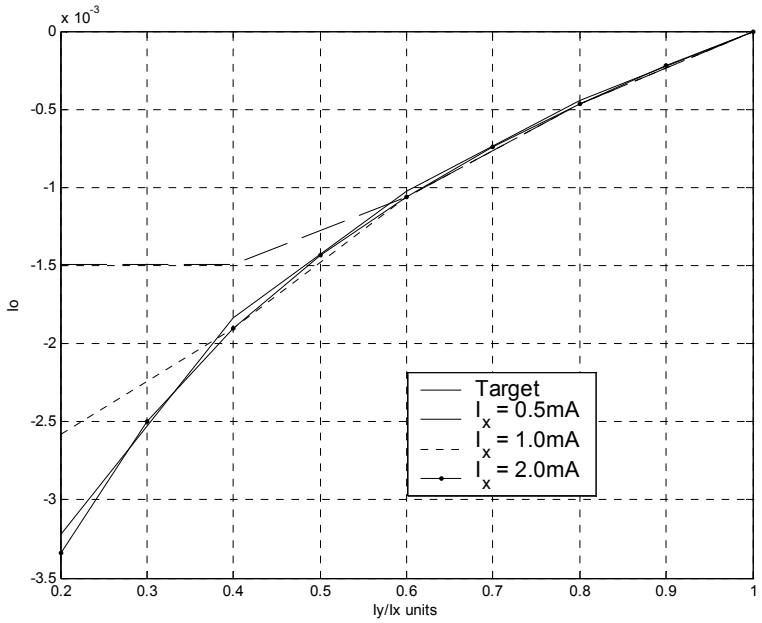



**Figure 3-31** Simulations of the circuit performance for different compensation currents.

Applying the same previous argument on $I_{o2}$ given in equation (3-62) results in the upper limit on the input $x$

$$x > \frac{V_T}{I_x R}\ln(x) - 1 \tag{3-71}$$

Substituting for $V_T$ and $R$ with the same previous values ($V_T$ = 0.026 v, and $R$ = 26 ohm), yield

$$x > \frac{10^{-3}}{I_x}\ln(x) - 1 \tag{3-72}$$

The graphical solution for this inequality is presented in Figure (3-32). From this figure it can be seen that the inequality of equation (3-72) is satisfied for all range of $x$. Thus the only limitation on the upper limit of the value of $x$ is the voltage drop across the load due to the output current.

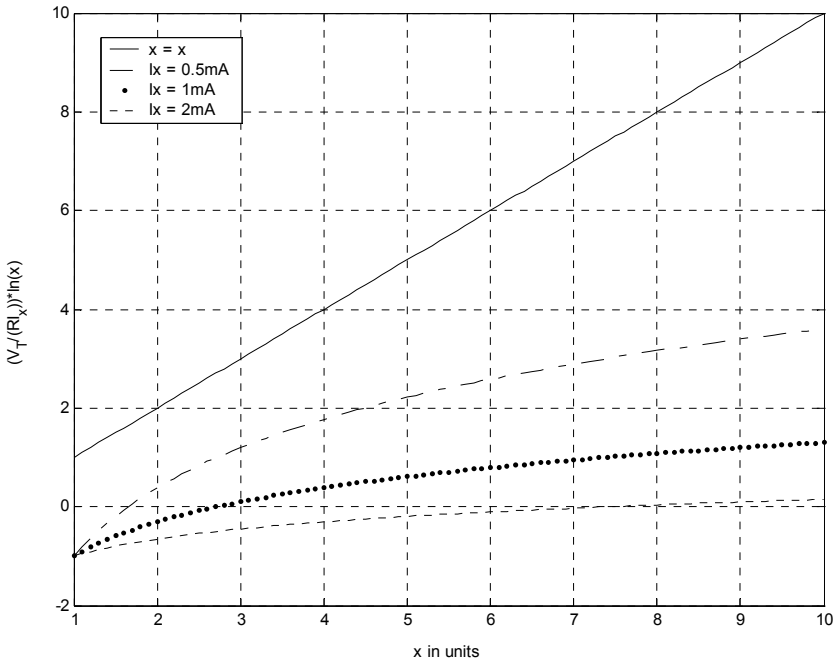



**Figure 3-32** Graphical solution of the inequality (3-73) to assign the limits of the usable range of the input argument *x*

## 3.4 Supplementary Circuits

Configuration and programmability of the proposed CAB is carried out by programmable current sources. The current sources responsible for configuring the function of the CAB are labeled as $I_E$ in all previous circuits. These current sources are either ON with a value of $1mA$ or OFF. One possible realization of such current source is shown in Figure (3-33). In this realization, the value of $I_E$ depends on the voltage difference between the gate and source voltages of the transistor M1. The gate of this transistor is connected to the output of a D-latch while the source is connected to a reference voltage adjusted to assure that the value of $I_E$ to $1mA$. The input of the D-latch is coming from a Decoder controlled by three configuration bits which are part of the control word. The Decoder's output determines the mode of operation of the CAB according to table (3-2). The generated $I_E$ is mirrored by transistors M2-M8 to generate more than one copy of it. In order to generate $I_E/2$, transistors M7 and M8 are assumed to have W/L half that of all other transistors.

In order to achieve programmability of the parameters of the previous circuits, two programmable current sources, one for $I_A$ and one for $I_X$, are assumed. Each of these current sources is realized using two circuits as the one shown in Figure (3-34) one for coarse tuning and the other for fine tuning. In this current source, the W/L of all transistors are assumed to be the same and all transistors to work in the saturation region. This current source is divided into seven units each is responsible of

generating a current component proportional to the number of parallel MOSFETs forming it. The gates of all parallel-transistors units are connected to nodes D0-D6 which represent the outputs of D-latches. The outputs of these D-latches are controlled by data bits forming the other part of the control word. The sources of the transistors are connected to a reference voltage which is adjusted to make $I_0 = 1\mu$A for the fine tuning part and $I_0 = 0.1m$A for the coarse tuning part. Noting that

$$I_6 = 64I_0 = 32I_1 = 16I_2 = 8I_3 = 4I_4 = 2I_5$$

we can write

$$I_t = \begin{cases} 10^{-6}\sum_{i=0}^{6} D_i(i+1) & , \quad \text{fine tuning} \\ 10^{-4}\sum_{i=0}^{6} D_i(i+1) & , \quad \text{coarse tuning} \end{cases} \tag{3-73}$$

where $D_i$ is either logic zero or logic one. According to this configuration, the fine tuning part of this current source can provide any current between $1\mu$A and $127\mu$A with a precision of $1\mu$A. Similarly, the coarse tuning part can provide any current between $0.1m$A and $12.7m$A with a precision of $0.1m$A. This results in a total programmable output current ranging from $1\mu$A up to $12.827m$A.

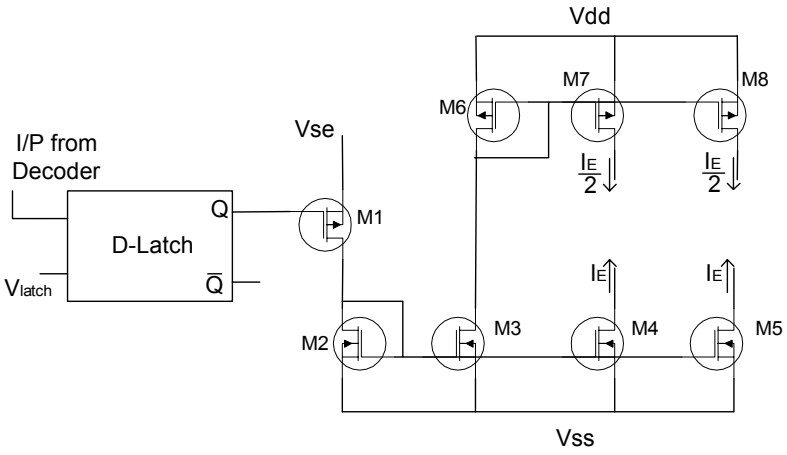



**Figure 3-33** Realization of the current source $I_E$.

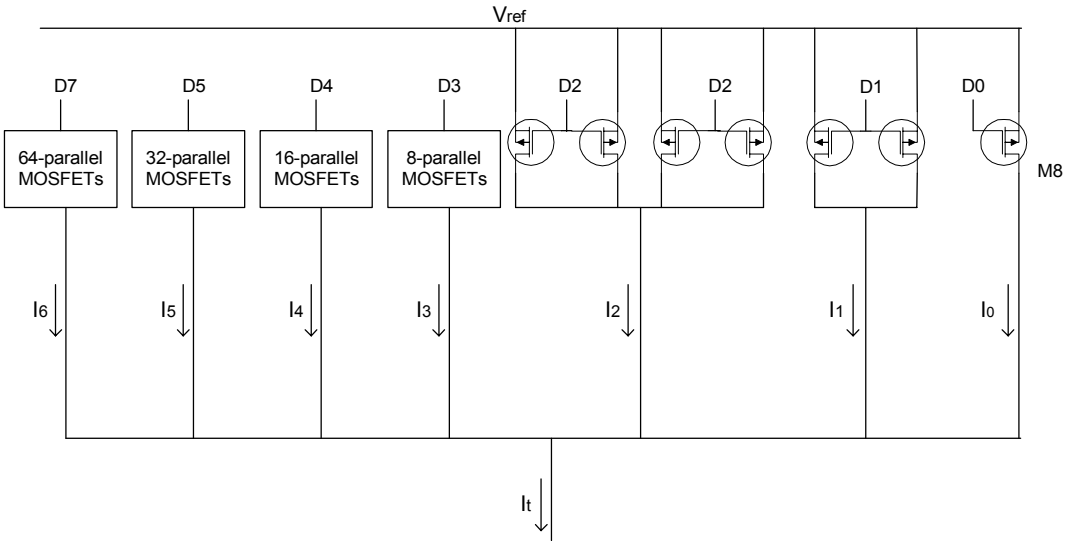



**Figure 3-34** Realization of one part of the programmable current sources $I_A$ and $I_X$.

**Table 3-2** Truth table of the Decoder showing the related functional mode of a CAB.

| $b_2$ | $b_1$ | $b_0$ | f | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | $f_0$ | Not used |
| 0 | 0 | 1 | $f_1$ | $Y(s) = \frac{a}{s+b} X(s)$ |
| 0 | 1 | 0 | $f_2$ | $Y(s) = a \cdot s \cdot X(s)$ |
| 0 | 1 | 1 | $f_3$ | $y = a \cdot \exp(x)$ |
| 1 | 0 | 0 | $f_4$ | $y = a \cdot \ln(x)$ |
| 1 | 0 | 1 | $f_5$ | $y = a \cdot x$ |
| 1 | 1 | 0 | $f_6$ | Not used |
| 1 | 1 | 1 | $F_7$ | Not used |

Figure (3-35) shows the complete block diagram of the supplementary circuitry connected to the CAB. The configuration bits and the programming bits are generated via CAD tool that works as an interface between the user and the FPAA. The biasing currents $I_B$ and $I_C$ are assumed to have fixed values. In order to form a complete FPAA, more than one such unit are connected together via a routing network. Commercial FPAAs such as the Anadigm and TRAC use 20 units.

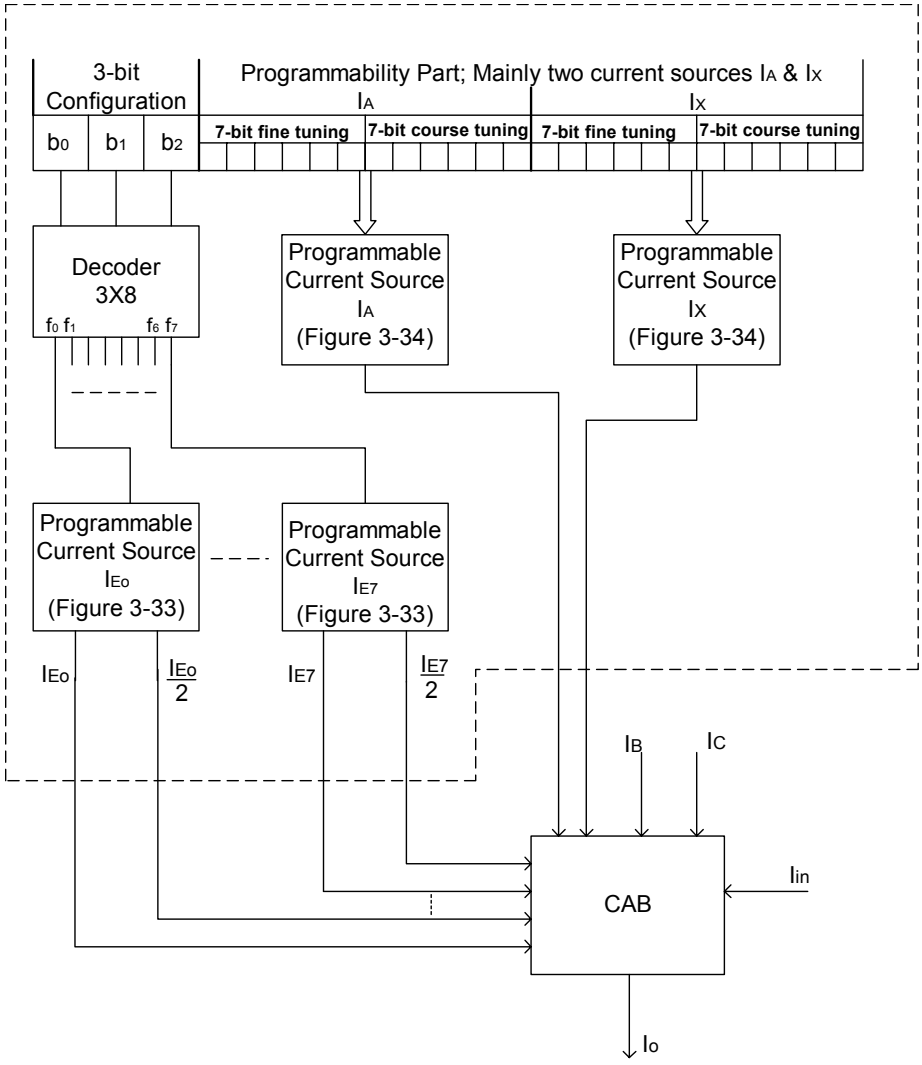



**Figure 3-35** Block diagram showing all supplementary circuitry connected to a CAB.

## 3.5 Summary

In this chapter, five current-mode translinear-based analog circuits were presented to implement the integral, differential, pass, exponential, and logarithmic functions. The output current of all these implementations is represented in the difference mode. This makes these circuits suitable for mixed VLSI implementation.

As these circuits are translinear-based, all base currents were neglected in the derivations. This can be considered as the main source of error that could affect the performance of the circuits, especially when using BJT's with relatively low DC current gain. Fortunately, the effect of these base currents is minimized via compensation currents. These compensation currents are simply added to the effective values of the other current sources used in each circuit. Although the value of these compensation currents are related to the input current themselves, the variation of the actual needed values of the compensation currents compared to their values when being adjusted assuming the input is zero is very small and can be safely neglected.

As the output current of these circuits is temperature-dependent, temperature compensation is needed. In the case of the integrator and differentiator circuit, this compensation is simply achieved by simply replacing one of the constant current sources with a temperature-dependent current source. Unfortunately, this method can not be applied to the exponential and logarithmic circuits. One method that can be used here is to use a temperature dependent resistor instead of the normal resistance. However, due to the very limited dynamic range of such resistors, the dynamic range

of the circuits will reduce seriously. On the other hand, in many applications, both the log and the exponential circuit are used in cascaded manner. For such applications, the output will be temperature-independent.

# CHAPTER 4

# PROPOSED APPLICATIONS

In this chapter, a set of applications are realized using the CABs proposed in Chapter 3. As a first application, the CABs are configured in two different methods to form a second order universal filter. The realized universal filter is capable of performing lowpass filter (LPF), bandpass filter (BPF), highpass filter (HPF), bandreject filter, and allpass filter (APF). The CABs in both topologies are configured as a lossless integrator, a lossy integrator or a differentiator. As a second application, a power law function generating circuit is realized. This circuit is realized using four cascaded CABs configured as either a log or anti-log operator. The last application realized using these CABs is an AM modulator/demodulator system. This system is built using two stages. The first stage consists of two CABs configured as log operators, and the second stage consists of a single CAB configured as anti-log operator. In order to get the final waveform out of the AM demodulator, the LPF realized as part of the universal filter is used as a final filtering stage. The last section of this chapter

consists of some of other possible areas that these CABs can fined straightforward applications within.

## 4.1 2nd Order Universal Filter

As a first application of the previous building blocks, a programmable biquadratic filter is built to function as a universal filter. Basically there are two possible topologies in which the CABs can be connected to each other to form a universal filter, the string-like topology and the matrix-like topology. In order to investigate the performance of the CABs under each topology, the universal filter is built first using four CABs connected in two string-like rows, presented in section 4.1.1, and in the matrix-like configuration as presented in section 4.1.2.

### 4.1.1 String-Like Universal Filter

Figure (4-1) shows the block diagram of four CABs connected in a two string-like topology. Depending on the values of the biasing currents of each CAB, the overall circuit can be programmed to work as a 2nd order LPF, HPF, BPF, Notch and APF. The standard transfer functions of these filters can be lumped together in one biquadratic form written as

$$\frac{I_o(s)}{I_{in}(s)} = \frac{\alpha_1 s^2 + \beta_1 s + \gamma_1}{s^2 + \beta_2 s + \gamma_2} \tag{4-1}$$

where $\alpha_1$, $\beta_1$, $\beta_2$, $\gamma_1$ and $\gamma_2$ are all programmable constants depending on the biasing currents and $I_o(s)$ and $I_{in}(s)$ are the output and input currents of the circuit respectively.

In order to be able to implement it using string like CABs, connected as shown in Figure (4-1), this transfer function must be factorized into two terms. Each of these terms can then be implemented using one of the strings and the results added to give the needed operation. However, factorizing this transfer function imposes a very strict limit on the values of $\beta_2$ and $\gamma_2$ and thus on the possible values of the $Q$-factor of the implemented filters. This limitation comes from the fact that all currents are of real values and thus the following inequality must be satisfied

$$\sqrt{\beta_2^2 - 4\gamma_2} > 0 \tag{4-2}$$

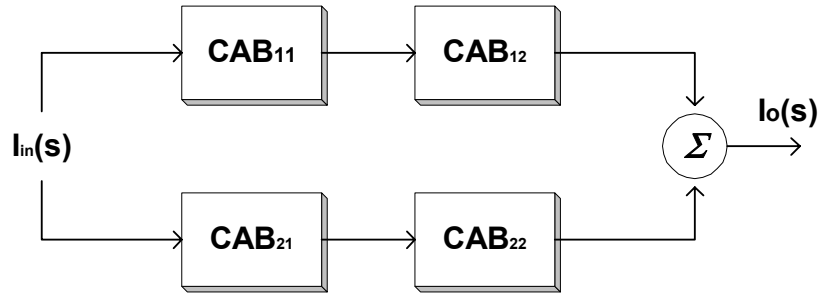
The center frequency and the $Q$-factor are related to $\beta_2$ and $\gamma_2$ as follows

$$w_o = \sqrt{\gamma_2} \tag{4-3}$$

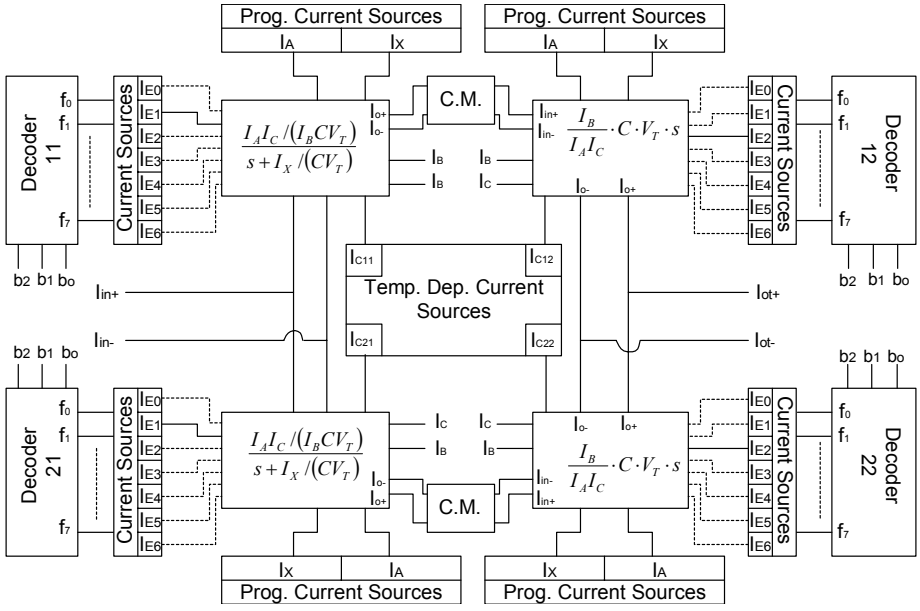
and

$$Q = \frac{\sqrt{\gamma_2}}{\beta_2} \tag{4-4}$$

Substituting equations (4-3) and (4-4) in equation (4-2), it can be seen that the $Q$-factor must be less than 0.5.




(a)




(b)

**Figure 4-1** a) Block diagram of the string-like universal filter, and b) detailed blocks of the CABs when configured as a HPF.

#### 4.1.1.1 Low Pass Filter

Setting both $\alpha_1$ and $\beta_1$ of equation (4-1) to zero results in the following transfer function of a second order LPF

$$\frac{I_o(s)}{I_{in}(s)} = \frac{\gamma_1}{s^2 + \beta_2 s + \gamma_2} \tag{4-5}$$

The -3dB frequency, $w_c$, can be represented as

$$w_c = \frac{1}{2}\sqrt{\beta_2^2 + \gamma_2} - \frac{1}{2}\beta_2 \tag{4-6}$$

Factorizing the denominator of equation (4-5), the LPF transfer function becomes

$$\frac{I_o(s)}{I_{in}(s)} = \frac{a_1}{s + b_1} \cdot \frac{a_2}{s + b_2} \tag{4-7}$$

where $a_1$, $a_2$, $b_1$, and $b_2$ are constants related $\gamma_1$, $\gamma_2$ and $\beta_2$ as follows

$$\gamma_1 = a_1 \cdot a_2 \tag{4-8}$$

$$\gamma_2 = b_1 \cdot b_2 \tag{4-9}$$

$$\beta_2 = b_2 + b_1 \tag{4-10}$$

Depending on the transfer function of equation (4-7), implementing the LPF becomes straightforward. The two CABs in the first string can be configured as two successive lossy integrators and the CABs of the second string in their OFF mode. Comparing the terms of equation (4-7) to the transfer function of the lossy integrator presented previously in section 3.1, equation (3-12), and after some mathematical manipulations, the constants $a_1$, $a_2$, $b_1$ and $b_2$ can be mapped into the biasing currents as follows

$$a = a_1 = a_2 = \frac{I_{A1,2}^2}{CV_T I_{B1,2}} \tag{4-11}$$

$$b_{1,2} = \frac{I_{X1,2}}{CV_T} \tag{4-12}$$

where the indexes 1 and 2 indicate integrator block one and two respectively, and $V_T$ is the thermal voltage.

As an example, the circuit is simulated for a cutoff frequency $f_c$ of 3MHz with $Q$ = 0.47 and a dc gain of 33dB. Figure (4-2) shows the gain- and phase-frequency characteristics of this realized LPF. To examine the effect of transistor parameters on the performance of the filter, the simulations are performed for the cases assuming default parameters with $\beta_f$ = 100, 1000 and assuming real (commercial) transistor parameters used in previous sections. Due to the fact that the DC gain of this filter and all other filters can be easily adjusted to the required value via the biasing currents and by using other gain-stages, it is the simulated cutoff frequency in the case of the LPF and the HPF and the center frequency in the case of the other filters that is important to be compared with the expected. The percentage error in the center frequency of this filter is less than 3% and the phase error is less than $2^o$ within the passband for the case assuming real transistor parameters. When assuming $\beta_f$ = 1000, these figures become even less.

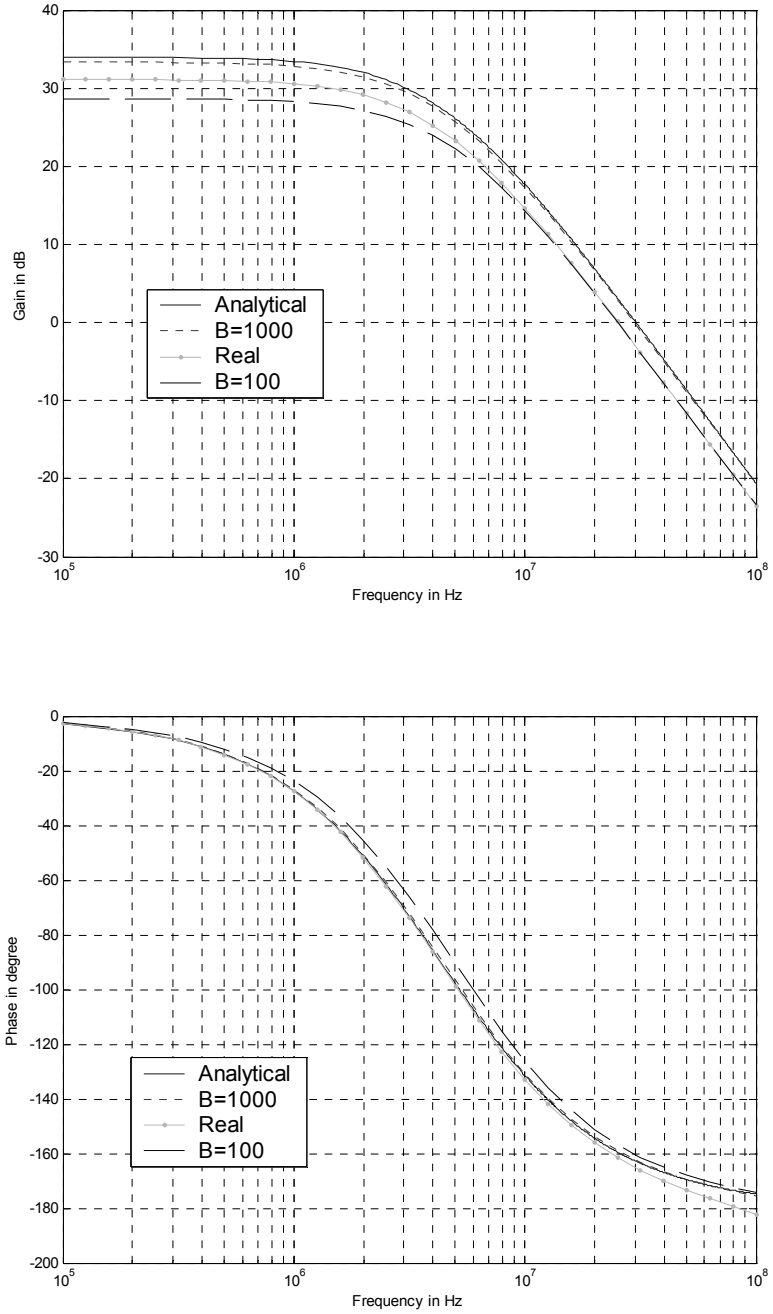



**Figure 4-2** Gain- and Phase-Frequency Characteristic curves of the realized LPF. The following values of the biasing currents are used; $I_{A1,2}$ = 0.1mA, $I_{B1,2}$ = 0.1mA, $I_{X1}$ = 10$\mu$A and $I_{X2}$ = 20uA.

#### 4.1.1.2 Band Pass Filter

As the transfer function of a BPF can be represented as

$$\frac{i_o}{i_{in}} = \frac{\beta_1 s}{s^2 + \beta_2 s + \gamma_2} \tag{4-13}$$

both $\alpha_1$ and $\gamma_1$ of equation (4-1) must be set to zero. This transfer function can be factorized as follows

$$\frac{I_o(s)}{I_{in}(s)} = \frac{a_1}{s + b_1} + \frac{a_2}{s + b_2} \tag{4-14}$$

To realize this transfer function, the first block of each string is configured as an integrator while the other blocks as either an amplifier or a pass blocks. Configuring the blocks in such manner and after some mathematical manipulations, the constants $\beta_1$, $\beta_2$, and $\gamma_2$ can be represented in terms of the constants $a_i$ and $b_i$ as

$$\beta_1 = a_2 + a_1 \tag{4-15}$$

$$\beta_2 = b_1 + b_2 \tag{4-16}$$

$$\gamma_2 = b_1 \cdot b_2 \tag{4-17}$$

$$b_1 = \frac{a_1}{a_2} b_2 \tag{4-18}$$

where the indexes 1 and 2 indicate, once again, integrator block one and two respectively. The constants $a_i$ and $b_i$ are directly mapped into currents exactly the same as in equations (4-11) and (4-12).

As an example, the circuit is simulated for a central frequency $f_o$ of 8.7MHz with $Q$ = 0.47 and a gain of 19dB. Figures (4-3) shows the gain- and phase-frequency

characteristics of the realized BPF. It can be seen from these figures that the central frequency is almost independent on the transistor parameter whereas the gain of the BPF does depend on it. The center frequency of the proposed BPF shows very good matching with the expected value with percentage error of about 2% for the case assuming real transistor parameters. The error in the phase within the bandwidth of the BPF is around $5^{o}$.

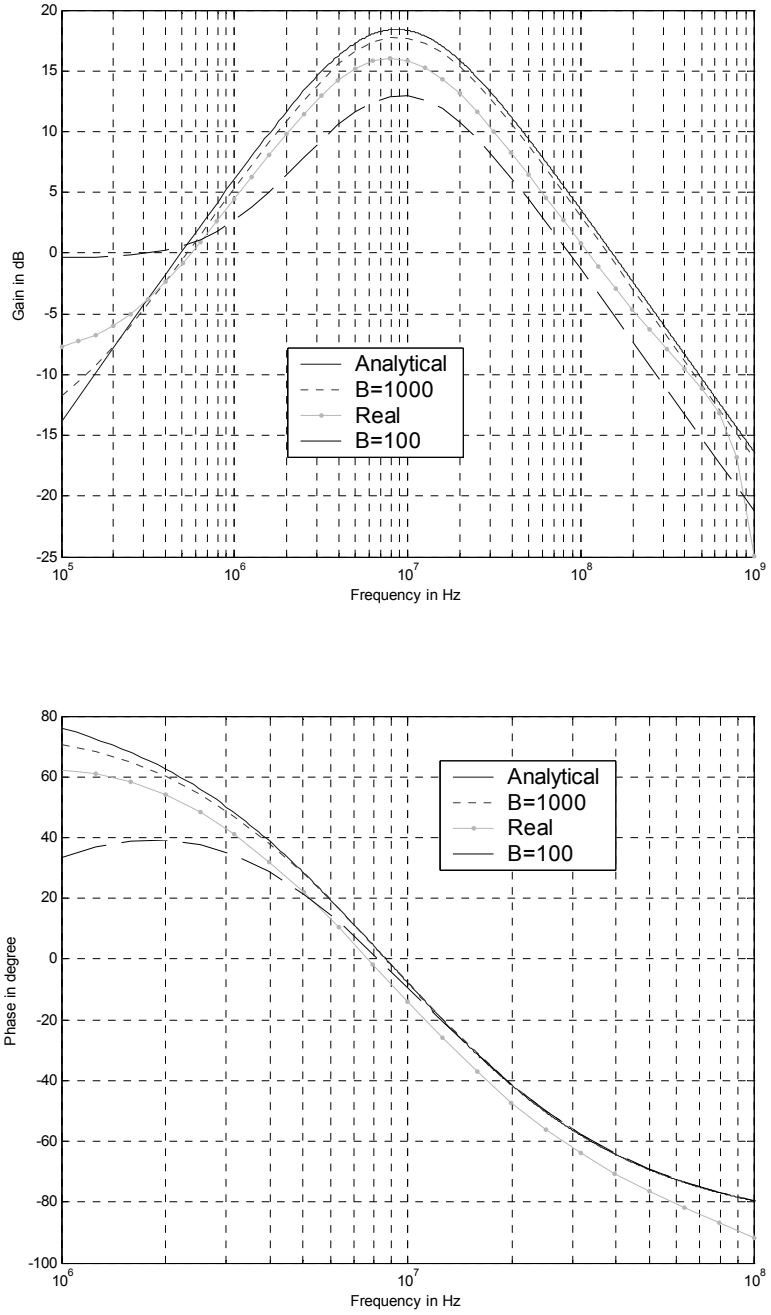



**Figure 4-3** Gain- and Phase-Frequency Characteristic curves of the BPF. The following values of the biasing currents are used; $I_{A1}$ = 0.1mA, $I_{B1}$ = 0.1mA, $I_{X1}$ = 40$\mu$A, $I_{A2}$ = 0.1mA, $I_{B2}$ = 0.2mA and $I_{X2}$ = 20$\mu$A.

#### 4.1.1.3 Notch Filter

The transfer function of a Notch Filter is given as

$$\frac{i_o}{i_{in}} = \frac{s^2 + \gamma_1}{s^2 + \beta_2 s + \gamma_2} \tag{4-19}$$

Utilizing the long division, this transfer function can be rewritten as

$$\frac{i_o}{i_{in}} = 1 - \frac{\beta_2 s + (\gamma_2 - \gamma_1)}{s^2 + \beta_2 s + \gamma_2} \tag{4-20}$$

This new form can be factorized as in equation (4-14) and thus can simply be implemented using the same blocks configuration. The constants $\beta_2$, $\gamma_1$ and $\gamma_2$ are represented in terms of the biasing currents as

$$\beta_2 = b_1 + b_2 = a_1 - a_2 \tag{4-21}$$

$$\gamma_2 = b_1 \cdot b_2 \tag{4-22}$$

$$\gamma_2 - \gamma_1 = a_1 b_2 - a_2 b_1 \tag{4-23}$$

where a1, a2, b1, and b2 are as defined previously in equations (4-11) and (4-12).

As an example, the circuit is simulated for a central frequency $f_o$ of 1.27MHz with $Q$ = 0.3 and a gain of 0dB. Figure (4-4) shows the gain- and phase-frequency characteristics of the realized Notch filter. It can be seen from the simulation results that these parameters depend heavily on the parameters of the transistor used. In order to get more accurate results of this filter, the center frequency must be retuned to the required value by adjusting the biasing currents.

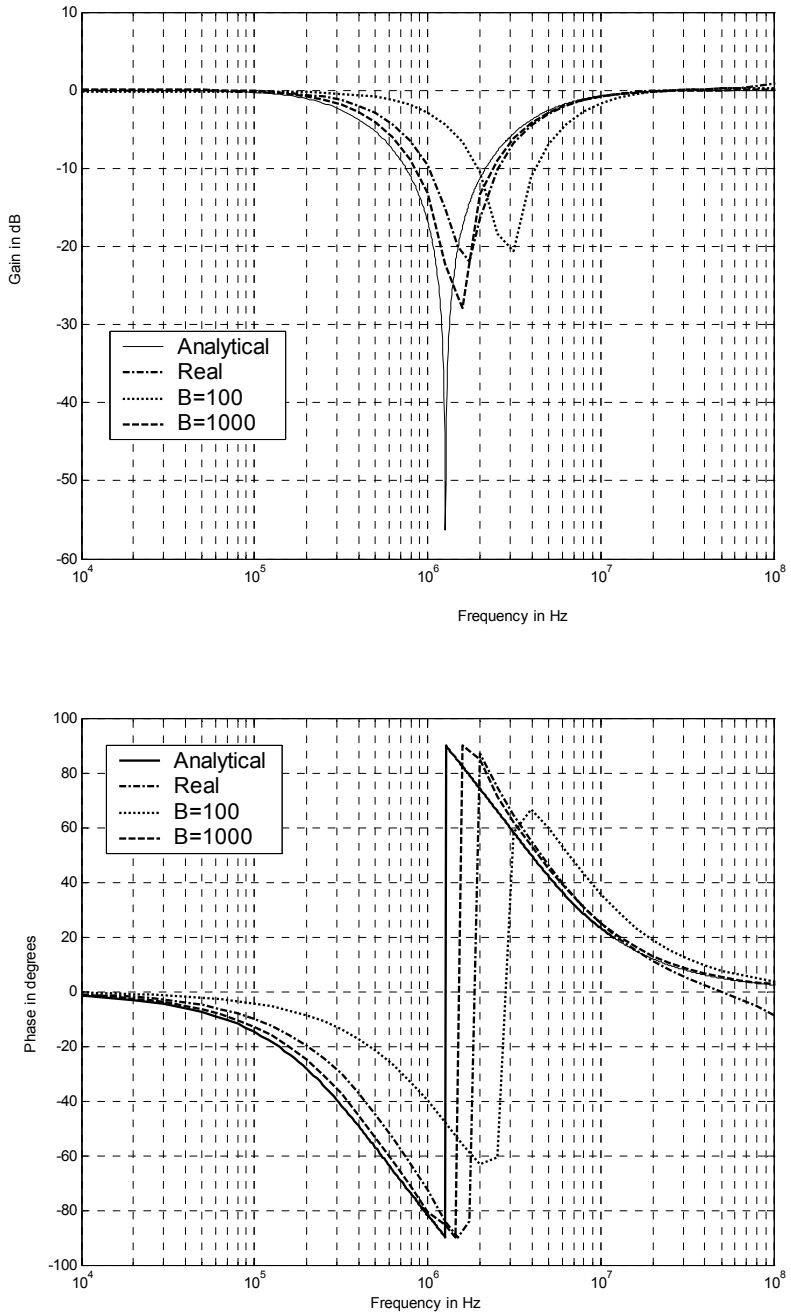



**Figure 4-4** Gain- and Phase-Frequency Characteristic curves of the Notch Filter. The following values of the biasing currents are used; $I_{A1}$ =39.5$\mu$A, $I_{B1}$ = .1mA, $I_{X1}$ = 124.8 20uA, $I_{A2}$ = 13.2$\mu$A, $I_{B2}$ = .1mA and $I_{X2}$ = 1.36$\mu$A.

#### 4.1.1.4 High Pass Filter

The transfer function of a HPF is given as

$$\frac{i_o}{i_{in}} = \frac{s^2}{s^2 + \beta_2 s + \gamma_2} \tag{4-24}$$

where both $\beta_1$ and $\gamma_1$ of equation (4-1) are set to zero. In realizing this transfer function, the first block of each string is configured as an integrator while the other blocks configured as differentiators. Factorizing the transfer function as in equation (4-14) leads to the following relations

$$\alpha_1 = a_2 = \frac{a_1}{2} \tag{4-25}$$

$$\beta_2 = 3\, b_2 \tag{4-26}$$

$$\gamma_2 = 2\, b_2^2 \tag{4-27}$$

$$b_1 = 2\, b_2 \tag{4-28}$$

The constants $a_i$ and $b_i$ are related to the biasing currents as follows

$$a_{1,2} = \frac{I_{A1,2}^2 I_{BD1,2}}{I_{B1,2} I_{AD1,2} I_{CD1,2}} \tag{4-29}$$

$$b_{1,2} = \frac{I_{X1,2}}{CV_T} \tag{4-30}$$

where the index letter *D* in equation (4-29) indicates the biasing currents related to the differentiator blocks.

As an example, the circuit is simulated for a cutoff frequency $f_c$ of 50MHz with $Q$ = 0.47 and a gain of 0dB. Figure (4-5) shows the gain- and phase-frequency

characteristics of the realized HPF. Although the phase response is affected heavily by the transistors parameters used, the gain response of this HPF showing matching with the expected response in terms the center frequency with a percentage error of less than 2% for real parameters.

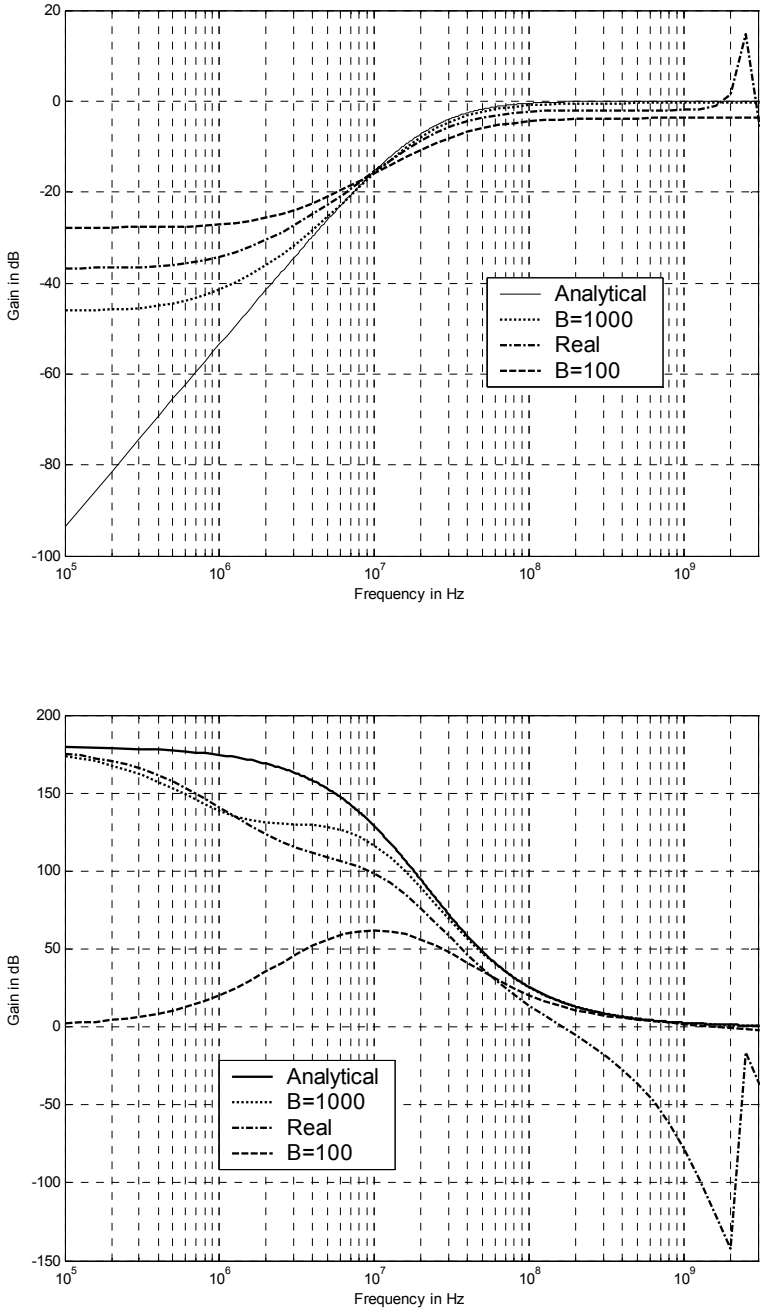



**Figure 4-5** Gain- and Phase-Frequency Characteristic curves of the HPF. The following values are used; $I_{A1} = I_{B1} = 1\text{mA}$, $I_{X1} = 100\text{uA}$, $I_{AD1} = 1\text{mA}$, $I_{BD1} = 2\text{mA}$, $I_{CD1} = I_{A2} = I_{B2} = 1\text{mA}$, $I_{X2} = 50\mu\text{A}$, $I_{AD2} = 1\text{mA}$, $I_{BD2} = 1\text{mA}$ and $I_{CD2} = 1\text{mA}$.

#### 4.1.1.5 AllPass Filter

The transfer function of an APF is given as

$$\frac{I_o}{I_{in}} = \frac{s^2 - \beta s + \gamma}{s^2 + \beta s + \gamma} \tag{4-31}$$

This transfer function can be simplified to a simpler one utilizing the long division which yields,

$$\frac{I_o}{I_{in}} = 1 - \frac{2\beta s}{s^2 + \beta s + \gamma} \tag{4-32}$$

As in the case of the BPF and the notch filter, the first two blocks are configured as integrators while the last ones as pass or amplifier cells. Factorizing equation (4-32) as in equation (4-14) yields

$$\beta = 2 \cdot (b_1 + b_2) = a_1 - a_2 \tag{4-33}$$

and

$$\gamma = b_1 \cdot b_2 \tag{4-34}$$

where $a_1$, $a_2$, $b_1$, and $b_2$ are as defined in equations (4-11) and (4-12).

As an example, the circuit is simulated for a center frequency $f_c$ of 13MHz with $Q$ = 0.43 and a gain of 0dB. Figure (4-6) shows the gain- and phase-frequency characteristics of the realized APF. The gain response of the filter shows expected characteristics up to nearly 50 MHz with a maximum phase error less than $5^o$ and 100 MHz for a maximum phase error of about $20^o$.

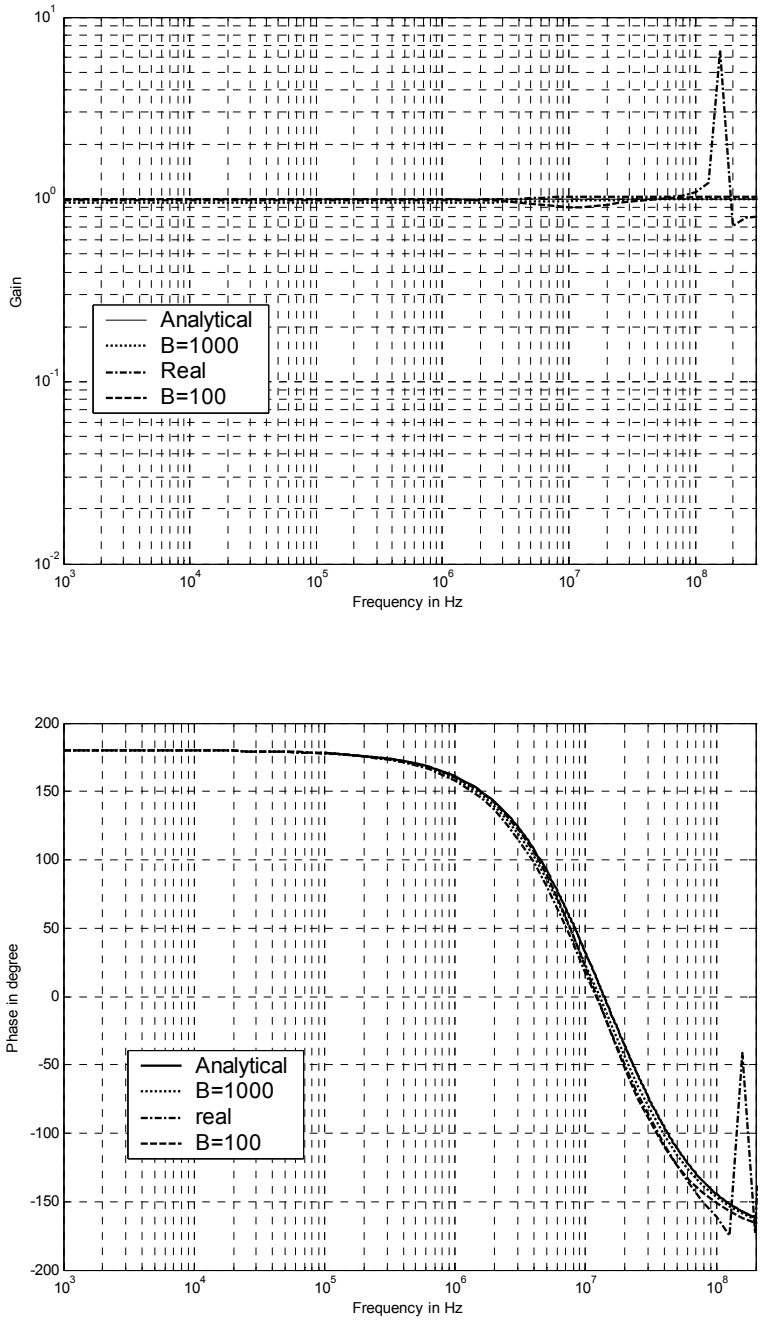



**Figure 4-6** Gain- and Phase-Frequency Characteristic curves of the All Pass Filter. The following values of the biasing currents are used; $I_{A1}$ = 0.1766mA, $I_{B1}$ = 0.1mA, $I_{X1}$ = 73$\mu$A, $I_{A2}$ = 0.096mA, $I_{B2}$ = 0.1mA, and $I_{X2}$ = 24$\mu$A.

#### 4.1.1.6 Filter Programmability

Configuration of the proposed universal filter is carried out by programmable current sources. Assuming that the CABs are going to be built as a part of a mixed system, the programmable current sources are realized using MOSFETs as shown in Figures (3-33) and (3-34). Each current source is assumed to consist of two programmable cells, one for coarse tuning and the other for fine tuning. The value of the output current depends on a controlling binary code word that is generated by a user interface program, designed using Visual Basic. Depending on the filtering function and the specifications of the required filter, i.e. the *Q*-factor, gain, and the cutoff frequency, the user interface program generates the required controlling word. This controlling word is stored in latches that control the gate voltages of the MOSFETs of the programmable current sources and thus giving the required values of the biasing currents needed. Figures (4-7) and (4-8) show examples of the dialog windows of the designed user interface program.

The programmable current sources used in this application use 7-bits for each tuning part, fine and coarse. Of course, increasing the number of bits used will increase the accuracy and the tuning range of these current sources. This has direct influence on the resulting accuracy and tuning range of the overall system.


**Figure 4-7** Example of dialog windows of the designed user interface program showing all possible filtering functions.

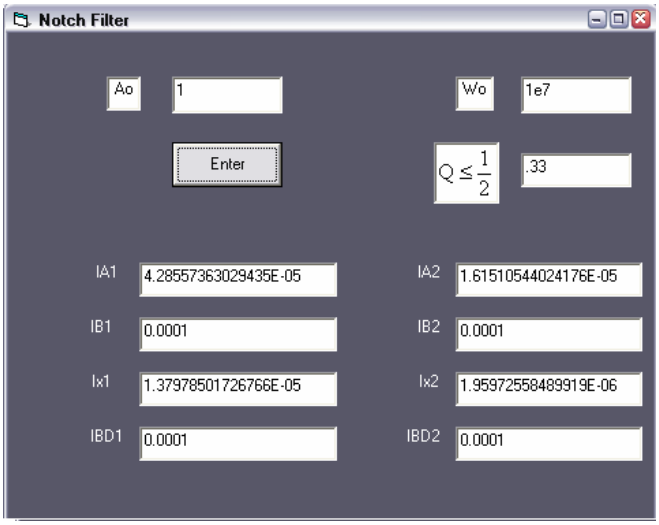



**Figure 4-8** Example of dialog windows of the designed user interface program showing the relative values of the current sources.

### 4.1.2 Matrix-Like Universal Filter

Figure (4-9) shows the block diagram of a matrix-like configured universal filter. In this configuration only two CABs are used and configured as integrators. Simple current mirrors and summing nodes are used to act as the summer blocks. As all filtering functions are achieved simultaneously, simple selecting switches are used to obtain the required filtering operation.

One realization of such biquadratic filter based on current mode techniques was proposed in [108]. In that work, the biquadratic filter was implemented using two basic single input single output integrator cells with relatively large values of capacitors, 2$\mu$F and 1nF. This limits the bandwidth of the filters and makes the implementation unsuitable for fully integrated systems.

Using the CAB developed earlier instead of the integrators used in [108] permits the implementation of a fully differential biquadratic filters suitable for integration mainly for high frequency applications.

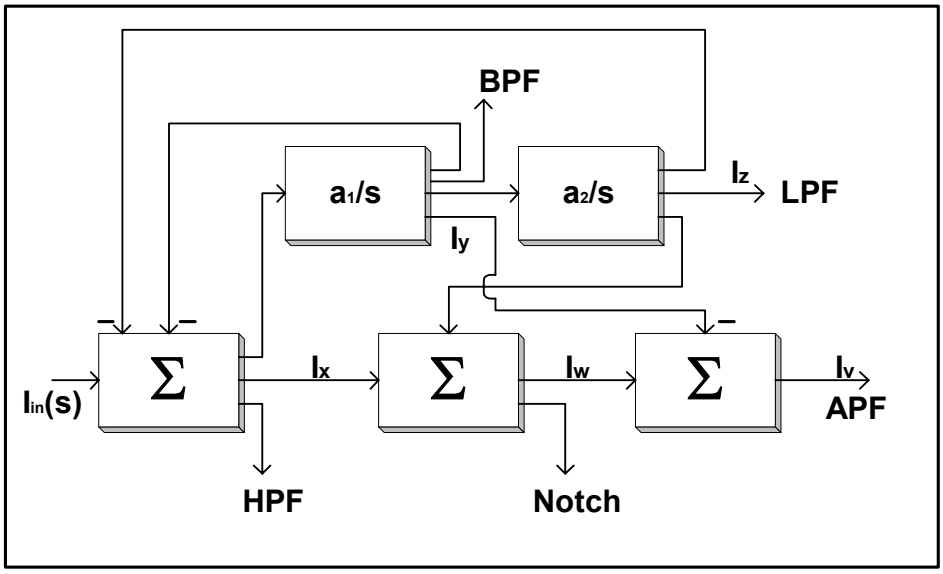



**Figure 4-9** Block diagram of a 2nd order biquadratic universal filter [108].

From Figure (4-9) we have,

$$I_x = I_{in} - I_y - I_z \tag{4-35}$$

$$I_y = \frac{a_1}{s} I_x \tag{4-36}$$

$$I_z = \frac{a_2}{s} I_y = \frac{a_1 a_2}{s^2} I_x \tag{4-37}$$

Substituting equations (4-36) and (4-37) in equation (4-35), we get

$$I_x = I_{in} - \frac{a_1}{s} I_y - \frac{a_1 a_2}{s^2} I_z \tag{4-38}$$

Rearranging equation (4-38), we get

$$\frac{I_x}{I_{in}} = \frac{s^2}{s^2 + a_1 s + a_1 a_2} \tag{4-39}$$

which represent a HPF characteristics. Substituting equation (4-39) in equation (4-36) for $I_x$ results in

$$\frac{I_y}{I_{in}} = \frac{a_1 s}{s^2 + a_1 s + a_1 a_2} \tag{4-40}$$

Thus $I_y$ represents a BPF function. Substituting equation (4-40) in equation (4-37) results in

$$\frac{I_z}{I_{in}} = \frac{a_1 a_2}{s^2 + a_1 s + a_1 a_2} \tag{4-41}$$

which represents a LPF function.

The current $I_w$ is the sum of $I_x$ and $I_z$ and thus can be written as

$$\frac{I_w}{I_{in}} = \frac{I_x + I_z}{I_{in}} = \frac{s^2 + a_1 a_2}{s^2 + a_1 s + a_1 a_2} \tag{4-42}$$

which represents notch filtering characteristics. Similarly, the current $I_v$ is the difference between $I_w$ and $I_y$ and can be written as

$$\frac{I_v}{I_{in}} = \frac{I_w - I_y}{I_{in}} = \frac{s^2 - a_1 s + a_1 a_2}{s^2 + a_1 s + a_1 a_2} \tag{4-43}$$

We note here that the denominators of all filtering characteristics are the same. The center frequency of these filters is $w_o = \sqrt{a_1 a_2}$ and the $Q$-factor is $Q = \sqrt{\frac{a_2}{a_1}}$. The constants $a_1$ and $a_2$ are related to the biasing currents as follows;

$$a_{1,2} = \frac{I_{A1,2}^2}{C V_T I_{B1,2}} \tag{4-44}$$

Thus these constants can be tuned independently by programming the biasing currents $I_{A1,2}$ and $I_{B1,2}$.

#### 4.1.2.1 Low Pass Filter

Figures (4-10) and (4-11) show the simulation results for the gain- and phase-frequency characteristics for different $Q$-factor values with a center frequency $w_c$ of 1MHz. In Figure (4-10), simulations done assuming default transistor parameters with $\beta$ = 450 while in Figure (4-11), the transistors are assumed practical parameters. Figures (4-12) and (4-13) show the programmability of the cutoff frequency $w_o$ while maintaining $Q$ = 5.

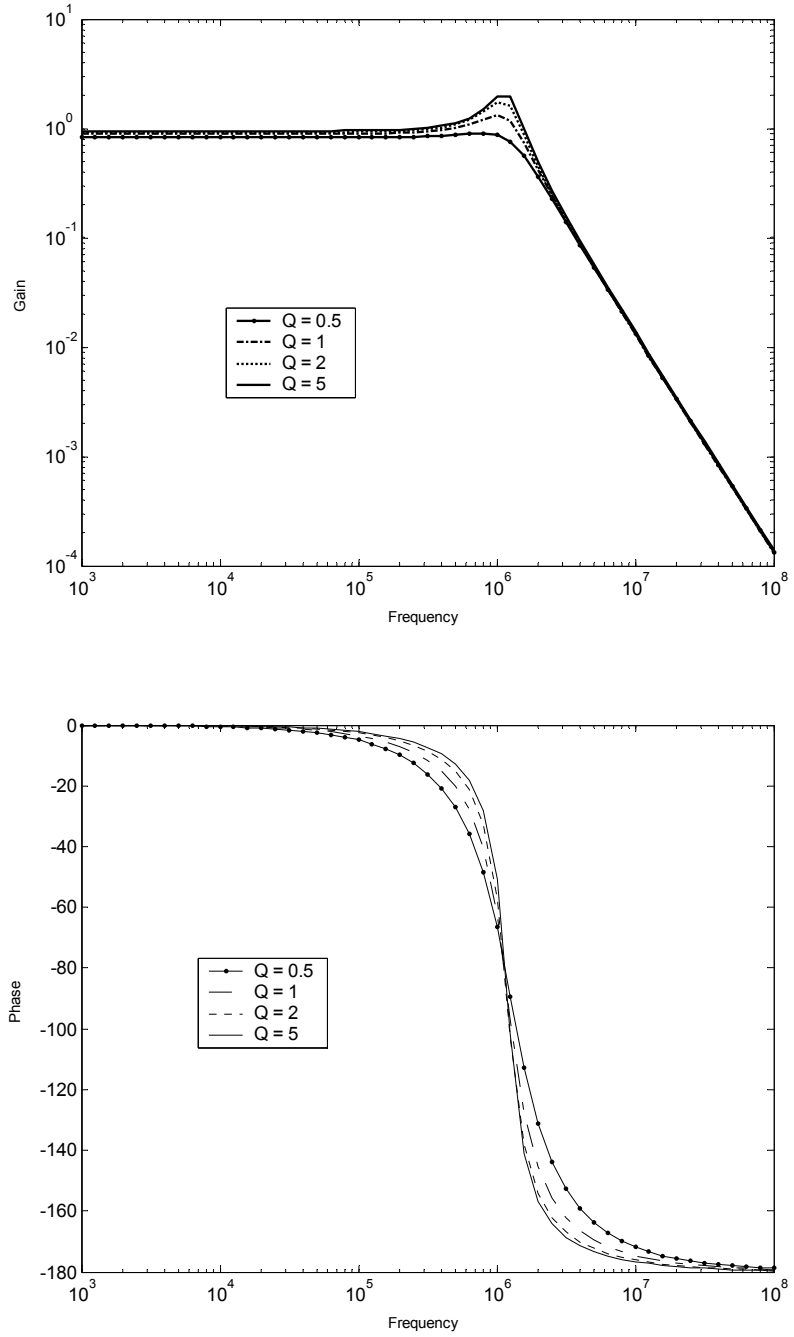



**Figure 4-10** Gain and Phase response of the LPF with default parameters with $\beta$ = 450. Tuning $Q$ is achieved by via $I_A$ while keeping the values of $I_{B1,2}$ = 1mA.

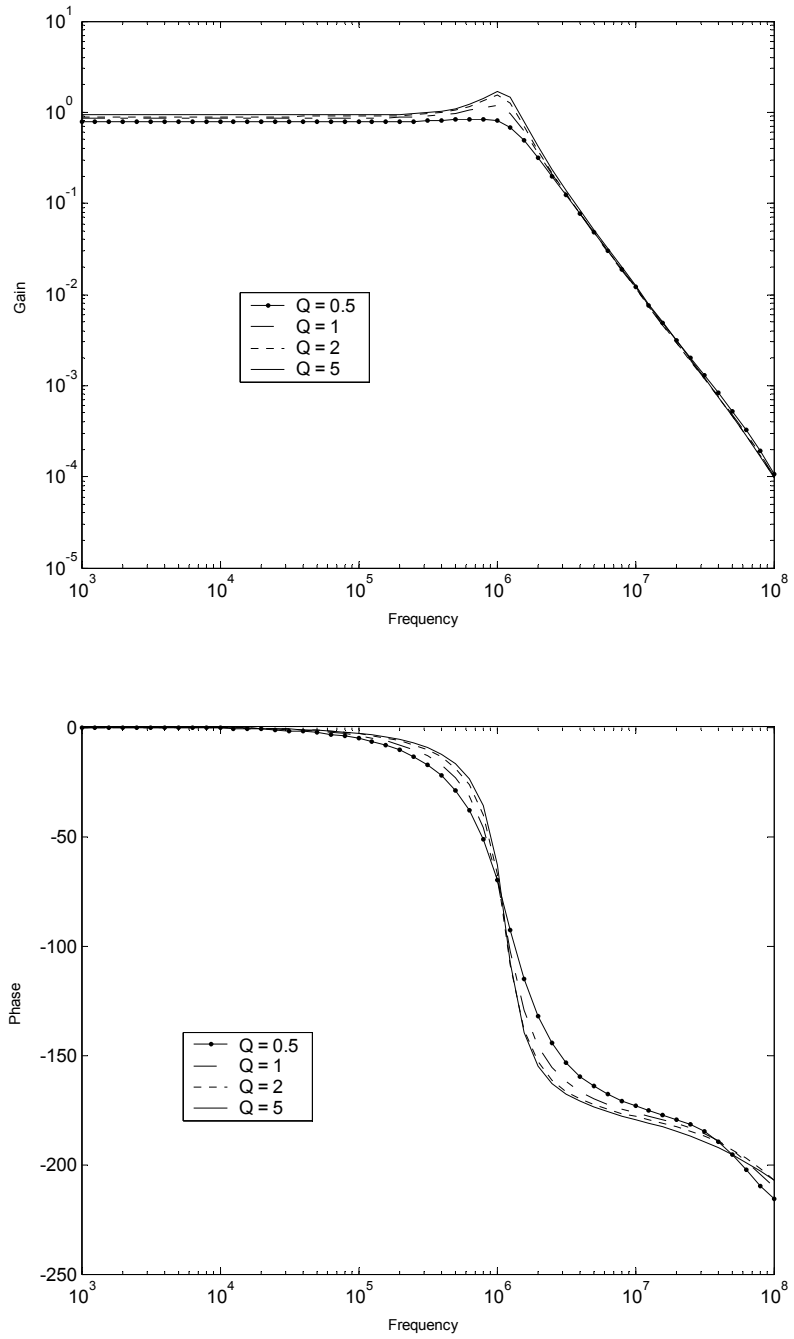



**Figure 4-11** Gain- and Phase-Frequency response of the LPF assuming actual transistor parameters.

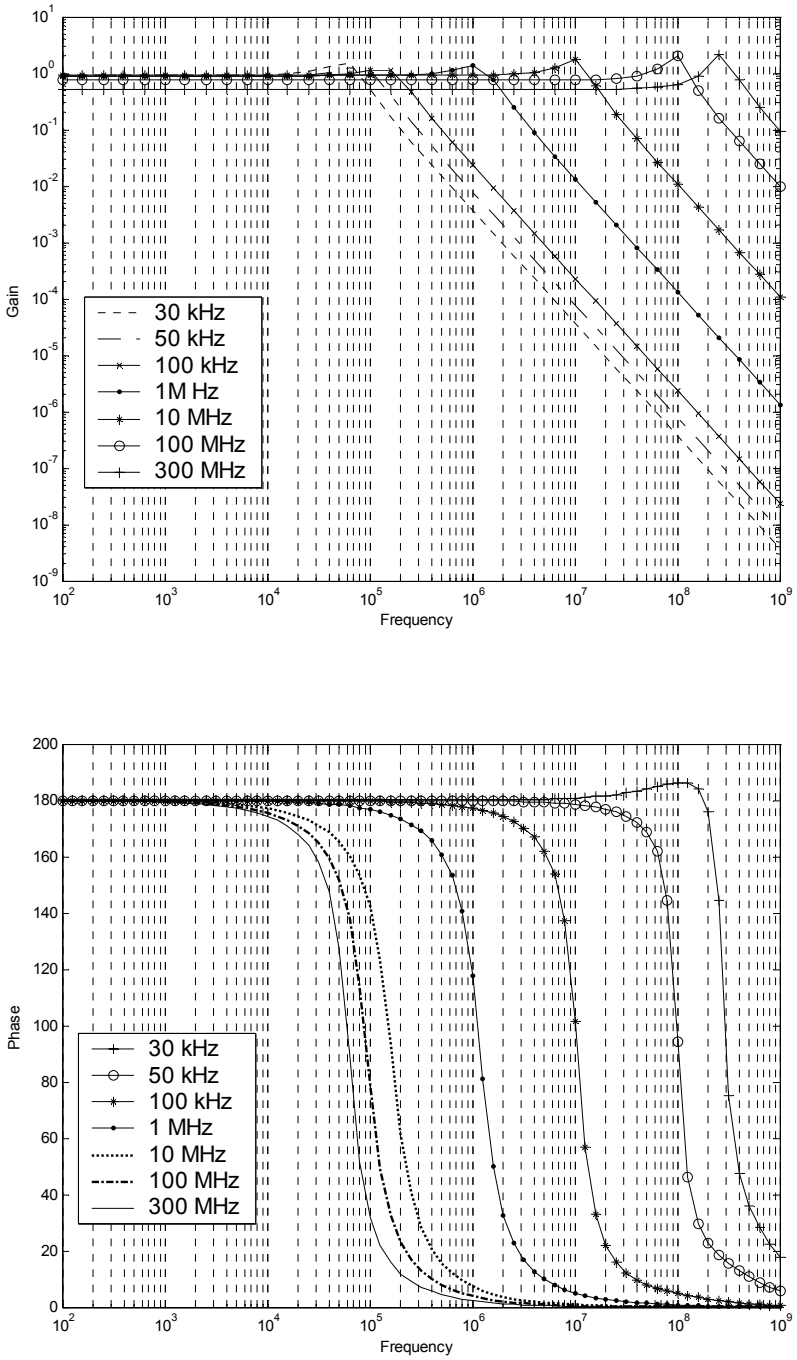



**Figure 4-12** Gain and Phase responses of the LPF with default parameters with $\beta$ = 450. Tuning the center frequency $f_o$ is achieved via $I_A$ and $I_{B1,2}$ = 1mA. $Q$ =5.

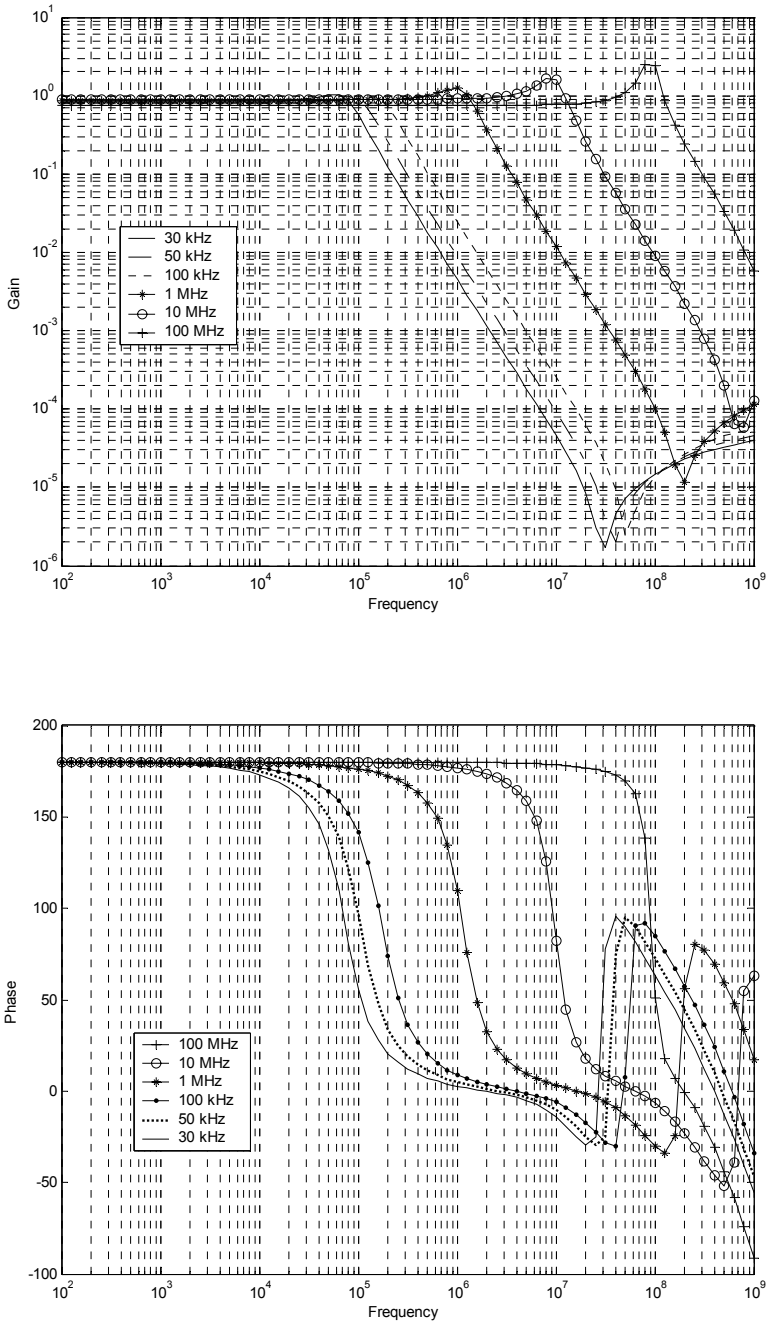



**Figure 4-13** Gain- and Phase-Frequency response of the LPF assuming practical transistor parameters. Tuning center frequency is achieved as in Figure (4-12) under the same biasing current values.

#### 4.1.2.2 Band Pass Filter

Simulation results of the BPF are presented in Figures (4-14) through (4-21). Figure (4-14) shows the gain-frequency, and phase-frequency performance of the BPF assuming default transistor parameters with $\beta$ = 450. Tuning the $Q$-factor is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA. Figure (4-15) shows the same results but when using practical transistor parameters as that used in previous simulations of chapter 3. Figures (4-16) and (4-17) show the gain- and phase-frequency performance of the BPF for different $w_c$ assuming default BJT parameters with $\beta$ = 450 and practical parameters, respectively. Tuning $w_c$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 0.1mA. A $Q$-factor of 1 is assumed.

In all previous graphs a saturation behavior can be noticed as the frequency decreases. Although these saturation levels are out of band, they affect the minimum frequency range that the BPF can be used at. This saturation is mainly due to the proportional decrease in the levels of the residual currents inside integrators circuits. This is because the effect of the base currents of the BJTs, especially those parallel to the capacitors, of Figure (3-1) becomes dominant. As discussed before, this problem can be partially solved either using compensation currents or BJTs with higher $\beta$. Using BJTs with higher $\beta$ can solve the problem effectively. Yet, this may impose conditions on the cutoff frequency of the BJT and thus limits the high frequency range. Using compensation currents, on the other hand, does not impose any limits on the high frequency range. Figures (4-18) and (4-19) show comparison between the

performance of compensated and uncompensated circuits for two different center frequencies, 50 KHz and 10 MHz respectively.

Choosing the values of the compensation currents is a little bit simple. As the values of these currents are not only proportional to the input signal, as discussed earlier, but also to the level of the tuning currents, $I_{A1,2,}$ the user can either compensate for each required center frequency independently or simply compensate at midband. Of course compensating at each center frequency will give much better results. Figures (4-20) and (4-21) show the same results of Figures (4-16) and (4-17) but with $Q$ = 10. In these simulations, compensation currents adjusted to compensate for the tuning current of the smallest $w_c$. The effect of adjusting these currents to one value of the tuning currents is noticeable on the peak values of these curves. In applications require to work at pre-determined center frequencies, the variation in the peak values become of minor importance since the compensation currents can be set according to these center frequencies.

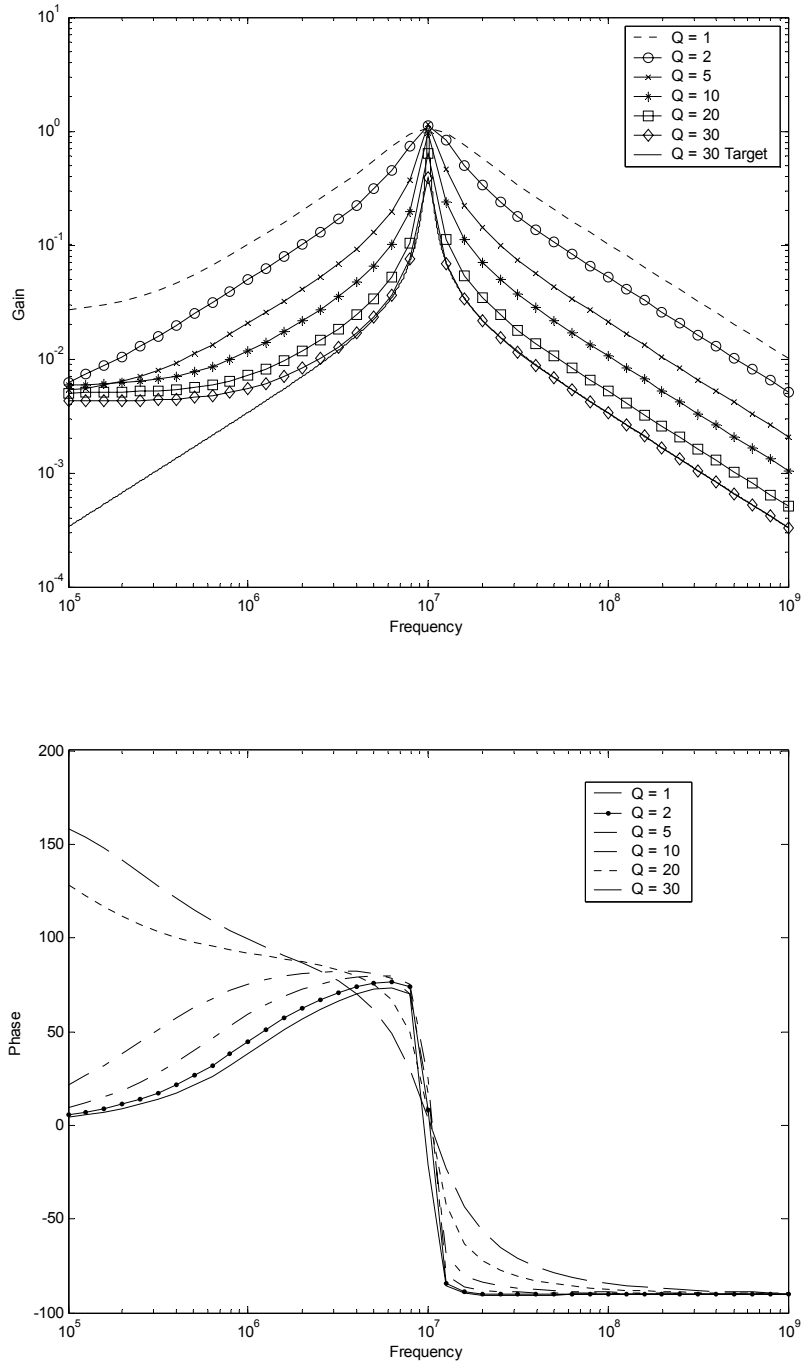



**Figure 4-14** Gain- and Phase responses of the BPF with default parameters with $\beta$ = 450. Tuning the $Q$-factor is achieved via $I_A$. $I_{B1,2}$ = 1mA

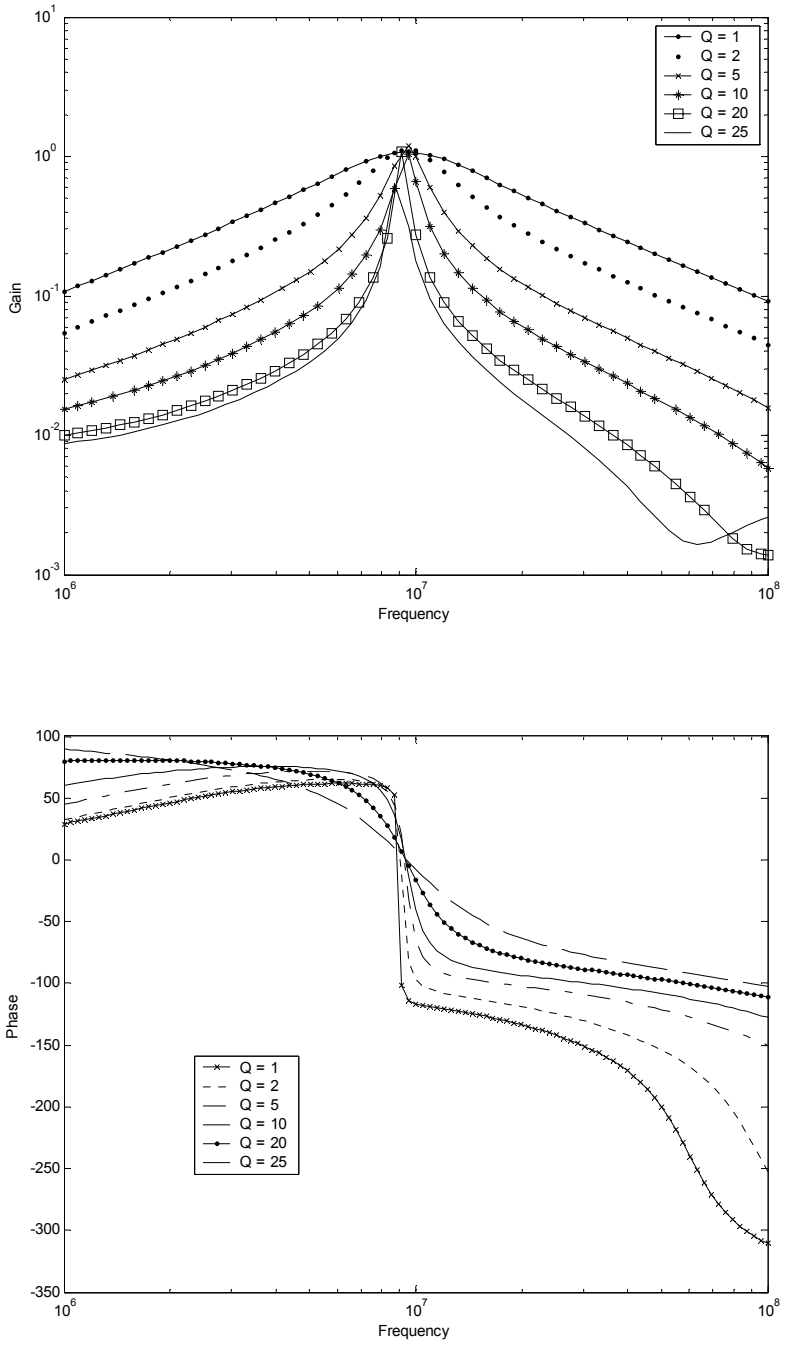



**Figure 4-15** Gain- and Phase-Frequency response of the BPF assuming practical transistor parameters. Tuning the *Q*-factor is achieved as in Figure (4-14) under the same biasing current values.

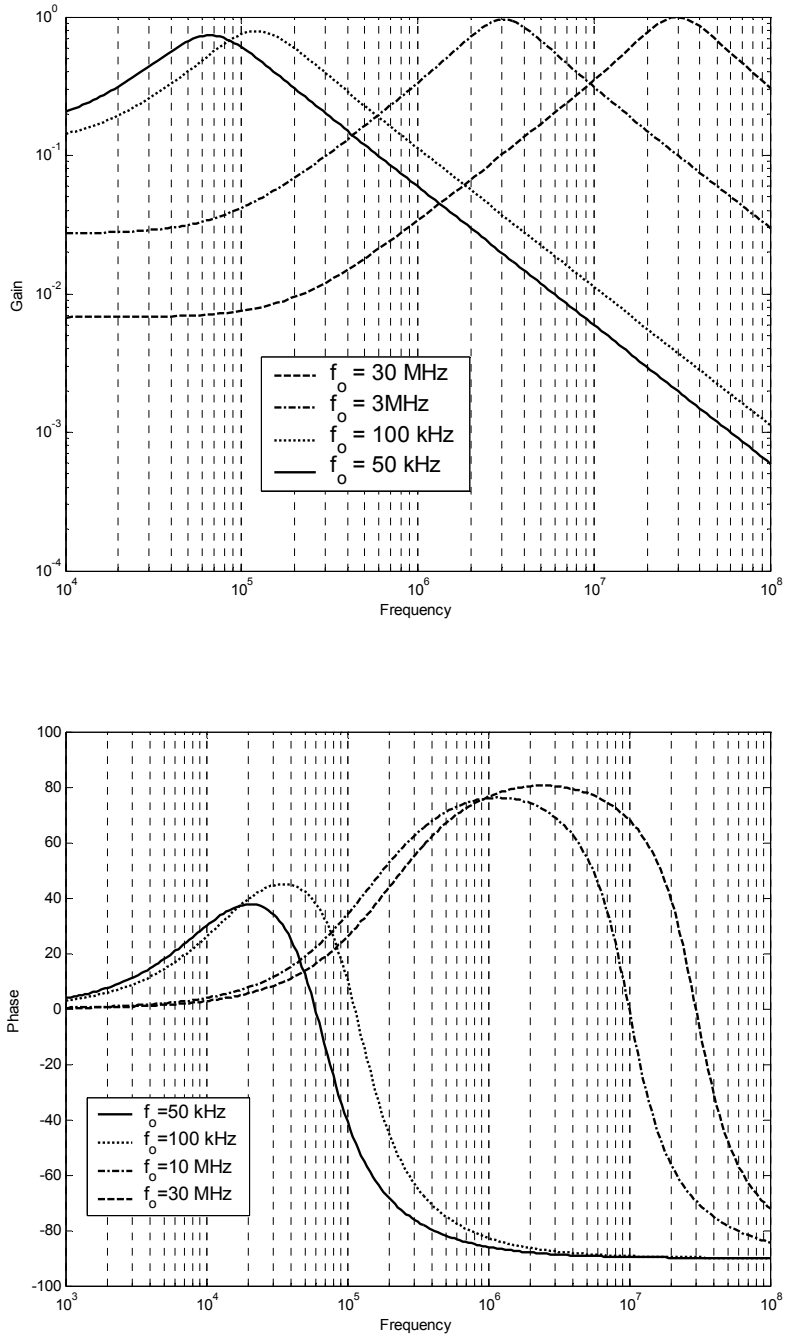



**Figure 4-16** Gain- and Phase-Frequency response of the BPF with default parameters with $\beta$ = 450. Tuning the center frequency $w_o$ is achieved via $I_A$ as in Figure (4-12). $I_{B1,2}$ = 0.1mA $Q$ = 1. No compensation currents used.

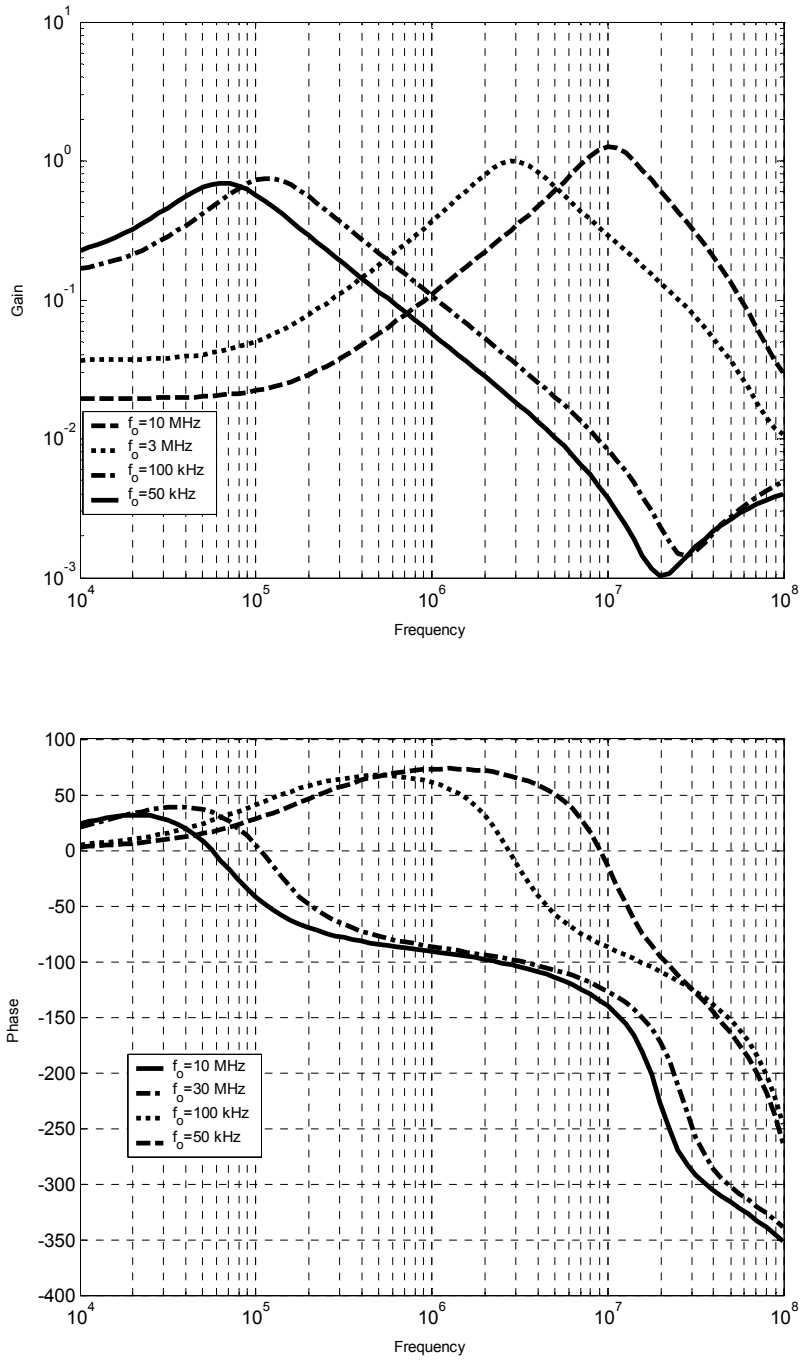



**Figure 4-17** Gain- and Phase-Frequency response of the BPF assuming practical parameters. Tuning the center frequency $f_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 0.1mA $Q$ = 1. No compensation currents used.

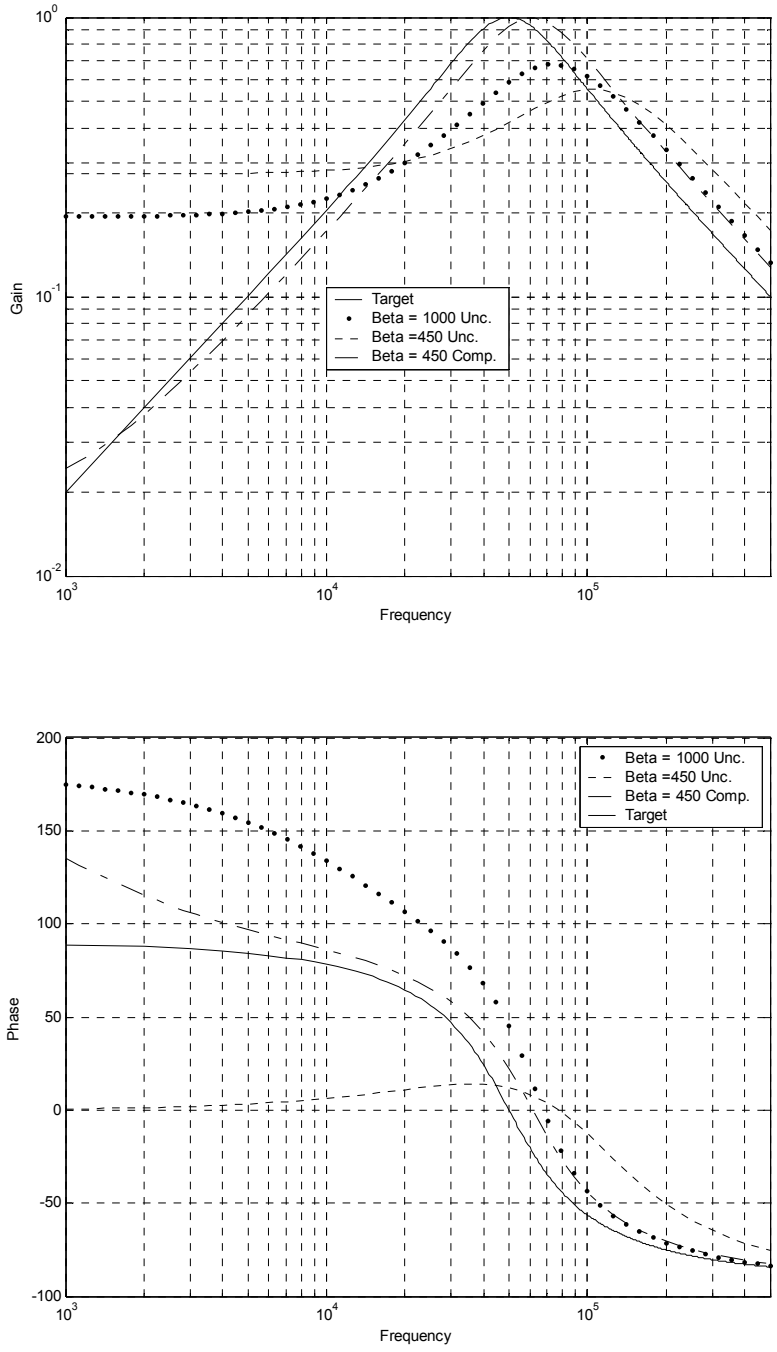



**Figure 4-18a, b** Effects of using compensation currents on the frequency response performance. Center frequency = 50KHz.

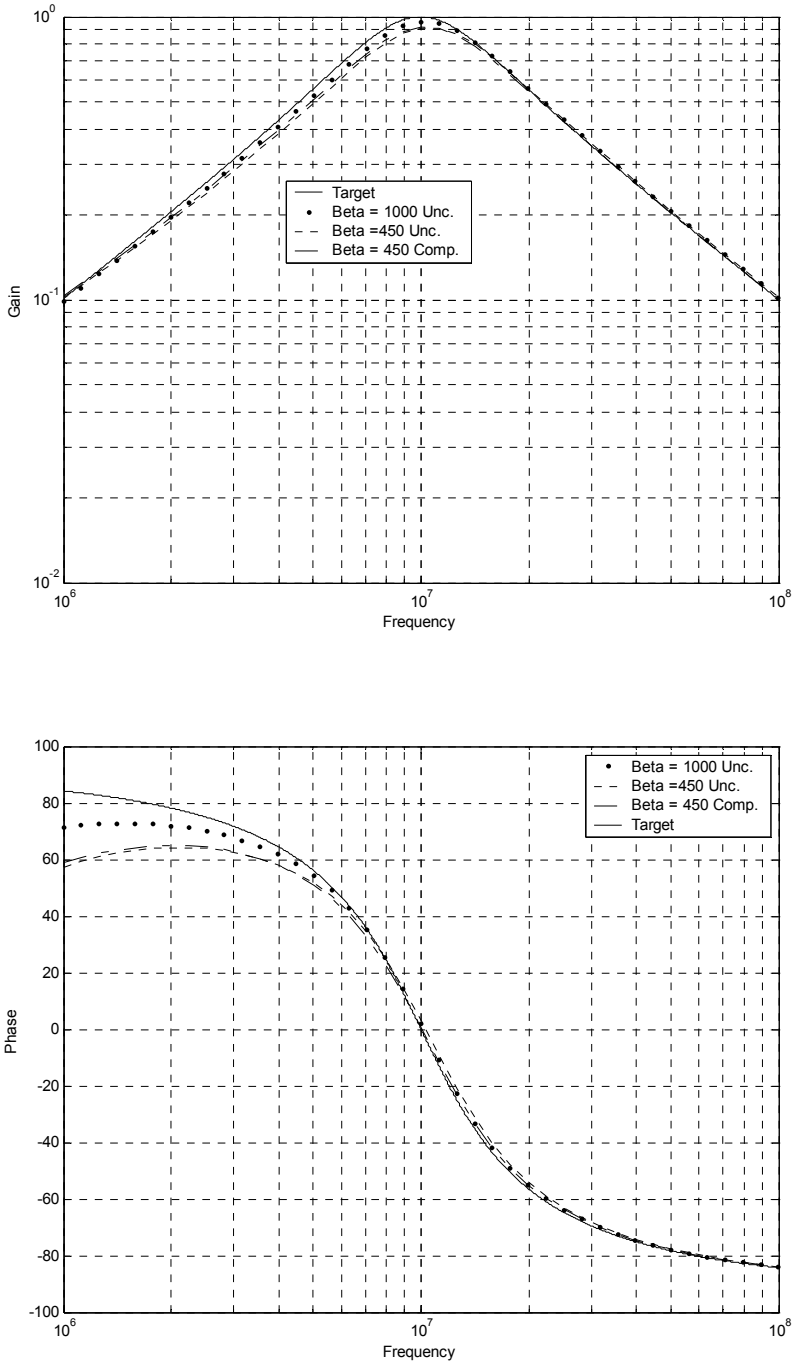



**Figure 4-19** Effects of using compensation currents on the frequency response performance. Center frequency = 10MHz

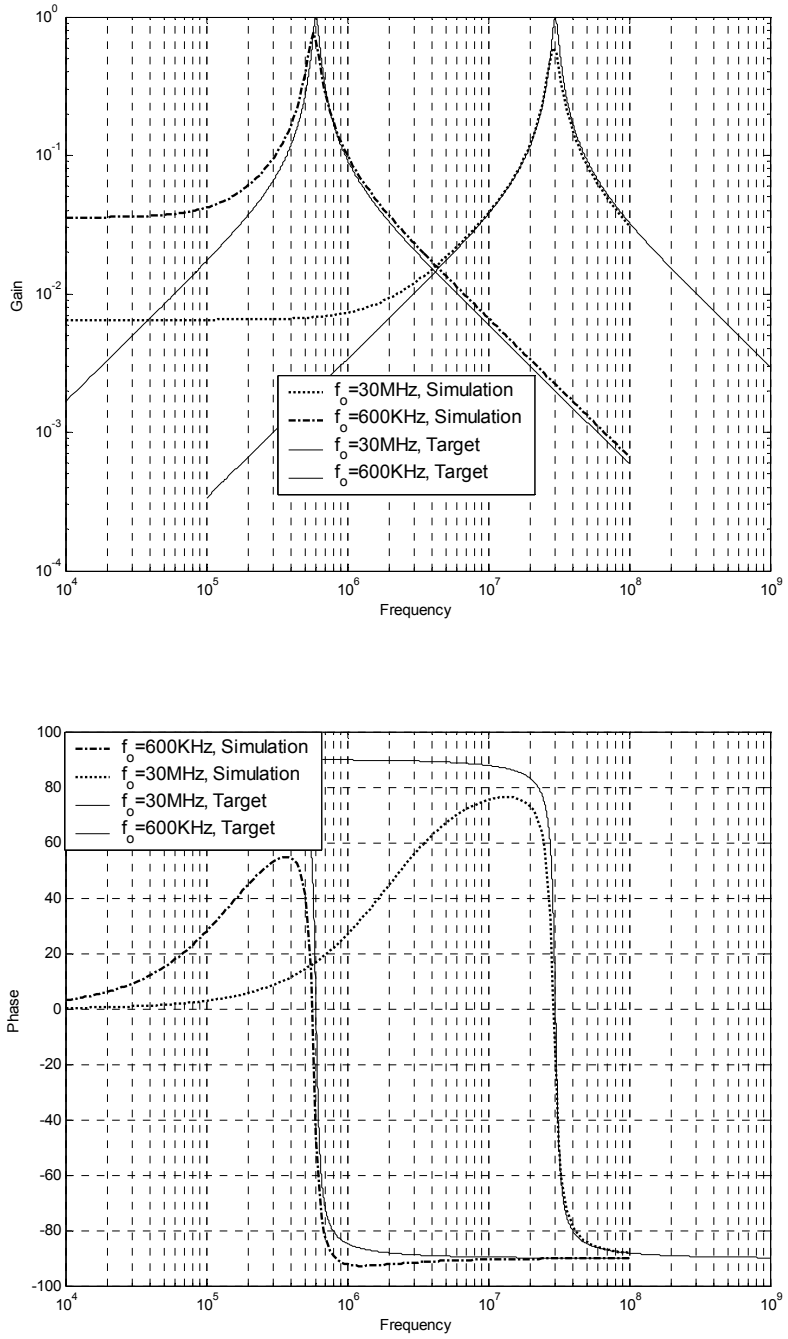



**Figure 4-20** Gain- and Phase-Frequency response of the BPF assuming default parameters with $\beta$ = 450. Tuning the center frequency $f_o$ is achieved via $I_A$ while maintaining the values of $I_{B1,2}$ = 0.1mA $Q$ = 10. With compensation currents.

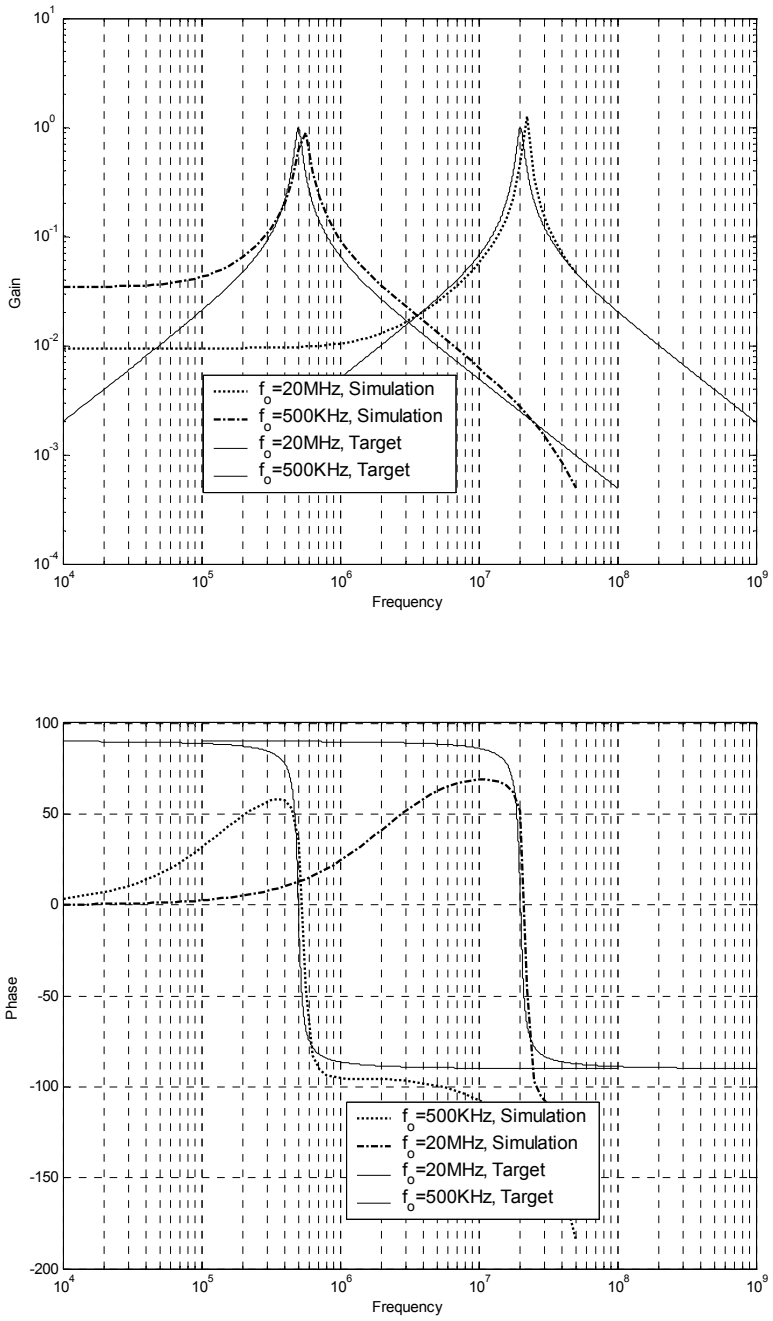



**Figure 4-21** Gain- and Phase-Frequency response of the BPF assuming practical parameters. Tuning the center frequency $f_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 0.1mA $Q$ = 10. Compensation currents used.

#### 4.1.2.3 Notch Filter

Programming the center frequency $w_o$ and the $Q$-factor for this filter is achieved exactly as for the previous LPF and BPF.

Figures (4-22) through (4-27) show the simulation results of the implemented notch filter. Figure (4-22) shows the gain- and phase-frequency characteristic curves of the Notch filter assuming default BJT parameters with $\beta$ = 450. Tuning the $Q$-factor is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA. In this simulation no compensation currents are used. Figure (4-23) shows the same results but for practical BJT parameters and with no compensation currents. It can be seen out of these two simulations that as the $Q$-factor increases, the minimum possible value that can be achieved, cutoff, decreases. This is once again due to the relatively small values of the tuning biasing currents $I_{A1,2}$, needed to achieve the required $Q$, which makes the effect of the base currents obvious. Like the case with the BPF, this problem can be toggled either by using BJTs with larger $\beta$ or by using compensation currents. Figure (4-24) shows the effects of using compensation currents compared to uncompensated performance. The center frequency $f_o$ is taken as 10MHz with a $Q$-factor of 10.

Figures (4-25) and (4-26) show the gain- and phase-frequency response of the Notch filter for two different ranges of $f_o$. The simulations performed assuming default BJT parameters with $\beta$ = 450 and no compensation currents were used. Tuning the center frequency $f_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA

with $Q$ = 1. Figure (4-26) shows the same results but with a $Q$-factor of 10. In this simulation, compensation performed around each cutoff frequency independently.

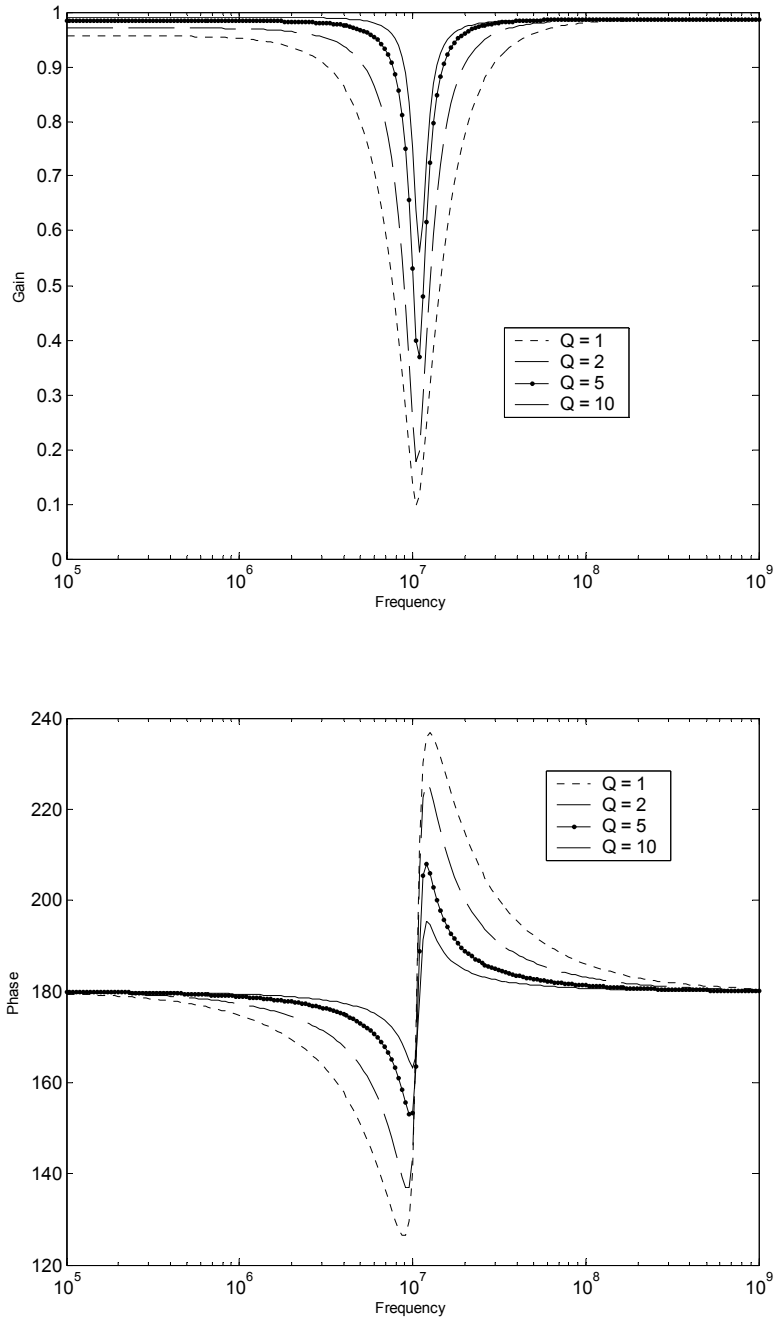



**Figure 4-22** Gain- and Phase-Frequency response of the Notch filter assuming default parameters with $\beta$ = 450. Tuning the $Q$-factor is achieved via $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA No compensation currents used.

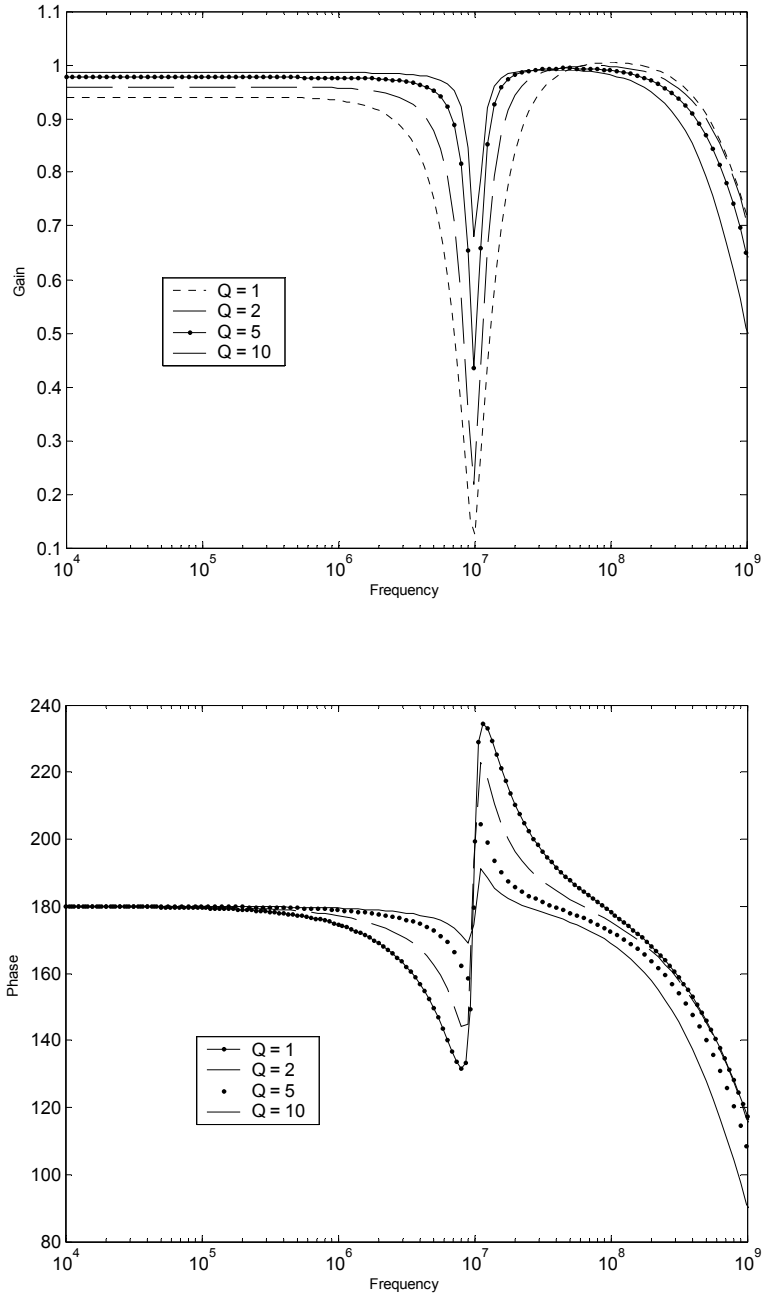



**Figure 4-23** Gain- and Phase-Frequency response of the Notch filter assuming practical parameters. Tuning the *Q*-factor is achieved via $I_A$. $I_{B1,2}$ = 1mA No compensation currents used.

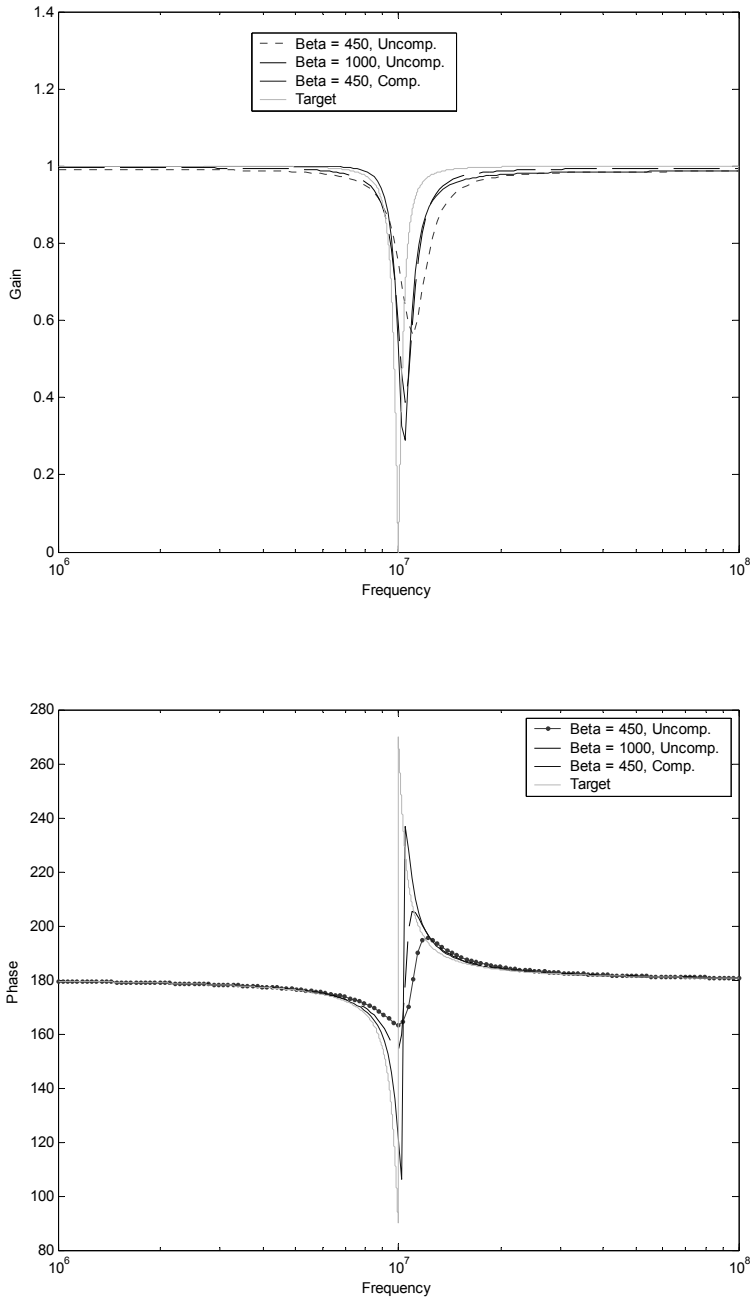



**Figure 4-24** Effects of using compensation currents on the frequency response performance. Center frequency = 10MHz and *Q*-factor = 10.

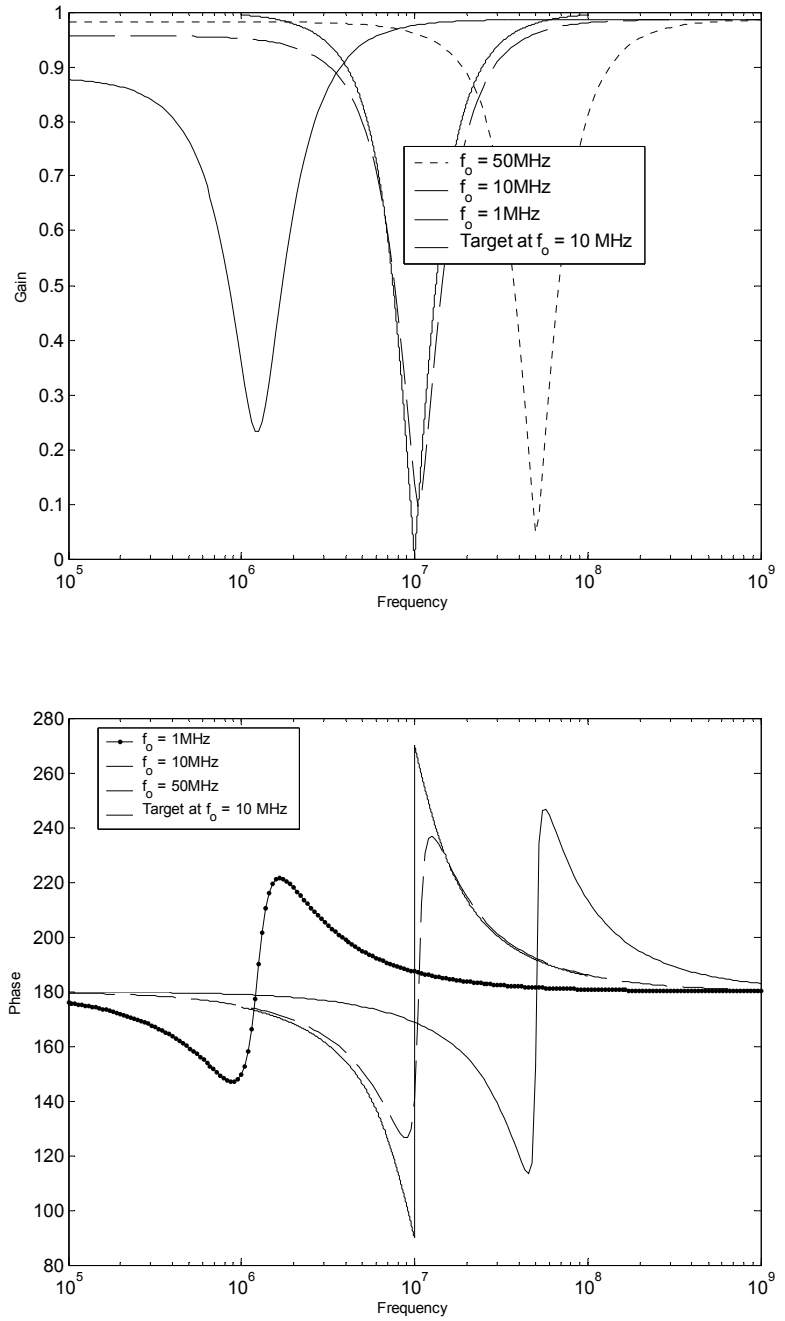



**Figure 4-25** Gain- and Phase-Frequency response of the Notch filter assuming default BJT parameters with $\beta = 450$. Tuning the cutoff frequency $w_c$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA $Q$ = 1. No compensation currents used.

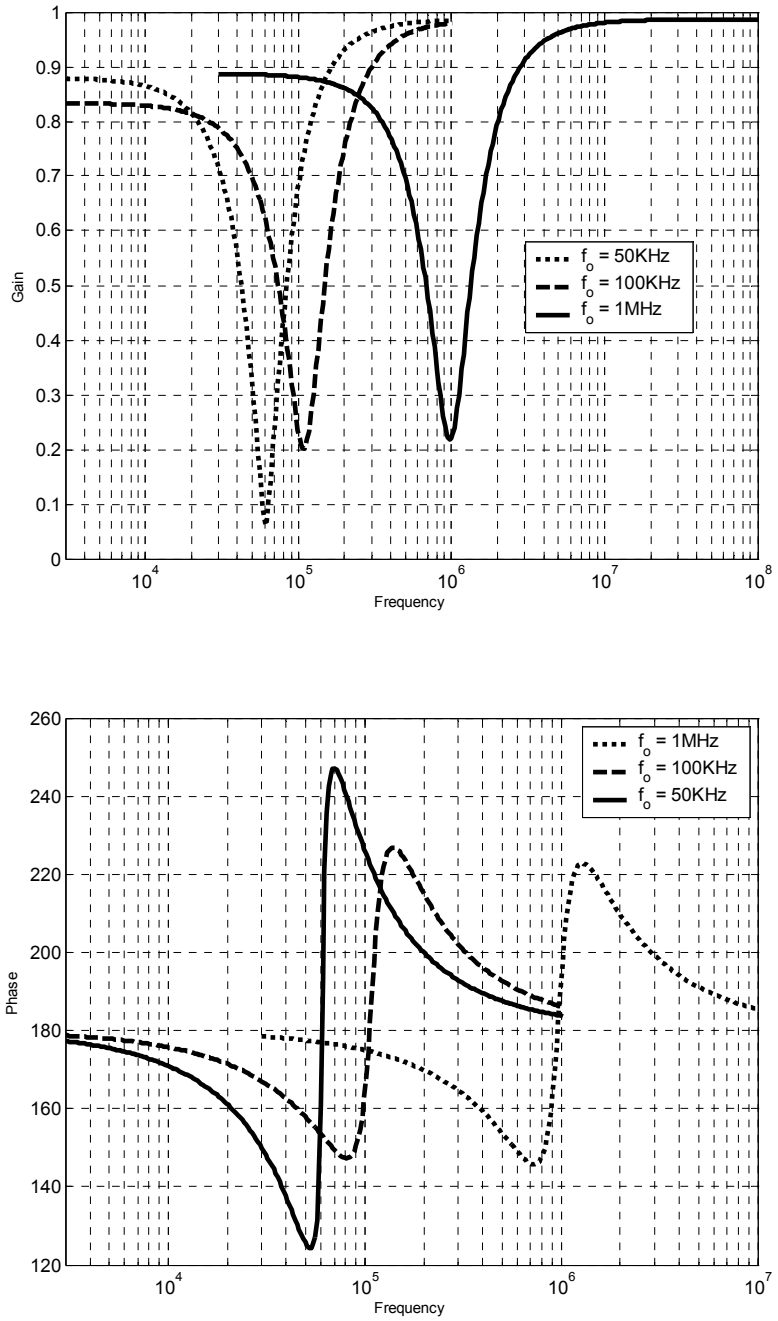



**Figure 4-26** Gain- and Phase-Frequency response of the Notch filter assuming default BJT parameters with $\beta$ = 450. Tuning the cutoff frequency $w_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 10mA $Q$ = 1. Circuit compensated around $f_o$=50KHz.

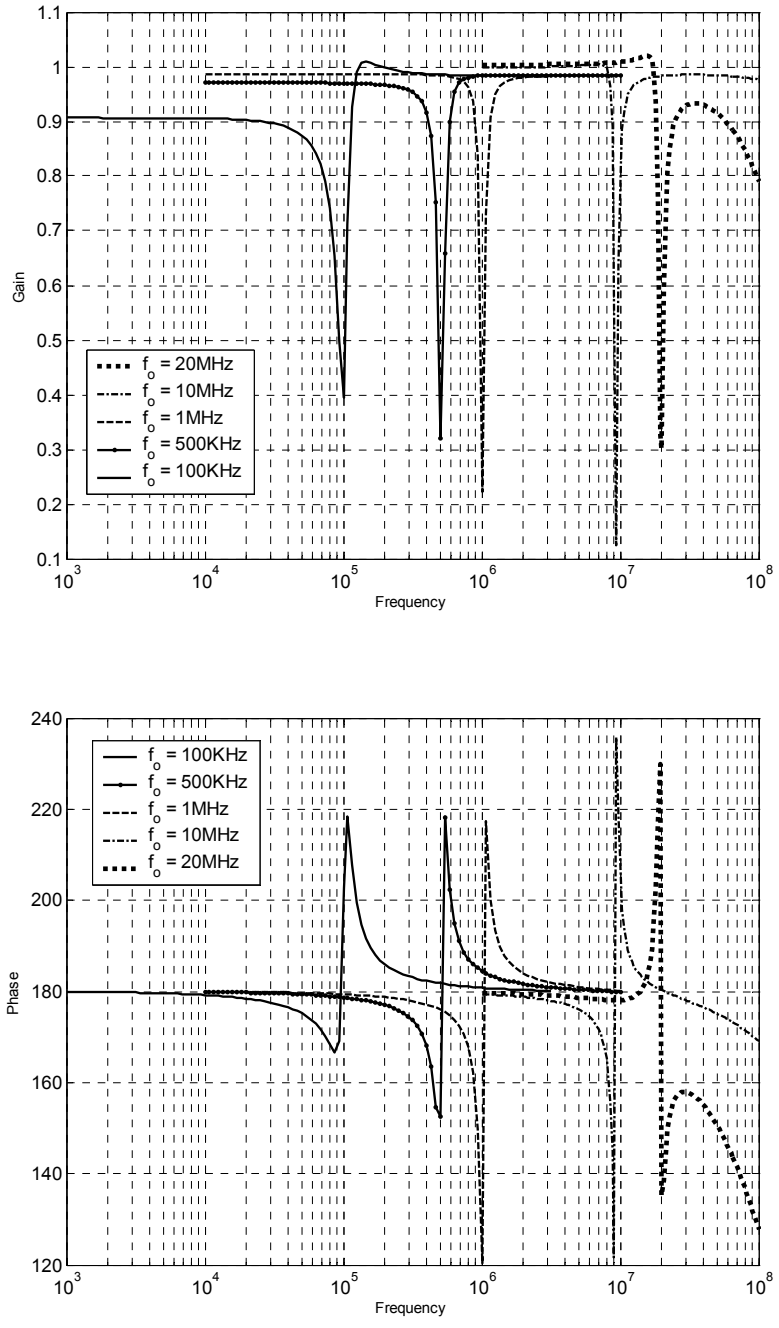



**Figure 4-27** Gain- and Phase-Frequency response of the Notch filter assuming practical parameters. Tuning the cutoff frequency $w_o$ is achieved via $I_A$. $I_{B1,2}$ = 1mA $Q$ = 10. Circuit compensated around each center frequency independently.

#### 4.1.2.4 High Pass Filter

Figures (4-28) and (4-29) show the simulation results of the gain- and phase-frequency performance of the implemented HPF for a $Q$-factor of one and two respectively. In these simulations, default transistor parameters with $\beta$ = 450 are assumed. Tuning the $w_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA. No compensation currents used. Figure (4-30) shows the effect of using compensation currents on the saturation performance of this filter at the low frequency side of the characteristic curves.

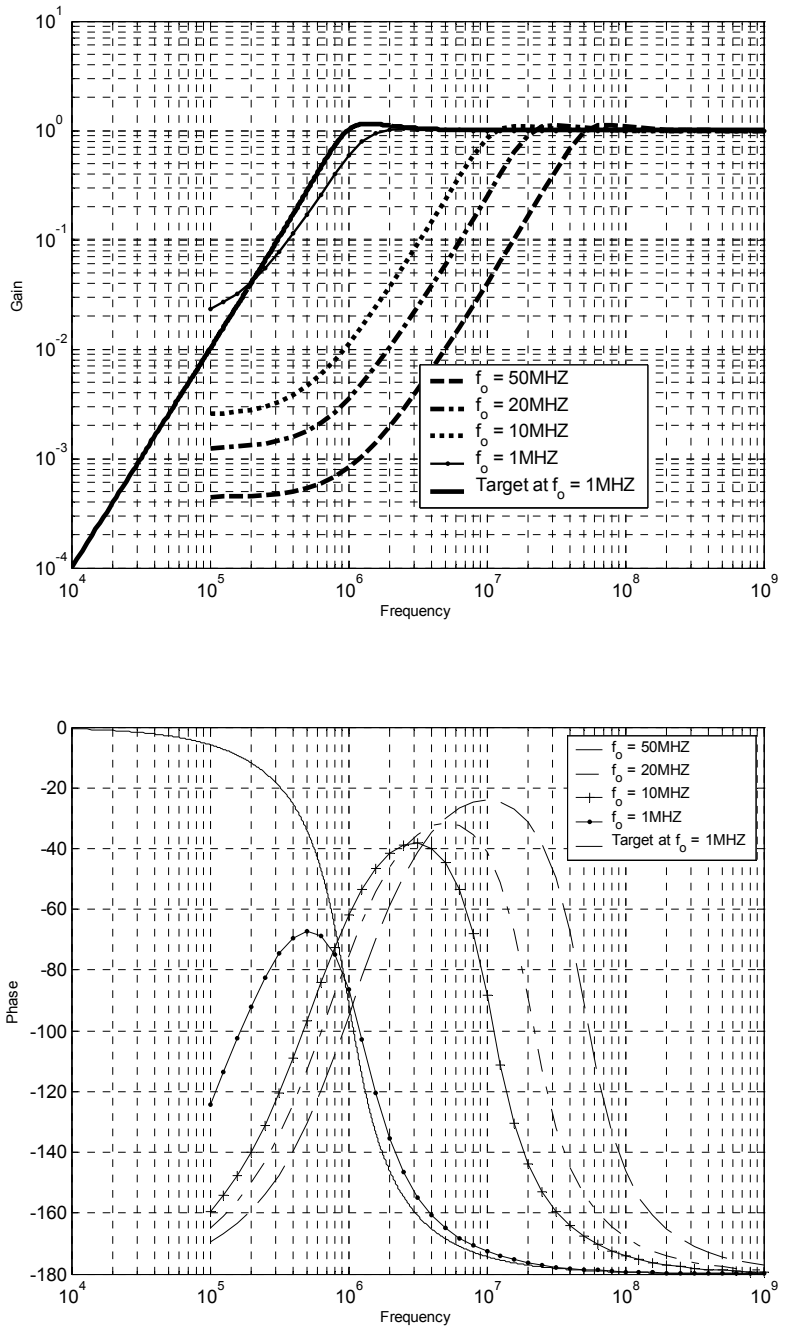



**Figure 4-28** Gain- and Phase-Frequency response of the HPF assuming default transistor parameters with $\beta$ = 450. Tuning the $w_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA. $Q$ = 1. No compensation currents used.

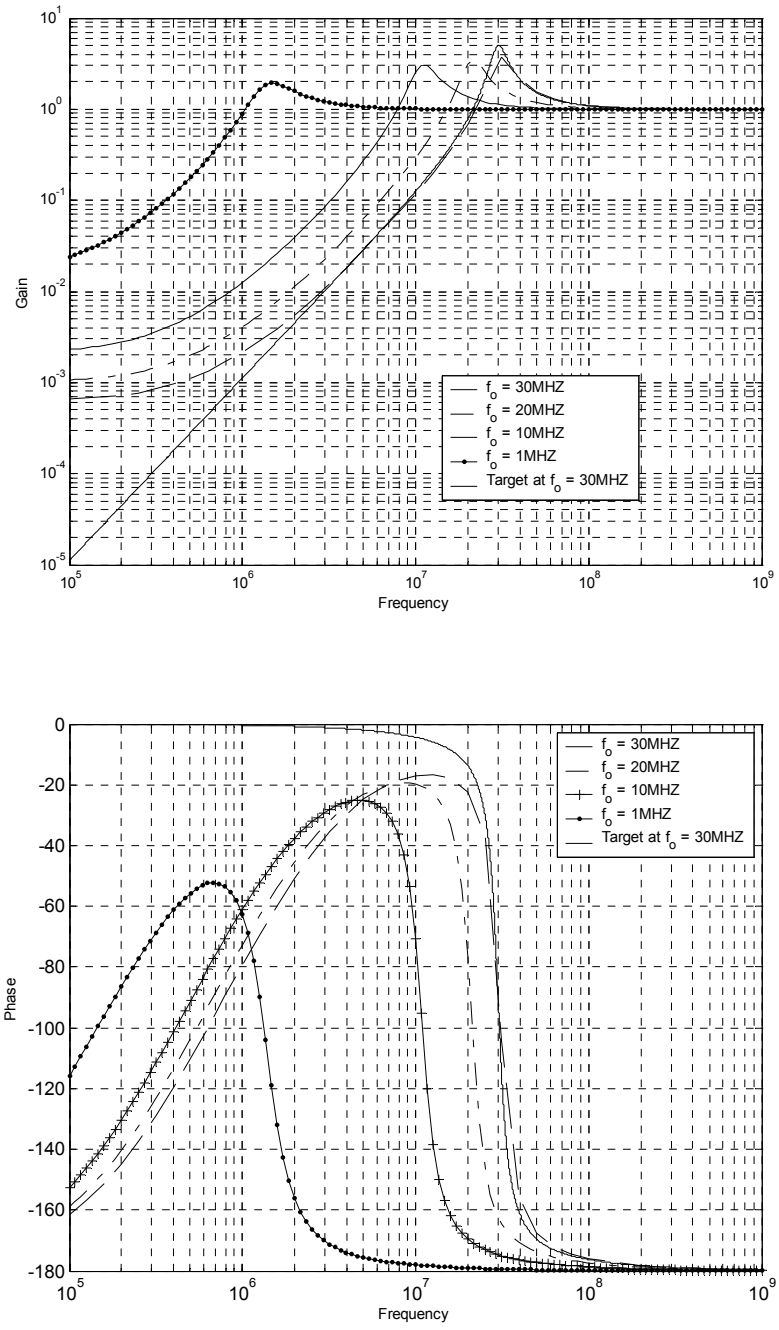



**Figure 4-29** Gain- and Phase-Frequency response of the HPF assuming default transistor parameters with $\beta$ = 450. Tuning the $w_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA. $Q$ = 5. No compensation currents.

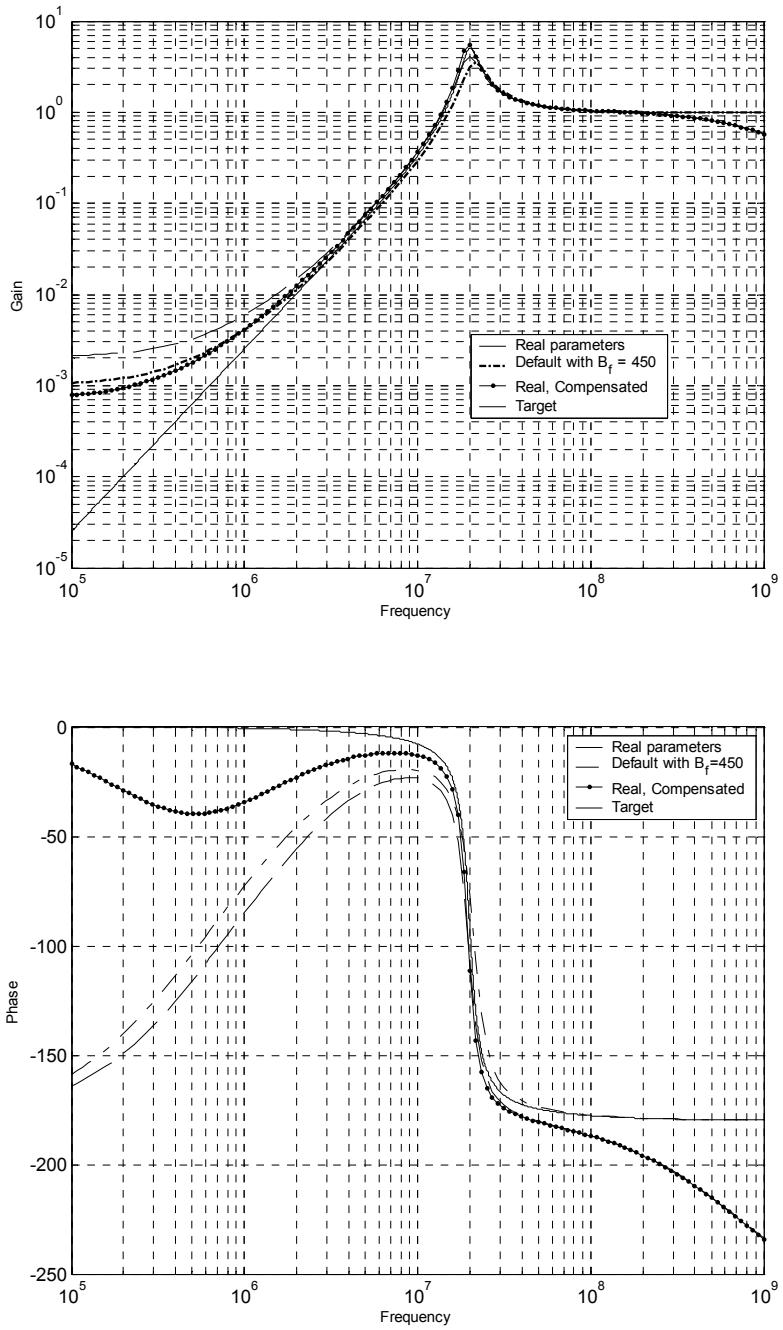



**Figure 4-30** Effects of using compensation currents on the saturation performance at low frequencies. Center frequency = 20MHz and *Q*-factor = 5.

#### 4.1.2.5 All-Pass Filter

Figures (4-31), (4-32) and (4-33) show the simulation results for the implemented all-pass filter. In Figure (4-31) simulations done assuming default BJT parameters with $\beta$ = 450 and $Q$ = 1. Simulations in Figures (4-32) and (4-33) are done assuming practical transistor parameters with $Q$ = 1 and 5 respectively. In both cases the circuit is compensated at $f_o$ = 500KHz

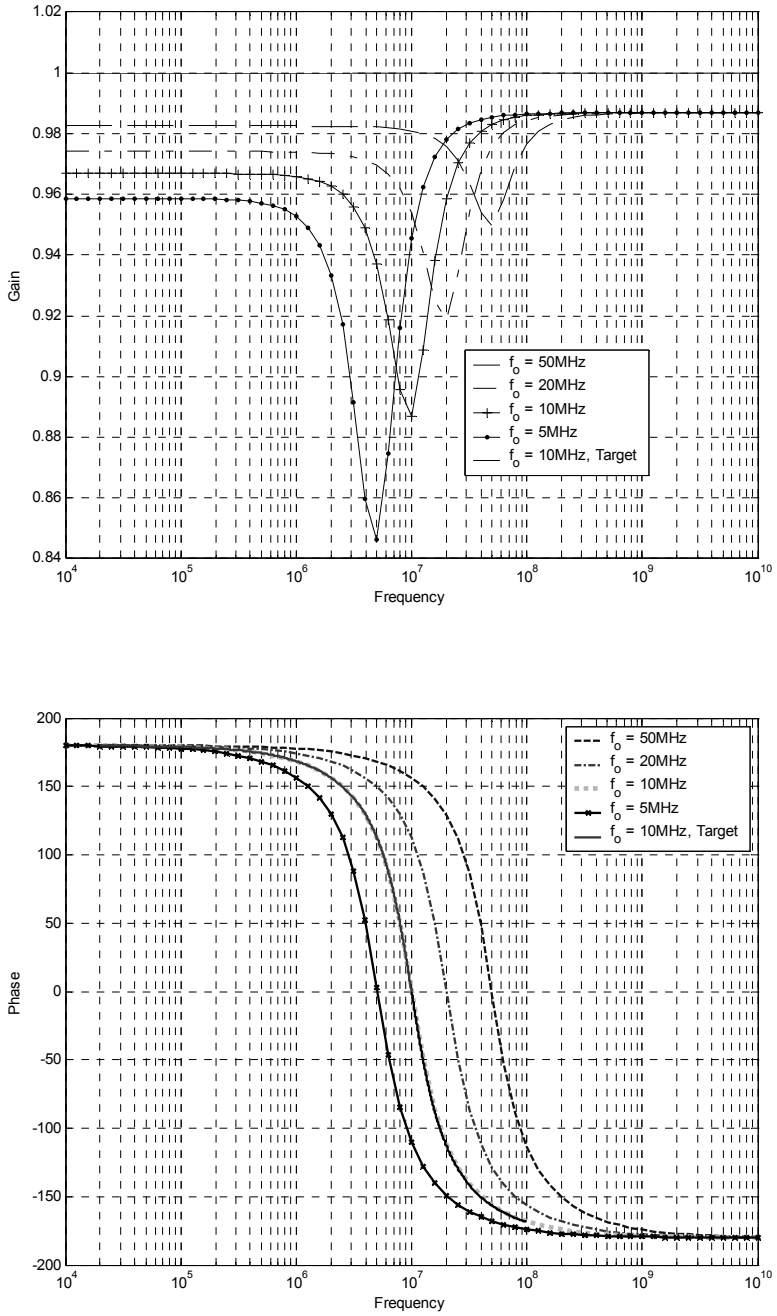



**Figure 4-31** Gain- and Phase-Frequency response of the APF assuming default transistor parameters with $\beta$ = 450. Tuning the $w_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA. $Q$ = 1. No compensation currents used.

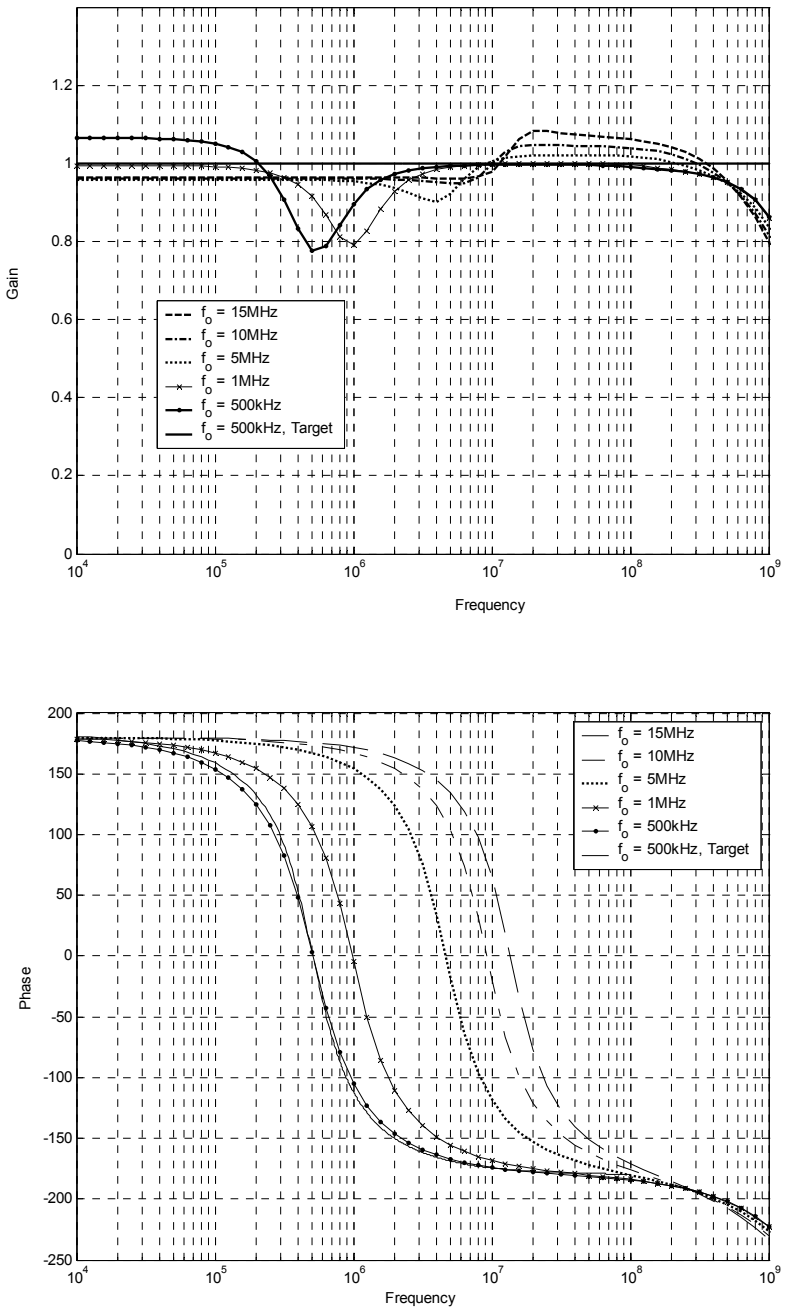



**Figure 4-32** Gain- and Phase-Frequency response of the all-pass filter assuming practical BJT parameters. Tuning the $w_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA. $Q$ = 1. Circuit compensated at $f_o$ = 500KHz.

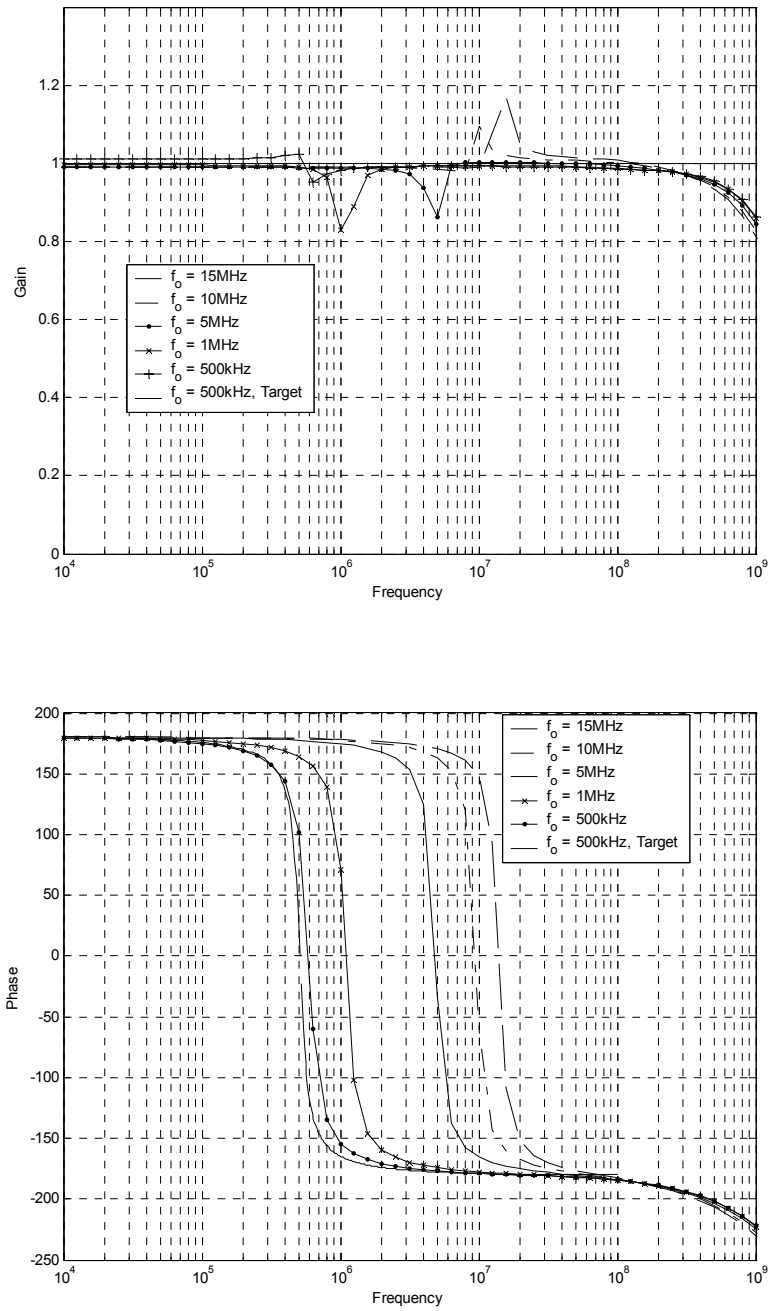



**Figure 4-33** Gain- and Phase-Frequency response of the all-pass filter assuming practical BJT parameters. Tuning the $w_o$ is achieved by changing $I_A$ while maintaining the values of $I_{B1,2}$ = 1mA. $Q$ = 5. Circuit compensated at $f_o$ = 500KHz.

#### 4.1.2.6 Filters Specifications

In addition to all advantages associated with current-mode techniques, the proposed filters have the advantage of being realized using differential-input differential-output integrator cells and thus are suitable for integration. Both the center frequency and the *Q*-factor of these filters are orthogonally tunable using biasing currents. As the maximum value of the capacitors that can be provided by integration is very limited, and because the minimum tuning currents are limited by the base currents of the BJTs, the proposed realization is suitable for high frequency applications. The upper bound of the frequency range is limited by the cutoff frequency of the used BJT transistors. The lower bound of the frequency range is limited mainly by the base currents of the BJTs. As the implementation of the basic integrator cells depend on the translinear loop, Section 3.1, all base currents were neglected in the derivations. Thus, as the filters need to be tuned to low frequency ranges, the tuning currents become smaller and smaller and will be dominated by the base currents. In order to reduce the effect of these base currents, compensation current are used. This helps in reducing the minimum frequency bound but at the expense of using very accurate current sources. If low frequency ranges are required, MOSFETs in subthreshold can be used safely instead of the BJTs.

Table 4-1 below summarizes the specifications of all realized filters.

**Table 4-1** Summary of simulation results of the biquadratic filter.

| **Filter Type** | | **Tuning Range** | |
|---|---|---|---|
| | | **Center frequency** | **Max *Q*-factor** |
| **LPF** | Default ($\beta$ = 450) | 50k-300MHz | 5 |
| | Realistic | 50k-100MHz | 5 |
| **BPF** | Default ($\beta$ = 450) | 50k-30MHz, $Q$ = 1<br>60k-20MHz, $Q$ = 10* | 30 at 10MHz |
| | Realistic | 500k-10MHz, $Q$ = 1<br>500k-20MHz, $Q$=10* | 20 at 10MHz |
| **Notch Filter** | Default ($\beta$ = 450) | 1M-50MHz, $Q$ = 1<br>60k-50MHz, Q = 1*<br>60k-20MHz, $Q$ = 10* | 10 at 10MHz |
| | Realistic | 100k-10MHz,<br>$Q$=10** | 7 at 10MHz |
| **HPF** | Default ($\beta$ = 450) | 1M-300MHz, $Q$ = 1 | 5 |
| | Realistic | 1M-30MHz, $Q$ = 5 | 5 |
| **All Pass Filter** | Default ($\beta$ = 450) | 5M-300MHz, $Q$ = 1 | 30 at 10MHz |
| | Realistic | 500k-15MHz, $Q$ = 1*<br>500k-10MHz, $Q$=5* | 20 at 10MHz |
| | | | |
| * Compensation currents used at one frequency. | | | |
| ** Compensation currents used at each frequency independently | | | |

## 4.2 Power Law Function Generator

Power law function generators are very attractive circuits in analog signal processing. Such circuits have many applications as basic blocks in communication electronic circuits, measurement systems and modeling of the non-linear current-voltage characteristics of many devices [109]. The general form of the power law function can be written as

$$y = A\left(\frac{x}{B}\right)^{\frac{C}{D}} \tag{4-45}$$

where *A, B, C* and *D* are constants.

Power-law circuits implemented in voltage mode techniques are usually built around operational amplifiers (Op-Amps) and diodes [110, 111], analog multipliers [112-114] or operational transconductance amplifiers (OTAs) [115-117]. Among these techniques, the OTA-based circuits are preferred due to their programmability and modularity. However, such realizations either depends on approximations of the power law function like in [116, 117] or if not are temperature dependent like in [115]. Moreover, this realization, [115], is relatively silicon intensive since it requires a large number of OTAs.

Due to the many benefits it has, Current mode implementation of power law circuits have been also reported [109, 118]. Both circuits are based on the BJT translinear principle. These circuits are a true power-low realization with temperature independent characteristics. In [109], the proposed circuit is a modification of the programmable current mirror proposed in [119]. However, due to the staking nature

of the BJTs used as diodes to get the required power law, this circuit can only operate with relatively high voltage power supplies. Simulation results reported were using ±5V.

In [118], the current-mode power law function generator circuit is based on three functional blocks, namely; a logarithmic, a multiplier and an exponential block. These three blocks are modifications of Gilbert multiplier [120]. The circuit can operate at power supply voltages even lower than 2V. However, the input and output currents of all the cells are single-input single-output. This makes them less immune to noise and thus less attractive for integration.

In this section, a realization of the power law function based on the CABs presented in Chapter 3 is proposed. The realization consists of four cascaded CABs. The first two are configured as logarithmic blocks and the last two as exponential blocks.

### 4.2.1 Proposed Realization

The proposed realization, shown in Figure (4-34), consists of four cascaded CABs. The first two are configured as logarithmic blocks and the others as exponential blocks.

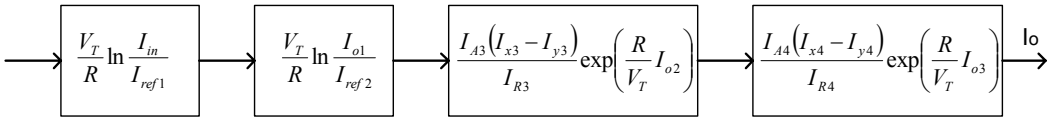



**Figure 4-34** Block diagram of the proposed power law circuit.

Recall that the functional relationships of both the logarithmic and exponential sub-cells are

$$I_{o_i} = \frac{V_T}{R}\ln\frac{I_{in_i}}{I_{ref_i}} \tag{4-46}$$

and

$$I_{o_i} = \frac{I_{A_i}\left(I_{y_i} - I_{x_i}\right)}{I_{R_i}}\exp\left(\frac{R}{V_T}I_{in_i}\right) \tag{4-47}$$

respectively. The sub-index *I* is to indicate the number of the cell. Taking the output of the first logarithmic cell as the input of the second one which is also logarithmic results in

$$I_{o_2} = \frac{V_T}{R}\ln\left[\frac{\frac{V_T}{R}\ln\frac{I_{in}}{I_{ref_1}}}{I_{ref_2}}\right] \tag{4-48}$$

Taking the reference current $I_{ref_2} = \frac{V_T}{R}$, equation 4-48 simplifies to

$$I_{o_2} = \frac{V_T}{R} \ln\left[ \ln\left( \frac{I_{in}}{I_{ref_1}} \right) \right] \tag{4-49}$$

Taking $I_{o_2}$ as the input to the third block configured as exponential cell yield,

$$I_{o_3} = \frac{I_{A_3}\left(I_{y_3} - I_{x_3}\right)}{I_{R_3}} \left[ \ln\left( \frac{I_{in}}{I_{ref_1}} \right) \right] \tag{4-50}$$

Equation (4-50) can be rewritten as

$$I_{o_3} = \left(I_{y_3} - I_{x_3}\right) \ln\left[ \left( \frac{I_{in}}{I_{ref_1}} \right)^{\frac{I_{A_3}}{I_{R_3}}} \right] \tag{4-51}$$

The resulting output current of the last stage is thus

$$I_o = \frac{I_{A_4}\left(I_{y_4} - I_{x_4}\right)}{I_{R_4}} \exp\left( \frac{R}{V_T}\left(I_{y_3} - I_{x_3}\right) \ln\left[ \left( \frac{I_{in}}{I_{ref_1}} \right)^{\frac{I_{A_3}}{I_{R_3}}} \right] \right) \tag{4-52}$$

Once again, taking $\left(I_{y_3} - I_{x_3}\right) = \frac{V_T}{R}$, equation (4-52) can be rewritten as

$$I_o = \frac{I_{A_4}\left(I_{y_4} - I_{x_4}\right)}{I_{R_4}} \left( \frac{I_{in}}{I_{ref_1}} \right)^m \tag{4-53}$$

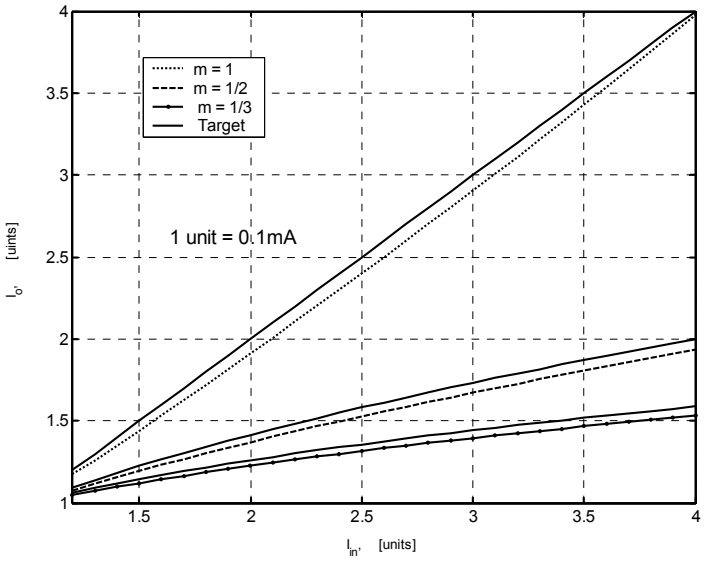
where $m = \frac{I_{A_3}}{I_{R_3}}$. By comparing equation (4-53) and equation (4-45), one can see that all constants, *A*-*D*, are represented by programmable biasing currents. It is worth noting here that although the CABs by themselves have temperature dependent characteristics, the net result is temperature independent. This temperature-

independent characteristic can be achieved in all applications requiring equal number of logarithmic and exponential blocks in the signal path.

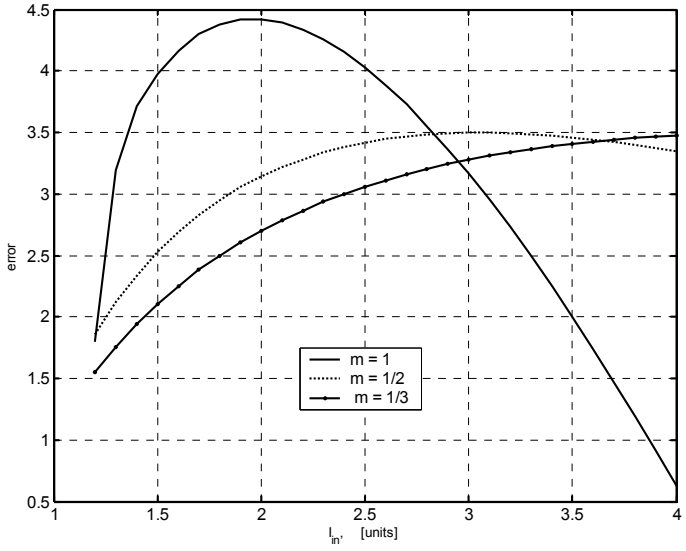
Because the current sources represent the power law are unidirectional, this power-factor is limited to positive numbers. However, if negative numbers are required, adding stages to take the inverse of the output current is straightforward.

### 4.2.2 Simulation Results

In order to verify the performance of the proposed power law generator, the proposed configuration is simulated using the same real BJT transistor model used before. Figure (4-35) shows the simulation results for different power law orders less than or equal to one. In these simulations the value of the resistor appearing in the logarithmic function is taken twice as that of the exponential function and with a value of 5.2kΩ. Thus all currents are normalized to 0.1mA. It can be seen from these results that an input dynamic range up to 4 units is achieved. Also the percentage error between these simulation results and the target ones is below 4.5% in its worst case.




(a)




(b)

**Figure 4-35** a) Simulations of the circuit performance for different values of the power factor $m = \frac{I_{A_3}}{I_{R_3}}$, and b) Percentage error.

Figure (4-36) shows simulation results for power-factors larger than one. It can be seen from this figure that the input dynamic range is much lower than the previous case. This is due to the relatively large resultant common-mode currents at the output of mainly the final exponential block. In order to partially solve this problem and thus to increase the input dynamic range, the currents can be shifted down to be normalized at 10uA rather than 100uA. This suggests that the values of the resistors used in the cells to be 10 times larger. However, deriving the BJTs to operate at lower biasing levels will impose limits on the usable bandwidth of the circuit. Figure (4-37) shows simulation results the frequency response of the circuit for both cases. From this figure, it can be seen that the bandwidth dramatically dropped from nearly 400MHz down to 40MHz (for phase error of less than $10^{o}$, the bandwidth dropped from 15MHz down to 500KHz).

Another very important factor to be noted for this case is the base currents of the transistor deriving the differential output currents of the exponential block. As the power factor increases, these output currents will increase and thus the base currents of transistors $Q_1$ and $Q_{11}$ in Figure (3-12) are going to dominate the reference current $I_R$. This will result in a large error in the total output. In order to solve this problem, both $Q_1$ and $Q_{11}$ must be biased without affecting the other currents inside the circuit and at the same time maintain the basic translinear loops. A suggested solution to this problem is to include emitter-coupled pair as the one formed from $Q_{E1}$ and $Q_{E2}$ in front of each of $Q_1$ and $Q_{11}$ transistors. Figure (4-38) shows the suggested additional

transistors. Figure (4-39) shows the simulation results using the new current levels, *i.e.* normalized to 10$\mu$A, together with the new modified circuit. From this figure it can be seen that the input dynamic range for power factors larger than one has increased to 4 units for both $m$ = 2 and $m$ = 3 and for 2.3 for $m$ = 4. However, the percentage error for this case is considerably larger than for power factors less than 1. For $m$ = 2, the maximum error is around 4%, and for $m$ = 3 and $m$ = 4 it is around 6.5% and 7.5% respectively.

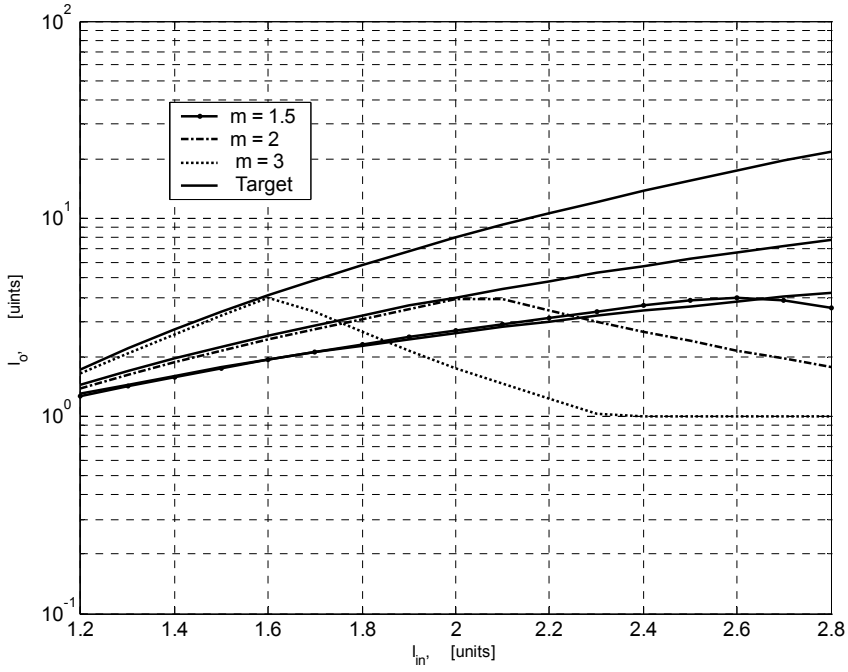
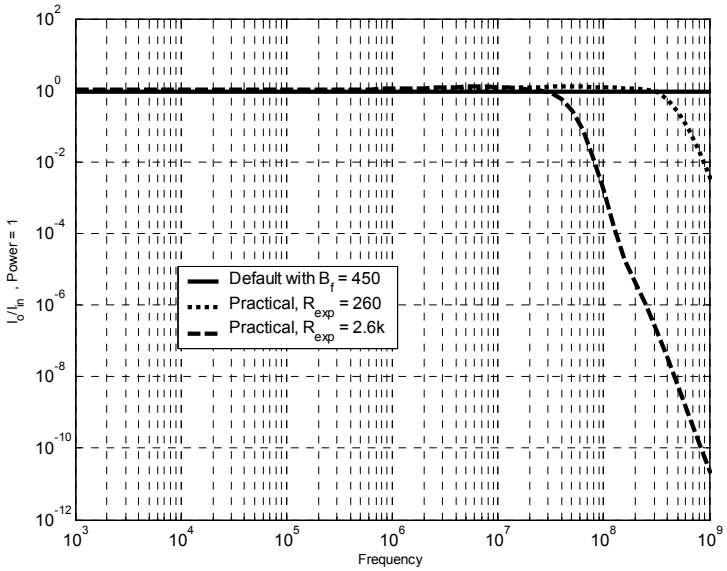
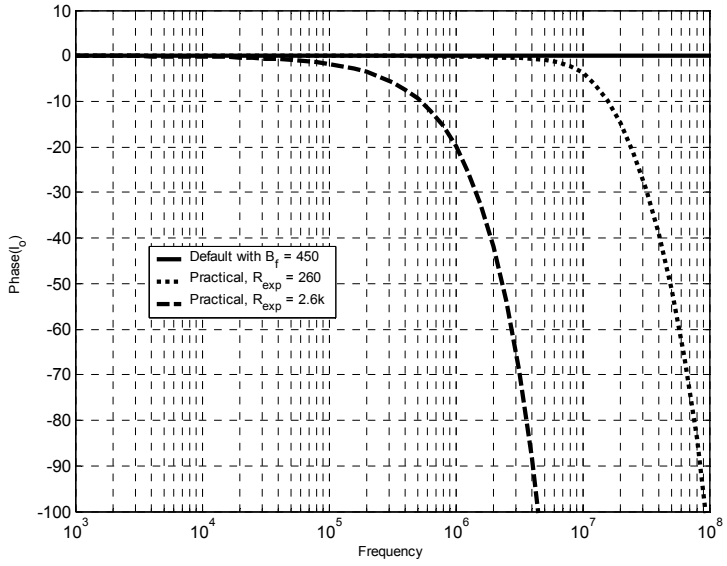



**Figure 4-36** Simulations of the circuit performance for power factor *m* larger than one. Limited input dynamic range is obvious; 2.7 units for $m = 1.5$, 2 units for $m = 2$, and 1.6 units for $m = 3$.




(a)




(b)

**Figure 4-37a, b** Frequency response of the proposed configuration for two different biasing currents levels. Power factor of one is used.

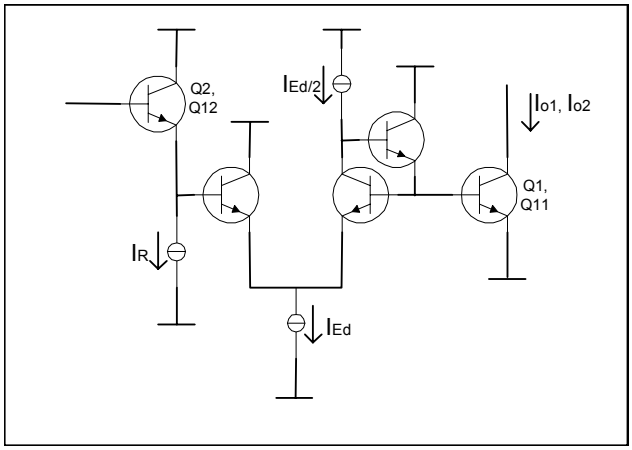
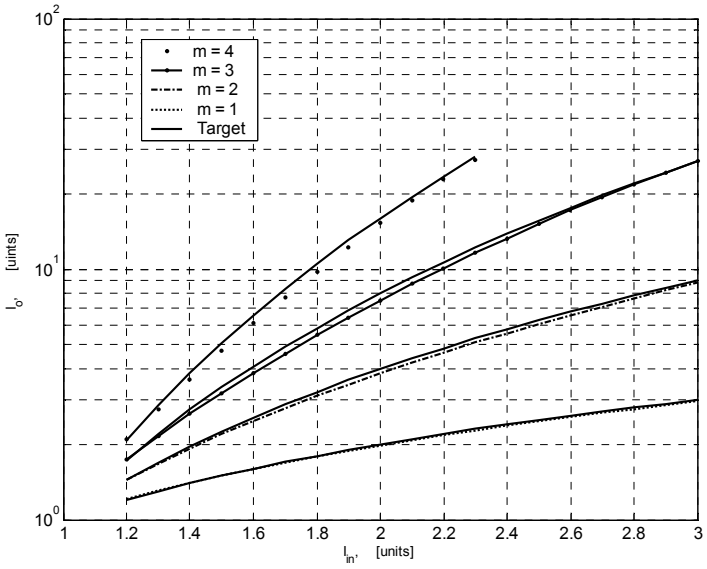
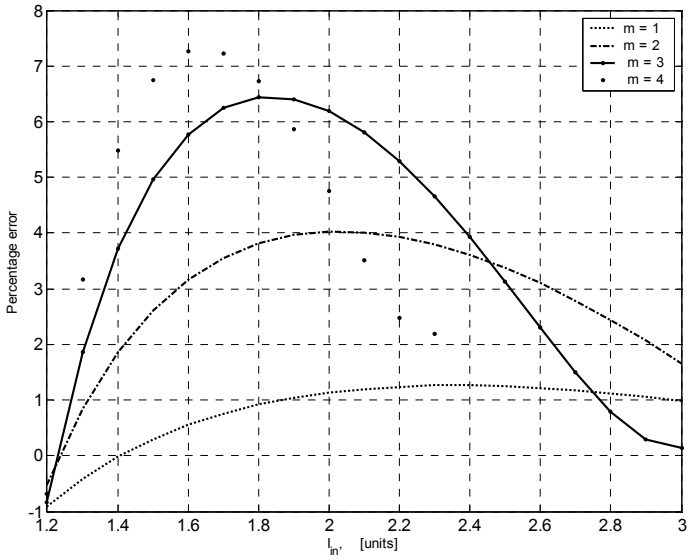



**Figure 4-38** Modified part of the exponential cell proposed in Figure (3-2).




(a)




(b)

**Figure 4-39** Simulations of the circuit performance for power factor *m* larger than one using low level biasing.

## 4.3 AM Modulator/Demodulator

As a third application of the designed CABs, an AM modulator/Demodulator is proposed and simulated. One direct implementation of AM receiver was built and tested to show the versatility of Zetex's Trac@ FPAA by Y. Sonneblick *et al* in [121]. As Trac is a voltage-mode FPAA, the design was a little bit more complicated since voltage summers needed to be designed as part of the system. The only drawback of their designed receiver, according to the authors, is that the FPAA is rather expensive. This suggests that with intensive research in the FPAA area, the main obstacle, which is the price, could be reduced sharply.

### 4.3.1 AM Modulator

Figure (4-40) shows the block diagram of a possible configuration of the CABs to work as a AM Modulator. In this block diagram, *m(t)* represents the modulating signal, *c(t)* the carrier signal, and *E* is a DC quantity to make sure that the inputs to the log-function blocks are always positive.

Recalling that the input/output relationship of the log-function circuit presented in Section (3-3), Figure (3-28), is given as

$$I_{o_i} = \frac{V_T}{R} \ln \frac{I_{in_i}}{I_{ref_i}} \tag{4-54}$$

the input to the exponential block can be represented as

$$I_{\exp_{in}} = \frac{V_T}{R} \left[ \ln \frac{m(t)+E}{I_{ref}} + \ln \frac{c(t)+E}{I_{ref}} - \ln \frac{E}{I_{ref}} \right] \tag{4-55}$$

Equation (4-55) can be simplified to give

$$I_{\exp_{in}} = \frac{V_T}{R} \ln\left[\frac{m(t)c(t) + E \cdot m(t) + E \cdot c(t) + E^2}{I_{ref} \cdot E}\right] \tag{4-56}$$

Recalling that the input/output relationship of the exponential function presented in Section (3-2-3), Figure (3-12), is

$$I_{o_i} = \frac{I_{A_i}\left(I_{y_i} - I_{x_i}\right)}{I_{R_i}} \exp\left(\frac{R}{V_T} I_{in_i}\right) \tag{4-57}$$

the output current of the exponential block is

$$I_{\exp_o} = \frac{I_A\left(I_y - I_x\right)}{I_R}\left[\frac{m(t)c(t) + E \cdot m(t) + E \cdot c(t) + E^2}{I_{ref} \cdot E}\right] \tag{4-58}$$

Setting $I_A = (I_y - I_x) = I_R = 1m\text{A}$ and subtracting the unneeded components from the output current, the final result becomes

$$I_o = \frac{1}{I_{ref}}\left[\frac{m(t)}{E} + 1\right] \cdot c(t) \qquad \text{(units)} \tag{4-59}$$

which represents full AM modulated waveform. If a suppressed-carrier waveform is needed, one can simply subtract the component related to *c(t)* from the final result to get the needed waveform. Once again one can notice that the overall characteristics of the system are temperature independent. Choosing $E$ to be equal to $I_{ref}$ will simplify the modulation process, where the branch related to it is simply canceled.

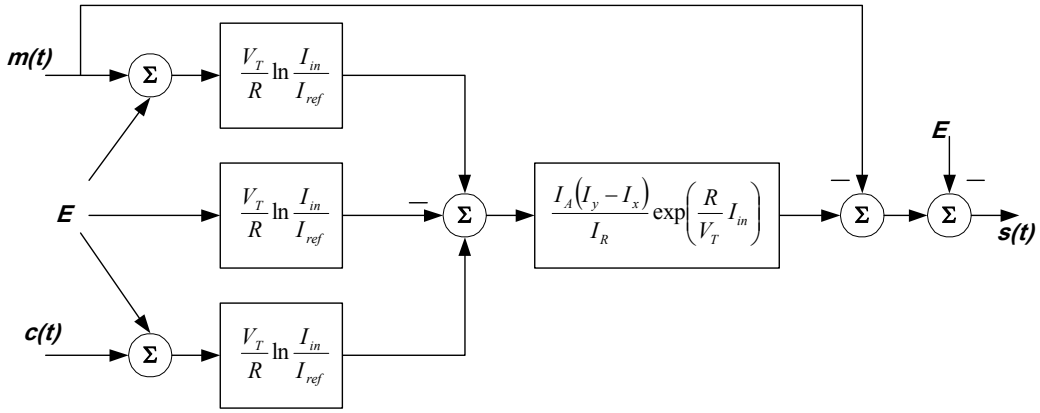



**Figure 4-40** Block diagram of the AM Modulator/Demodulator.

### 4.3.2 AM Demodulator

The same circuit used as AM modulator; Figure (4-40), can be used also as AM demodulator. The only change needed to be done is with the input to the log-function blocks. Taking the input of one of these blocks as the suppressed carrier modulated signal *m(t)c(t)*, and the input to the other block as the carrier signal *c(t)*, the output current to the exponential block can be written as

$$I_{\exp_o} = s(t) = \frac{I_A\left(I_y - I_x\right)}{I_R}\left[\frac{m(t)c^2(t) + E\cdot m(t)c(t) + E\cdot c(t) + E^2}{I_{ref}^2}\right] \tag{4-60}$$

Note that the suppressed carrier modulated signal *m(t)c(t)* is considered here to be in Amperes. The component of interest in equation (4-60) is of course $m(t)c^2(t)$. Taking $I_A = (I_y - I_x) = I_R = 1m\text{A}$ this component can be rewritten as

$$\frac{1}{I_{ref}^2}m(t)c^2(t) = \frac{1}{I_{ref}^2}m(t)\left[\frac{1}{2} + \frac{1}{2}\cos\left(2\pi f_c t\right)\right] \tag{4-61}$$

thus by introducing the output of the exponential cell to a lowpass filtering stage, the final output current will be

$$I_{\exp_o} = \frac{1}{2I_{ref}^2}m(t) + \frac{E^2}{I_{ref}^2} \tag{5-62}$$

Since the DC component of equation (5-62) is a known value, it can be subtracted from the final output to obtain the required modulating signal.

### 4.3.3 Simulation Results

Both the AM modulator and demodulator simulation results are presented in this subsection. Figure (4-41) shows the frequency spectrum of the exponential cell output current. Clearly, this graph shows four main frequency components, the first one is related to the modulating signal itself, in this example 10 kHz. The other three components are those for the required modulated signal. The carrier frequency is taken to be 800 kHz. Figures (4-42) and (4-43) show the modulated signal waveform for the two cases, full modulation and suppressed carrier modulation.

Simulation results for the AM demodulator are represented in Figures (4-44) and (4-45). Figure (4-44) shows both the modulated waveform and the constructed waveform after low pass filtering. The low pass filter used here is the same as the $2^{nd}$ order one realized in Section 3.1.2. The frequency spectrum of the constructed signal is shown in Figure (4-45). The frequency of both the modulating signal and the carrier signal are taken as in the modulating example, i.e. 10 kHz and 800 kHz respectively.

These simulation results clearly show the versatility of such CABs in wide range of applications.

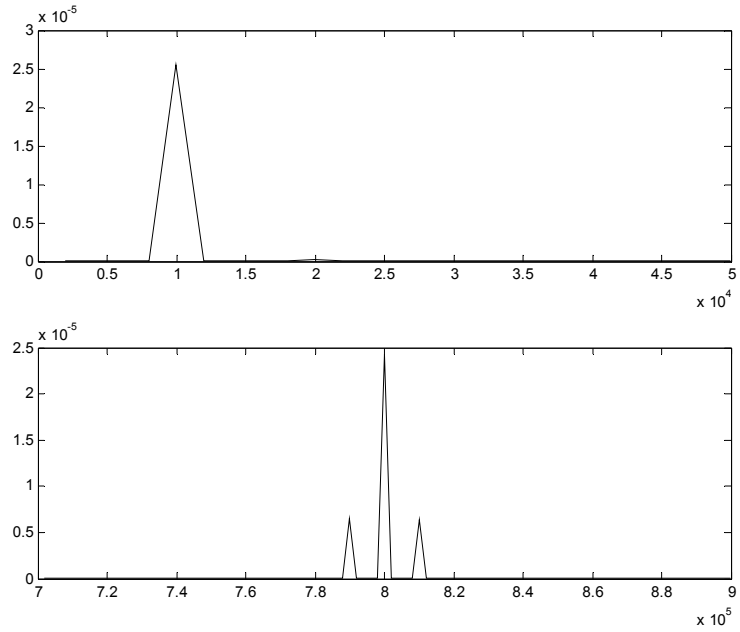



**Figure 4-41** Frequency spectrum of the resulting modulated signal before subtracting the modulating signal.

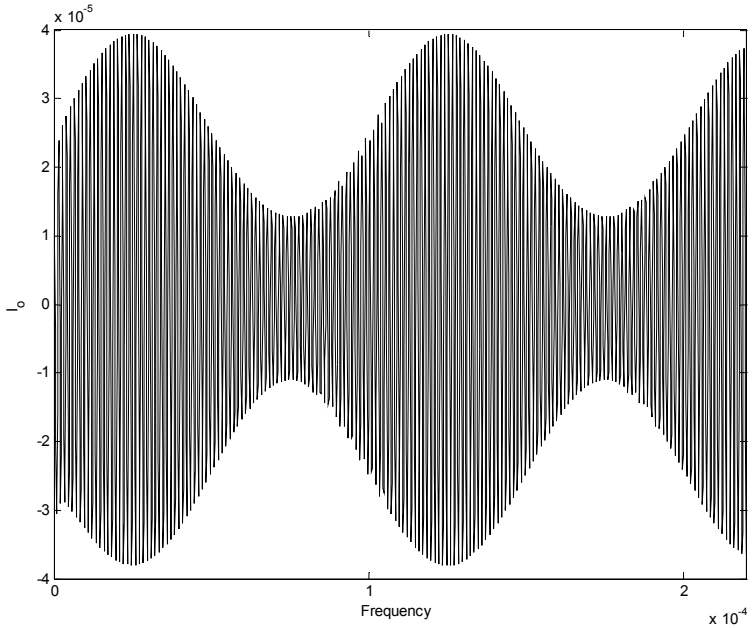



**Figure 4-42** Waveform of the full AM modulated signal

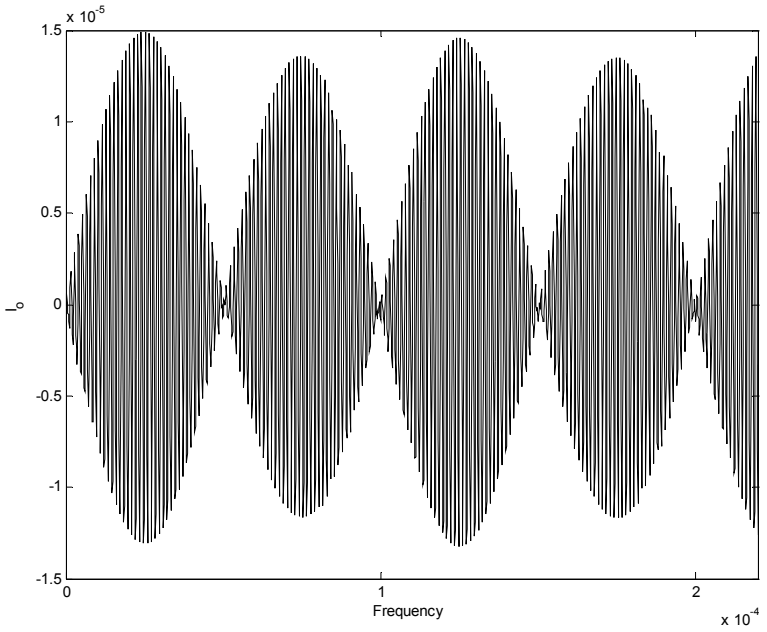



**Figure 4-43** Waveform of the suppressed carrier modulated signal

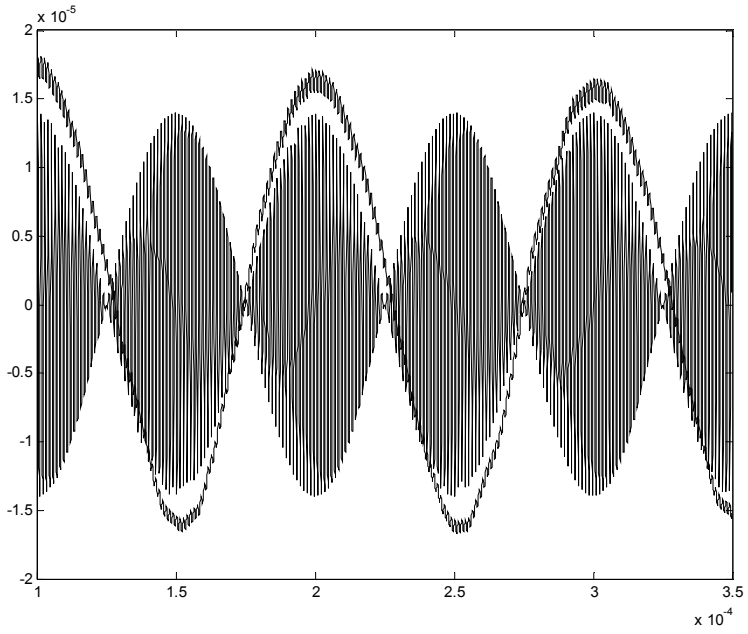



**Figure 4-44** Waveforms of both of the double sideband suppressed carrier modulated signal and the detected modulation signal after using low pass filter.

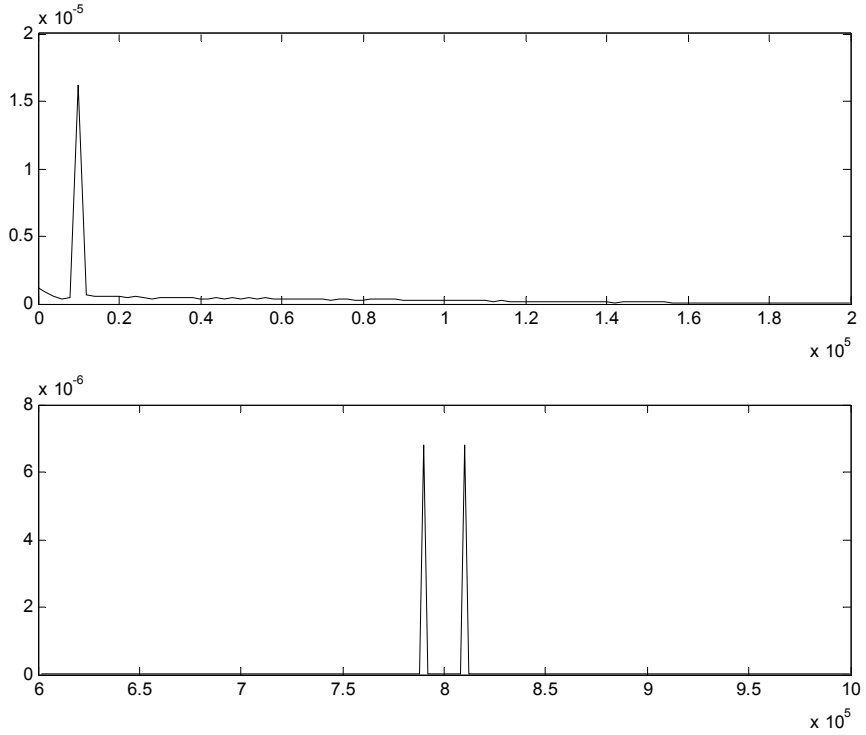



**Figure 4-45** The frequency spectrum of both a) the detected signal and b) the double sideband suppressed carrier signal.

## 4.4 Other Applications

Depending on the set of functions the CABs can perform, it is believed that having sufficient number of these blocks integrated on one chip allows the designer to carry out almost any analog task. As shown previously and using relatively small number of these CABs, maximum of four cascaded ones, implementation of two different configurations of second order universal filter, a power law function generator and an AM modulator/demodulator was feasible.

A number of other applications using these basic blocks can be implemented. For example, extending the universal filter into orders above two can be easily done by cascading several stages to it. Another very interesting field of applications of such CABs is in neural networks implementation. Using the proposed CABs, the implementation of functional artificial neural networks (FANN) becomes straightforward. Figure (4-46) shows the block diagram of a path from input to output in the FANN [122]. Building such a block diagram is very simple since only one CAB is needed and is configured as an exponential cell. Summers in current mode can simply be implemented as direct connection nodes.

These blocks can be easily configured and used also for nonlinear function synthesizer, for sinusoidal frequency division and for frequency multiplication.

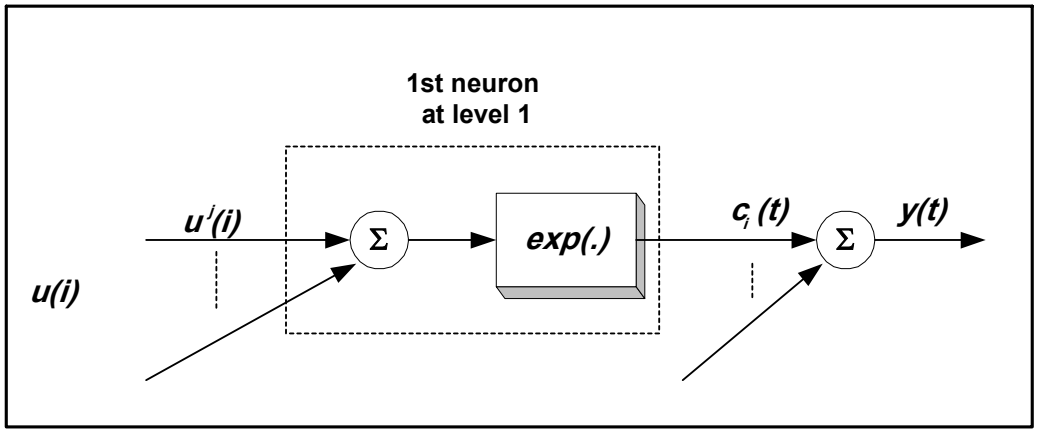



**Figure 4-46** Block diagram of one path from input to output in the FANN.

# CHAPTER 5

# Conclusion and Future Work

## 5.1 Conclusion

In this research, configurable analog blocks for field programmable analog arrays were developed. These CABs are capable of performing one of the following functions: Addition, Subtraction, Integration, Differentiation, Log and Anti-log. It is believed that using this small set of functions other functions and systems can be implemented. This set of functions is the same as the one adopted by the commercial TRAC FPAA. However, unlike the TRAC FPAA which uses op-amp based approach in realizing these functions, the continuous-time current-mode approach is chosen in this research. This choice is made mainly due to the many features this approach has over the other approaches. These features where discussed in section 2.1. The realization of these functions is presented in Chapter 3.

Add and Subtract functions are assumed to be straight forward since they can be implemented in current-mode using simple current mirrors and cross coupling. The

other four functions are realized using translinear circuits. The input signals, output signals and the tuning parameters are all realized using currents. Both the differentiator and integrator are fully differential circuits whereas the log and anti-log amplifiers are single-input differential-output.

In all circuits the output current is temperature dependent. This dependence can be compensated for in the case of the integrator and differentiator using temperature dependent biasing current sources. However, in the case of the log and anti-log functions it is not possible to use this compensation method. Fortunately, in many applications an equal number of cascaded log and anti-log functions are used resulting in overall temperature-independent characteristics.

As the proposed circuits are based on the translinear principle with BJTs in the active mode, one main factor affecting the accuracy and bandwidth of these circuits is the base currents. In order to partially solve this problem, BJTs with larger dc current gain can be used. However this may not be possible when using transistors with higher cutoff frequency. Another method to reduce the effect of these base currents is to use compensation current sources. This method was applied in this research and shown good enhancements.

In order to investigate the versatility of the adopted set of functions in realizing systems, three examples were discussed in Chapter four; a second order universal filter, a power factor generating circuit, and an AM modulator/demodulator system. The universal filter was realized using two different routing network topologies; the string-like and the matrix-like. From these two realizations, it has been shown that the

matrix-like topology gives designers more flexibility in dealing with the CABs and thus better characteristics. However, other applications can be implemented using either topology with the same degree of flexibility making it much simpler to use the string-like topology rather than the matrix like.

All proposed circuits and applications are simulated using Pspice software. All simulations where done assuming the practical parameters of the BFP640 Infineon$^{@}$ BJT transistor. In order to investigate the effect of the used transistor parameters on the characteristics, comparison with simulations assuming default parameters with same value of $\beta$ is done. All presented simulations showed good characteristic behaviors for all presented circuits.

The main enhancement achieved in this research over the CABs of the TRAC FPAA and the other CABs found either in the literature or in the market is in terms of both the frequency ranges and the power supply voltages. The maximum upper frequency achieved here was in the case of the low pass filter realization and it was around 100 MHz and the minimum was around 10 MHz in the case of the all pass filter. However, these circuits face problems when used for low frequency applications, the minimum possible frequency is 50 KHz for the BPF. One reason for this problem is the need for all capacitors to be on-chip. This implies serious limitations on the maximum possible value of these capacitors. It is assumed in all circuits that the capacitor value is 20 pF. Because the current-mode technique is used in all the designs, no high gain nodes exist in the circuits and thus Millar theorem can not be applied to enhance the effective value of the used capacitors. One possible solution to

this problem is to use biasing currents with smaller ranges. Although this will impose a reduction in the transistors cutoff frequency, this will not affect the results since we are assuming low frequency signals.

In order to investigate the effects of digital programming on the performance of the circuits, string-like universal filter proposed in Chapter four was fully digitally programmed. A CAD tool using Visual Basic programming language was developed to be used as a user interface.

All proposed analog CABs are assumed to operate using ±1.5 V power supply. However, these circuits, except the log-amplifier, can operate with supply voltage of ±1V without affecting the characteristics.

## 5.2 Future work

As a future extension to this work, a complete continuous-time current-mode FPAA can be designed. In order to reach this goal, more deep study of the up to date advances in the supplementary routing network, digital controlling part, and programmable current sources must be done. This is of critical importance especially with the new emerging Silicon-Germanium (SiGe) 50 GHz technology. According to IBM@ this new SiGe technology combines the integration and cost benefits of silicon with the speed of more esoteric and expensive technologies such as gallium-arsenide [123]. Germanium introduced into the base layer of an otherwise all-silicon bipolar transistor results in significant improvements in operating frequency, current, noise,

and power capabilities. At the same time, the key advantages of silicon process are maintained, including high integration level and economy of scale. Shortly, IBM will be releasing BiCMOS SiGe technology paving the way toward realizing complete mixed systems on a single chip.

# Appendix A: Realization of higher order Butterworth and Chebyshev low pass-filters

As discussed previously, Section 4-1, the implemented biquadratic filtering cell can be extended to realize higher order filters. In this appendix, the extension of these cells to realize higher order Butterworth and Chebyshev LPFs is presented [124].

The Butterworth filter function of order *n* is the function

$$T(s) = \frac{1}{B(s)} \tag{A-1}$$

with *n* left-half poles all on the unit circle. Although *B(s)* cannot be expressed in a simple closed form, its poles can easily be computed using the following formula

$$s = \begin{cases} 1e^{180^o m/n}, & m = 0, 1, 2, \ldots, 2n\text{-}1 \quad \text{for } n \text{ odd} \\ 1e^{\left(90^o + 180^o m\right)/n}, & m = 0, 1, 2, \ldots, 2n\text{-}1 \quad \text{for } n \text{ even} \end{cases} \tag{A-2}$$

From the roots of *B(s)* = 0 we can easily construct *B(s)*. A convenience in practical filter design is the general availability of tabulated results such as Table A-1. This table shows B(s) factored into first- and second-order polynomials. The first-order polynomial can directly be realized by a CAB configured as a lossy integrator, while

the second-order polynomial can be realized using two CABs connected as a biquadratic LPF as presented in Section 4-1. Cascading these stages together results in low pass Butterworth filters of the desired order.

The transfer function of a Chebyshev filter of order n takes the following form

$$T(s) = \frac{K}{s^n + a_{n-1}s^{n-1} + \cdots + a_o} \tag{A-3}$$

where $a_o$, …, $a_{n-1}$ are constants and $K = a_o$ for $n$ odd and $K = a_o / (1+\varepsilon^2)^{0.5}$ for $n$ even. $\varepsilon$ is the passband ripple. Table A-2 gives the denominator of T(s) in factor form of two different values of passband ripple. It is clear form this table that the same cascading configuration used to realize the Butterworth filters can be used to realize the Chebyshev filters. The only change needed to be done is the values of the biasing currents representing the multiplicative constants. This can be easily done by utilizing the programmable current sources discussed earlier.

Figures (A-1) and (A-2) represent simulation results compared to targets for the frequency response of a third order Butterworth and Chebyshev filters. Once again simulations are done assuming the practical parameters used through out the research. In order to investigate the effect of base currents on the performance of the filters, the simulations are also performed for the case with default Pspice transistor parameters but with $\beta = 1000$.

**Table A-1** Butterworth Filter Denominators

| **n** | **Factors of *B(s)*** |
|---|---|
| 1 | $( s + 1 )$ |
| 2 | $( s^2 + 1.4142\ s + 1)$ |
| 3 | $( s + 1 ) ( s^2 + s + 1)$ |
| 4 | $( s^2 + 0.7654\ s + 1) ( s^2 + 1.8478\ s + 1)$ |
| 5 | $( s + 1 ) ( s^2 + 0.6180\ s + 1) ( s^2 + 1.6180\ s + 1)$ |
| 6 | $( s^2 + 0.5176\ s + 1) ( s^2 + 1.4142\ s + 1) ( s^2 + 1.9318\ s + 1)$ |

**Table A-2** Chebyshev denominator factors for 0.5 and 3.0 dB ripple

| **Passband Ripple Value (dB)** | ***n*** | **Factors** |
|---|---|---|
| **0.5** | 1 | ( $s$ + 2.863 ) |
| | 2 | ( $s^2$ + 1.426 $s$ + 1.5164) |
| | 3 | ( $s$ + 0.626 ) ( $s^2$ + 0.626 $s$ + 1.142453) |
| | 4 | ( $s^2$ + 0.35 $s$ + 1.062881) ( $s^2$ + 0.846 $s$ + 0.35617) |
| | 5 | ( $s$ + 0.326 ) ( $s^2$ + 0.224 $s$ + 0.012665) ( $s^2$ + 0.568 $s$ + 0.476474) |
| | 6 | ( $s^2$ +0.156$s$+1.022148) ($s^2$ +0.424$s$+0.589588) ($s^2$+0.58 $s$ +0.157) |
| **3.0** | 1 | ( $s$ + 1.002 ) |
| | 2 | ( $s^2$ + 0.2986 $s$ + 0.83950649) |
| | 3 | ( $s$ + 0.299 ) ( $s^2$ + 0.2986 $s$ + 0.8395649) |
| | 4 | ( $s^2$ + 0.17 $s$ + 0.902141) ( $s^2$ + 0.412 $s$ + 0.1961) |
| | 5 | ( $s$ + 0.177 ) ( $s^2$ + 0.11 $s$ + 0.936181) ( $s^2$ + 0.288 $s$ + 0.377145) |
| | 6 | ($s^2$+0.076 $s$+0.95402) ($s^2$+0.208 $s$ +0.522041) ($s^2$+0.286$s$+0.0891) |

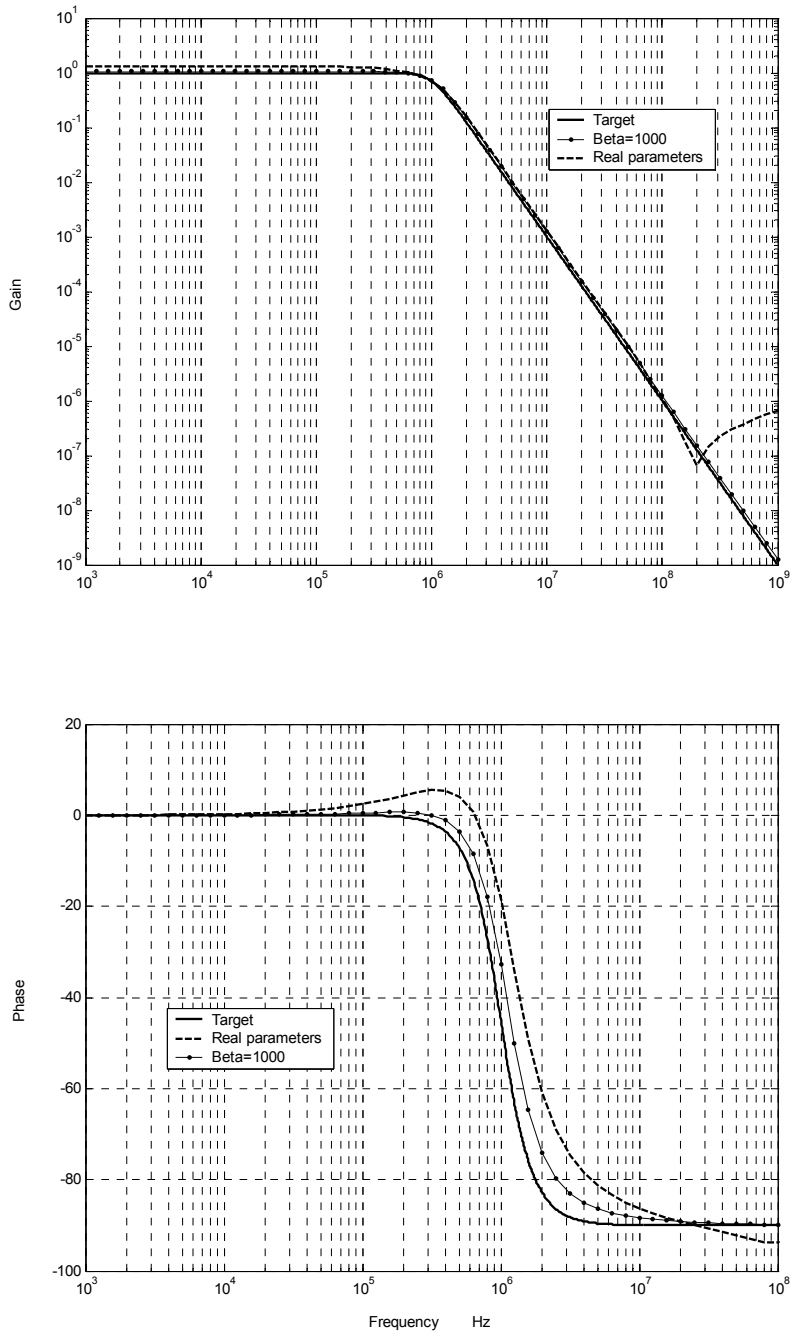



**Figure A-1** Gain- and Phase-Frequency response of third order Butterworth LPF.

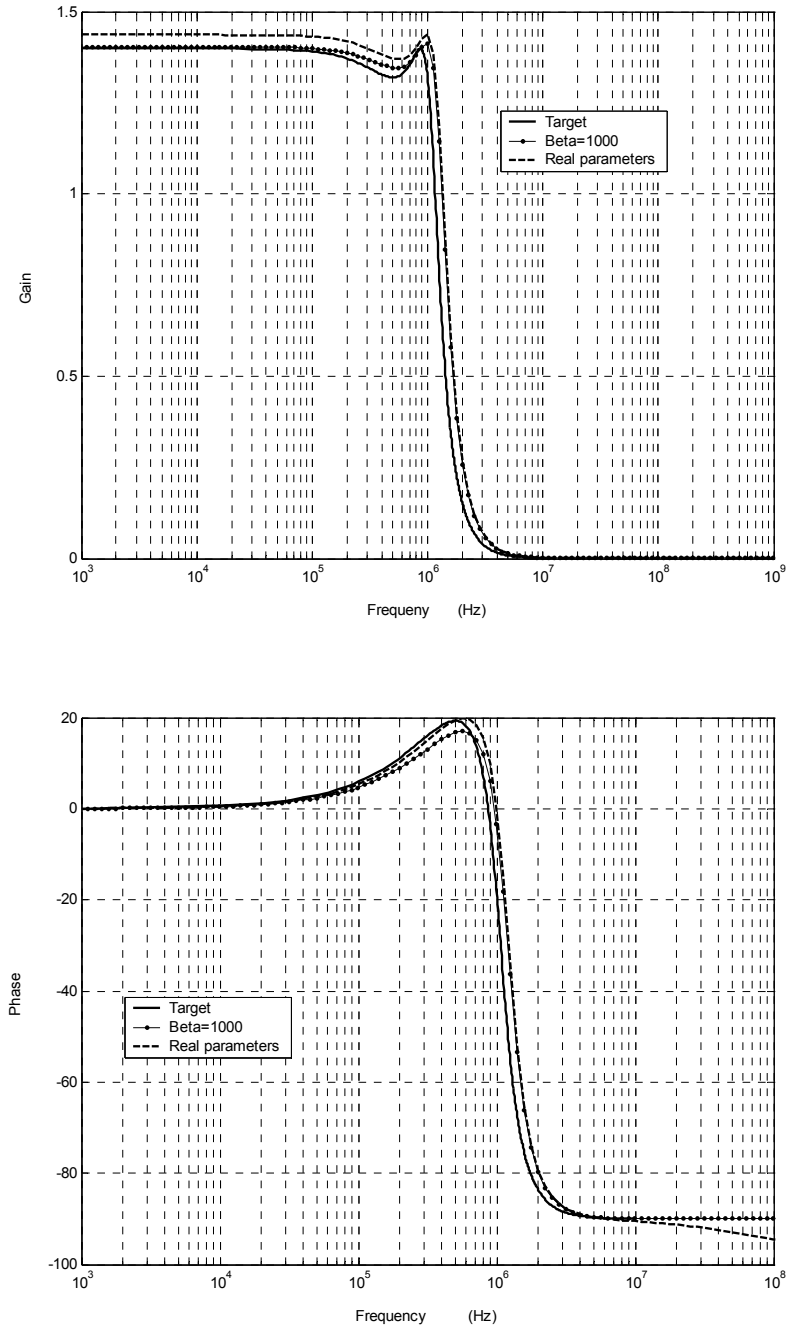



**Figure A-2** Gain- and Phase-Frequency response of third order Chebyshev LPF. 0.5 dB ripple is assumed.

# Appendix B: Temperature compensation techniques for Log and Anti-log functions

Figures (B-1) and (B-2) show techniques used to compensate for the temperature variations in both the log and anti-log functions respectively. In Figure (B-1), the current divider cell is assumed to be built using the log and anti-log resources available at the FPAA. Depending on this figure, the output current will be

$$I_o = I_c \frac{I_{o1}}{I_t} \tag{B-1}$$

where $I_c$ is a scaling DC current. Noting that both $I_{o1}$ and $I_t$ are the outputs of a log function, we can write equation (B-1) as

$$I_o = I_c \frac{\frac{R}{V_T}\ln\left[\frac{I_{in}}{I_{ref1}}\right]}{\frac{R}{V_T}\ln\left[\frac{I_{DC}}{I_{ref2}}\right]} = \frac{Ic}{\ln\left[\frac{I_{DC}}{I_{ref2}}\right]}\ln\left[\frac{I_{in}}{I_{ref1}}\right] \tag{B-2}$$

Equation (B-2) shows that the resulting output current is now temperature independent.

Similarly, Figure (B-2) shows a possible method that can be used to compensate for the temperature variations in the anti-log function. Once again, the current multiplier is assumed to be built using the log and anti-log resources on the FPAA. The output current can be written as

$$I_o = \frac{I_A}{I_R}\left(I_{y1} - I_{x1}\right)\exp\left[\frac{V_T}{R}\frac{\frac{R}{V_T}\ln\left(\frac{I_{DC}}{I_{ref\,2}}\right)}{Ic}I_{in}\right] \tag{B-3}$$

This equation can be simplified to

$$I_o = \frac{I_A}{I_R}\left(I_{y1} - I_{x1}\right)\exp\left[\frac{\ln\left(\frac{I_{DC}}{I_{ref\,2}}\right)}{Ic}I_{in}\right] \tag{B-4}$$

which results in a temperature-independent output current.

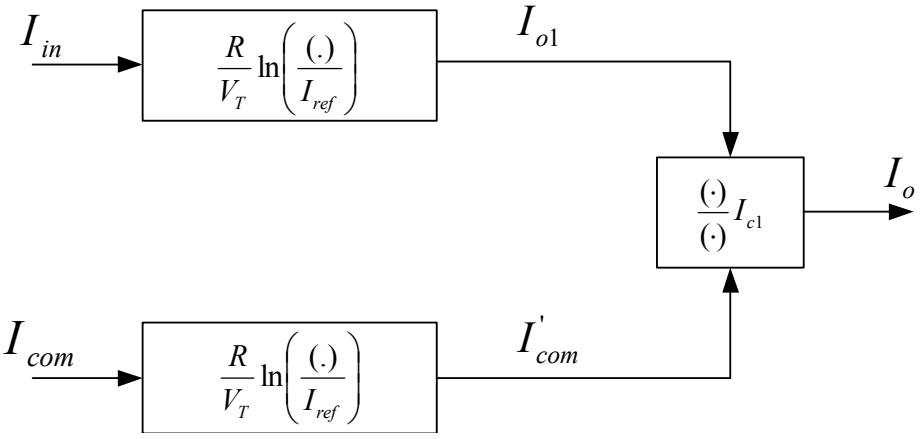



**Figure B-1** Block diagram of the technique used to compensate for temperature variations effects on the output of the log-function.

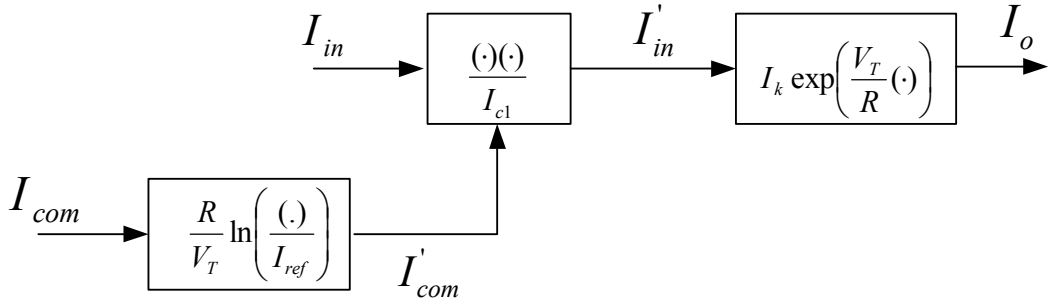



**Figure B-2** Block diagram of the technique used to compensate for temperature variations effects on the output of the anti-log function.

# Nomenclature

**A/D:** Analog to Digital converter.

**AM:** Amplitude Modulation.

**Anti-log:** Anti-logarithm function.

**ASP:** Analog Signal Processing.

**AUX:** Auxiliary.

***β*:** BJT's forward DC current gain.

**BiCMOS:** Bipolar-Complementary Metal-Oxide Semiconductor.

**BJT:** Bipolar Junction Transistor.

**BPF:** Band Pass Filter.

**C:** Capacitor.

**CAB:** Configurable Analog Block.

**CAC:** Configurable Analog Cell.

**CAD:** Computer Aided Design.

**CCII:** Second Generation Current Conveyor.

**CMOS:** Complementary Metal-Oxide Semiconductor.

**D/A:** Digital to Analog converter.

**DC:** Direct Current.

**DSP:** Digital Signal Processing.

$f_T$**:** Transistor Cutoff frequency.

$f_{ug}$**:** Unity-gain bandwidth.

**FANN:** Functional Artificial Neural Network.

**FPAA:** Field Programmable Analog Array.

**FPGA:** Field Programmable Gate Array.

**FPMA:** Field Programmable Mixed Array.

**HPF:** High Pass Filter.

**IC:** Integrated Circuit.

**IDE:** Integrated Design Environment.

**IPmodule:** Intellectual Property Module.

**ITS:** Intelligent Transport System.

**K:** Boltzmann constant.

**KCL:** Kirchhoff's Current Law.

**KVL:** Kirchhoff's Voltage Law.

**ln:** Natural logarithmic function.

**log:** Logarithm.

**LPF:** Low Pass Filter.

**M2M:** Metal to Metal.

**MOSFET:** Metal-Oxide Semiconductor Field-Effect Transistor.

**MUX:** Multiplexer.

**Op-Amp:** Operational Amplifier.

**OTA:** Operational Transconductance Amplifier.

**PC:** Personal Computer.

**PL:** Programming Logic.

**PLD:** Programming Logic Device.

**PR:** Programming Register.

***q*:** Electron charge.

**Q:** Bipolar Junction Transistor.

**R:** Resistor.

**S/C:** Switched Capacitor.

**S/I:** Switched Current.

**SiGe:** Silicon Germanium.

**SoC:** System on Chip.

**T:** Temperature in kelvin.

**TL:** Translinear Loop.

**TLP:** TransLinear Principle.

**VLSI:** Very Large Scale Integrated circuits.

$w_o$**:** Cutoff frequency in radian/sec.

$w_c$**:** Center frequency in radian/sec.

**W-CDMA:** Wide-band Code Division Multiple Access.

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