The Translinear Current Controlled Conveyor and its Applications

by

Noman Ali Tassaduq

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

In

ELECTRICAL ENGINEERING

May, 1998

INFORMATION TO USERS

This manuscript has been reproduced from the microfilm master. UMI films the text directly from the original or copy submitted. Thus, some thesis and dissertation copies are in typewriter face, while others may be from any type of computer printer.

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleedthrough, substandard margins, and improper alignment can adversely affect reproduction.

In the unlikely event that the author did not send UMI a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

Oversize materials (e.g., maps, drawings, charts) are reproduced by sectioning the original, beginning at the upper left-hand corner and continuing from left to right in equal sections with small overlaps. Each original is also photographed in one exposure and is included in reduced form at the back of the book.

Photographs included in the original manuscript have been reproduced xerographically in this copy. Higher quality 6" x 9" black and white photographic prints are available for any photographs or illustrations appearing in this copy for an additional charge. Contact UMI directly to order.

UMI

A Bell & Howell Information Company
300 North Zeeb Road, Ann Arbor MI 48106-1346 USA
313/761-4700 800/521-0600

THE TRANSLINEAR CURRENT CONTROLLED CONVEYOR AND ITS APPLICATIONS

BY

NOMAN ALI TASADDUQ

A Thesis Presented to the

FACULTY OF THE COLLEGE OF GRADUATE STUDIES

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS

DHAHRAN, SAUDI ARABIA

In Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

In

ELECTRICAL ENGINEERING

MAY 1998

UMI
300 North Zeeb Road
Ann Arbor, MI 48103

THE TRANSLINEAR CURRENT CONTROLLED CONVEYOR AND ITS APPLICATIONS

NOMAN ALI TASADDUQ

ELECTRICAL ENGINEERING

MAY 1998

KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS

DHAHRAN, SAUDI ARABIA

This thesis, written by

Noman Ali Tasadduq

under the direction of his thesis advisor, and approved by his thesis committee, has been presented to and accepted by the Dean, College of Graduate Studies, in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

Thesis Committee:

Chairman (Prof. M. T. Abuelma'atti)

Member (Dr. M. A. Al-Sunaidi)

Member (Dr. Chedly B. Yahya)

Member (Dr. Z. J. Al-Saati)

Dr. Samir A. Al-Baiyat
Department Chairman

Dr. Abdallah M. Al-Shehri
Dean, College of Graduate Studies

Date: 2016198

Acknowledgments

Praise be to the Lord of the World, the Almighty for having guided me at every stage of my life.

I am grateful to my thesis advisor Prof. M. T. Abuelma'atti for his continuous support and guidance throughout the work. I would also like to place on record my appreciation for the cooperation and guidance extended by my committee members, Dr. Z. J. Al-Saati, Dr. Chedly B. Yahya and Dr. M. A. Al-Sunaidi.

My thanks to the department chairman Dr. Samir A. Al-Baiyat for providing me every help and facility to carry out this research. I am grateful to all my friends, both from within and outside the department, who made my stay at KFUPM a pleasant and memorable one.

I recall with deep gratitude and respect the debt I owe to my mother, uncle Mr. Sirajuddin and brothers Imran and Rizwan for their unfathomable love, prays, support and encouragement throughout my studies. May Allah bless them and may they live long for me.

Contents

List of Figures

Abstract

Name: Noman Ali Tasadduq

Title: Current Controlled Conveyor and its Applications

Major Field: Electrical Engineering

Date of Degree: May 1998

The thesis discusses the use of current controlled conveyor in applications like filters, oscillator and impedance simulation. Parasitic resistance R_x of current conveyor is used to advantage for realizing programmable and resistorless circuits. Universal filters, sinusoidal oscillator, higher order filters and impedance simulation circuits are designed with minimum number of active and passive components and grounded capacitors. These circuits enjoy independent control of circuit parameters and low active and passive sensitivities. The proposed circuits are compared with the previously published work. Simulation results confirming the theoretical designs are included.

Master of Science Degree

King Fahd University of Petroleum and Minerals

Dhahran, Saudi Arabia

May, 1998

خلاصة الرسالة

الإسم : **نعمان عـــلي تـصدق**

عنوان الرسالة : **ناقـل التيار المـبرمـج وتـطبيقـاتـه**

التخصص : **الهـندسـة كـهربـائـية**

تاريخ الشهادة : **صفر ١٤١٩هـ**

تناقش هذه الرسالة تطبيقات ناقل التيار المبرمج في دوائر المرشحات ومولـدات الذبذبـات وكذلك الدوائر التمثيلية للمعانقة. وفي هذا الإطار تستخدم المقاومة الداخلية لناقل التيار (Rx) في تحقيق دوائر مبرمجة بدون استخدام مقاومات خارجية. وقد تم استنباط دوائر مرشـحات ، ومولد ذبذبات، مرشحات ذات درجة عالية وكذلك دوائر تمثيل الممانعة باسـتخدام الحـد الأدنى من المكونات وكذلك باستخدام مكثفات متصلة بالأرض. وكل هذه الدوائر تتمتـع بخاصية هامة وهي إمكانية التحكم المستقل في خصائصها وكذلك الحساسية القليلة للتغـيرات في مكونات الدوائر. وفي كل الحالات عقدت المقارنة بين الدوائر المقترحة والمستنبطة والدوائر المماثلة التي سبق نشرها. وكذلك استخدمت برامج الحاسب الآلي لتمثيـل هـذه الدوائـر واختبارها.

درجة الماجستير في العلوم

جامعة الملك فهد للبترول والمعادن

الظهران ـ المملكة العربية السعودية

صفر ١٤١٩هـ

Chapter 1

INTRODUCTION

Current mode signal processing circuit techniques are receiving considerable attention, because of their advantages in terms of speed, bandwidth and accuracy over the voltage mode circuits. Circuits are classified as current mode if the signals being processed are represented by time varying currents. Certain applications benefit from operating in the current mode domain rather than in the voltage mode [1]: for example in a predominantly capacitive environment, speed is maximized by driving currents rather than voltages. Basic operations like for example addition, subtraction or multiplication are easier to perform using currents instead of voltages. In addition current-mode functions exhibit simpler architectures and lower supply voltage capabilities than their voltage-mode counterparts. As a result numerous papers have been published reporting new and novel current mode circuits, common examples are amplifiers, filters, oscillators and rectifiers [2].

The theoretical basis of many of the current mode circuits dates back many years but it is only with developments in truly complementary bipolar technology that these devices can be realized. At present, a number of current mode circuit

techniques, such as current conveyors (CCs) [3][4], operational transconductance amplifiers (OTAs) [5]-[7] and switched current (SI) [8] have been developed. In these techniques the current conveyors have proved to be functionally flexible and versatile, rapidly gaining acceptance as a practical device with a wide range of high performance circuit and system applications. A host of circuits have been suggested on synthesis of various circuit elements using current conveyors [9].

1.1 Current Conveyor

Due to the growing role of current mode analog signal processing the current conveyors have become important building blocks in many applications. Current conveyors are a combination of voltage and current-mode devices offering low component count and high bandwidth. Unlike operational amplifiers, current conveyors do not have their bandwidth restricted by feedback. They can work over 100MHz bandwidth and remain stable with both inductive and capacitive loads.

Current conveyor was first introduced by Smith and Sedra in 1968 [10], as first generation current conveyor (CCI). In 1970 they introduced another type as second generation current conveyor (CCII) [11]. A third generation current conveyor (CCIII) was later introduced by Fabre in 1995 [12].

Current conveyor is normally a three terminal device with terminals marked as X, Y and Z. The input/output characteristics of the three types of conveyors can

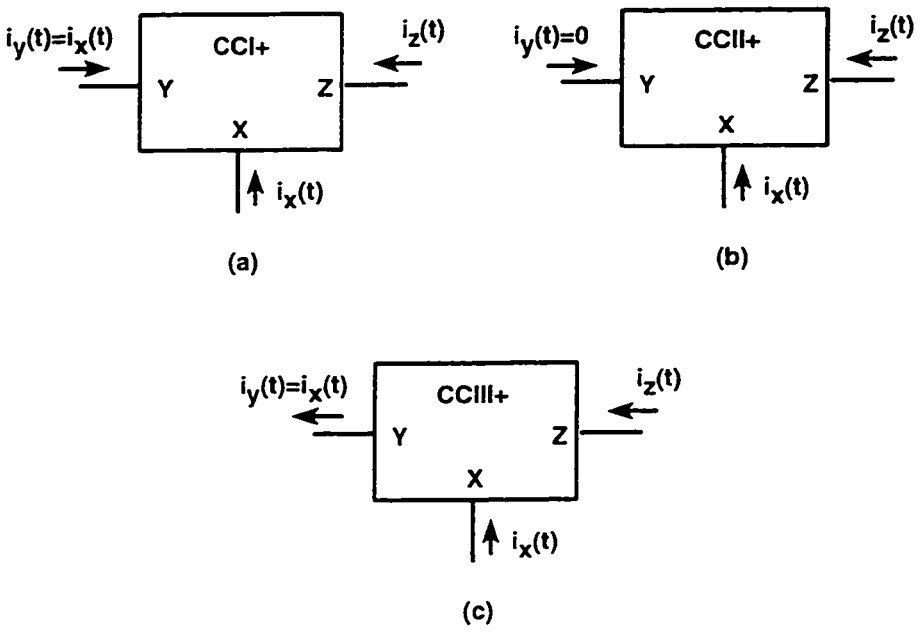


Figure 1.1: (a) Symbol of first generation current conveyor. (b) Symbol of second generation current conveyor. (c) Symbol of third generation current conveyor.

be represented in the form of a matrix as follows:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & b & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{1.1}$$

A first generation current conveyor (CCI) results if a=1, while a second generation current conveyor (CCII) results if $a = 0$. For $a = -1$, the third generation current conveyor (CCIII) is obtained. Usually, $b = \pm 1$. The sign of b parameter determines the conveyor current transfer polarity ($i_x \rightarrow i_z$). By convention, positive is taken to mean i_x and i_z both flowing simultaneously towards or away from the conveyor. Block representation of the three types of conveyors is shown in Figure 1.1. The operation of the first generation current conveyor is such that if a voltage is applied to terminal Y, an equal amount of voltage will appear on the terminal X. In the

same way, an input current i_x being forced into terminal X will result in an equal amount of current into terminal Y. The current supplied to X is also conveyed to output terminal Z with either positive or negative polarity. Terminal Z has the characteristics of a current source, with high output impedance.

To increase the versatility of the current conveyor a high impedance node is introduced in second generation current conveyor. No current flows in terminal Y and it exhibits an infinite impedance. The voltage at X follows that applied to Y. The current supplied to X is conveyed to the high impedance output terminal Z where it is supplied with either positive or negative polarity.

The operation of a third generation current conveyor is similar to the first generation except that the current through terminal Y is in opposite direction to terminal X.

The second generation current conveyor, because of its versatility has proven to be more useful than CCI. They have led to a great number of applications in the various designs of analog electronics, like amplifiers, filters or more generally signal processing circuits [1]-[3][9].

1.2 Monolithic Implementation of Current Conveyors

Since the introduction of current conveyors, several configurations have been introduced to implement these conveyors [1][9]. Two types are suitable for monolithic implementation. One is based on the operational amplifier (OA) power supply current sensing technique and the other is based on the translinear cell. These are

discussed below.

1.2.1 Power Supply Current Sensing Technique

In the earlier design of current conveyors voltage mode operational amplifiers were used for realizing a current conveyor. They suffered from the disadvantage of large number of operational amplifiers, use of matched resistances and low bandwidth [13]. Operational transconductance amplifiers have also been used but again were limited by poor bandwidth and poor output capability [14]. In an effort to minimize the disadvantages of using operational amplifiers as building blocks for current conveyors, a series of circuits and applications [15]-[20] were proposed. These circuits sensed the output stage current in an operational amplifier and produced a current conveyor function with appropriately connected current mirrors. The technique makes use of the fact that the current flowing from the output of the operational amplifier must be drawn through the supply leads. Current mirrors are thus used to sense the phase split output current via the operational amplifiers' supply leads. The current mirror outputs are then recombined to provide the required single high impedance bipolar output.

A CCII+ implementation using supply current sensing technique proposed by Wilson [16] is shown in Figure 1.2. Input Y draws only the bias current and acts as a high impedance input, whereas input X reflects the voltage at Y. As shown in Figure 1.3 a CCII- can be realized by simply adding a second pair of mirrors that are crosscoupled to produce a phase inversion between input and output current.

Although there had been attempts to improve the performance of supply current sensing techniques [16][20], however there are disadvantages which result from the

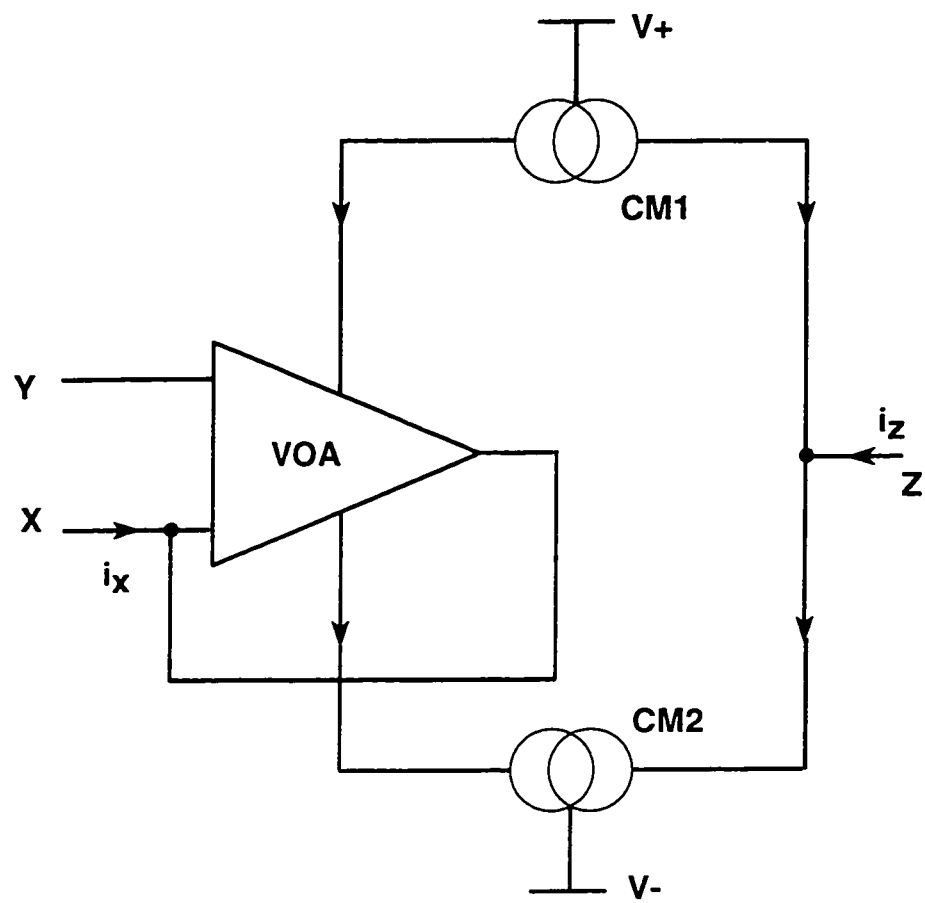


Figure 1.2: Schematic of VOA based CCII+

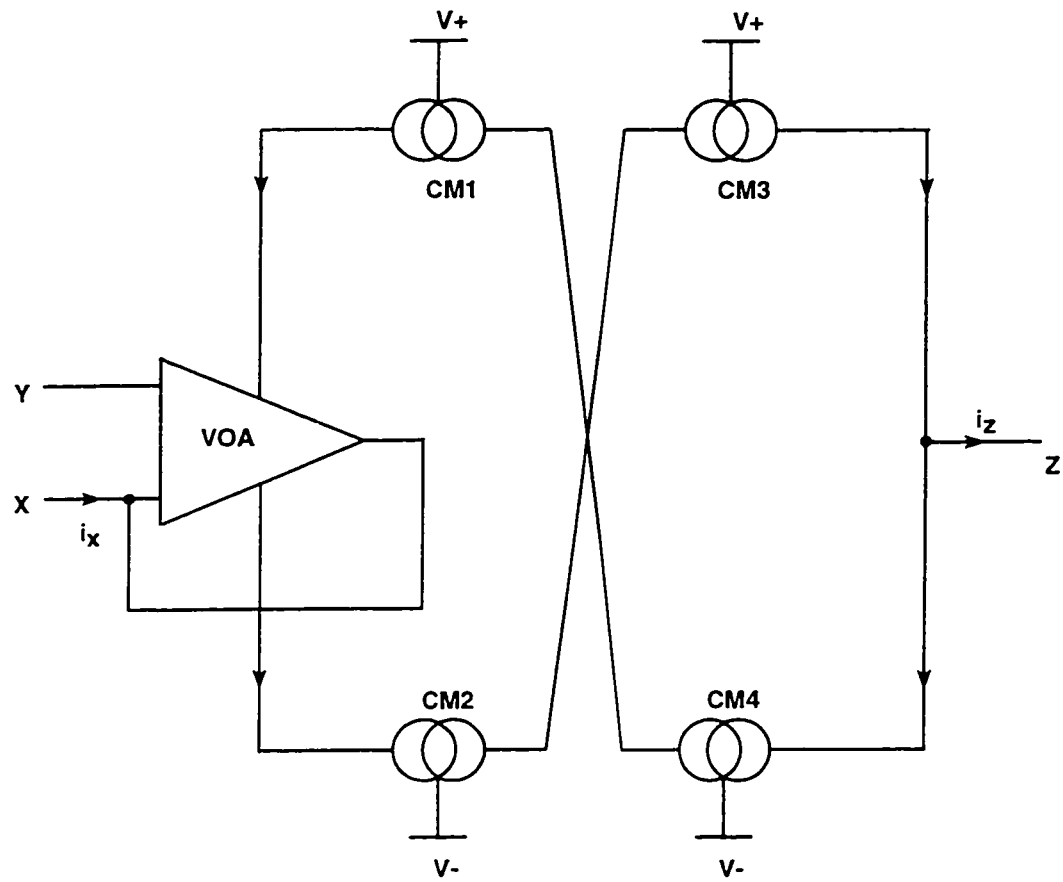


Figure 1.3: Schematic of VOA based CCII-.

presence of operational amplifier. These are listed below:

- low bandwidth (a few MHz to tens of MHz).
- large number of active and passive components necessary for the design of operational amplifier.
- increase of the power dissipation due to the operational amplifier.
- indirect monitoring of the output current introduces errors due to the bias component of the supply current.

1.2.2 Translinear Cell

As discussed in section 1.2.1, the use of operational amplifier limits the performance of the circuits in terms of frequency and power dissipation. There had been attempts to design circuits that did not require operational amplifier. One of the major achievement in this regard is the implementation of the input cell with a mixed translinear loop composed of complementary bipolar transistors instead of an operational amplifier. Translinear implementation allows the design of high performance circuits that exhibit extended bandwidth [21]-[23].

The translinear principle [24] can be applied to the loops containing n base-emitter junctions of PNP bipolar transistors and n junctions of NPN bipolar transistors. There is an elegant circuit arrangement known as mixed translinear cell (or simply translinear cell) conceived by Gilbert [23]. As shown in Figure 1.4, it uses a set of transistors arranged in a ring. This topology shows a strong resemblance to a pair of back-to-back two transistor mirrors. Because of its high performance it is

commonly used as the input stage of many high performance analog functions including transimpedance amplifiers [25], current controlled current sources [26]-[30], current conveyors [31]-[33]and impedance convertors [34][35]. Assuming that the following translinear conditions are satisfied [27],

- the current gain $\beta \gg 1$.
- $V_{BE} > 4V_T$ ($V_T = kT/q$ is the thermal voltage).
- all the junctions are at the same temperature.
- the emitter areas of the NPN transistors are the same and those of PNP transistors are the same.

then the translinear principle produces the current balance,

$$I_1 I_3 = I_2 I_4 \tag{1.2}$$

Many different circuit functions may be achieved by a suitable choice of currents. For example, when I_1, I_2 and I_3 are actively driven from input circuits then the output I_4 will be equal to $I_1 I_3 / I_2$, providing the opportunity for multiplication (I_2 held constant), division (I_3 held constant) and squaring ($I_1 = I_3 = I_i$ and I_2 held constant).

A current conveyor based on Gilbert translinear cell was proposed by both Fabre [32] and Normand [31] independently and is shown in Figure 1.5. In this circuit the translinear current equation and mirror arrangements force the current out of Z to be equal to the current out of X, while the voltage at X will faithfully track Y: exactly the properties of a CCII+ current conveyor. This conveyor is characterized by an improved frequency response for the voltage transfer from port Y to port X

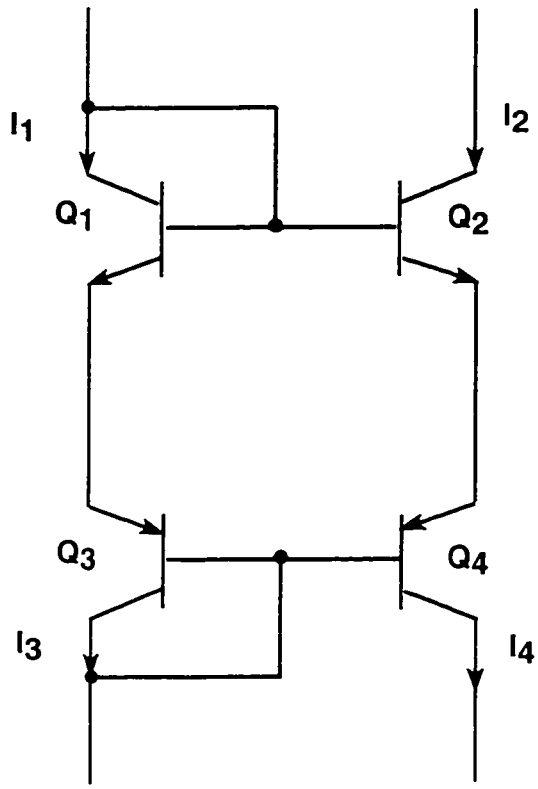


Figure 1.4: Circuit diagram of translinear cell.

[22] and needs a few number of active and passive components. Hence it requires less silicon area for implementation.

To introduce multiple outputs a pair of mirrors can be connected in parallel as shown in Figure 1.6. In order to realize CCII- cross coupled mirrors can be connected as shown in Figure 1.7.

Implementation of CCI+ is shown in Figure 1.8. Multiple outputs or negative output are easily realizable. Although there is no monolithic implementation for CCIII, it can be implemented by using multiple output CCII [12].

1.3 Effect of Internal Resistance in Current Conveyors (CCII)

The disadvantage associated with the topologies involving translinear cell as the input stage is that they have non-negligible parasitic resistance on port X (around 140Ω, for a bias current equal to $100\mu A$) which leads to errors when a load is connected at port X. Moreover, this may lead to instability if a capacitive load is connected at port X.

In the following section the effect of internal resistance in current conveyor circuits will be highlighted.

1.3.1 Multiple input single output (MISO) based circuit

Consider the circuit shown in Figure 1.9. It is a multiple input single output current mode circuit. It uses three current conveyors for filter realization. Routine analysis of the circuit assuming ideal current conveyor ($v_x = v_y$, $i_z = i_x$) gives the following

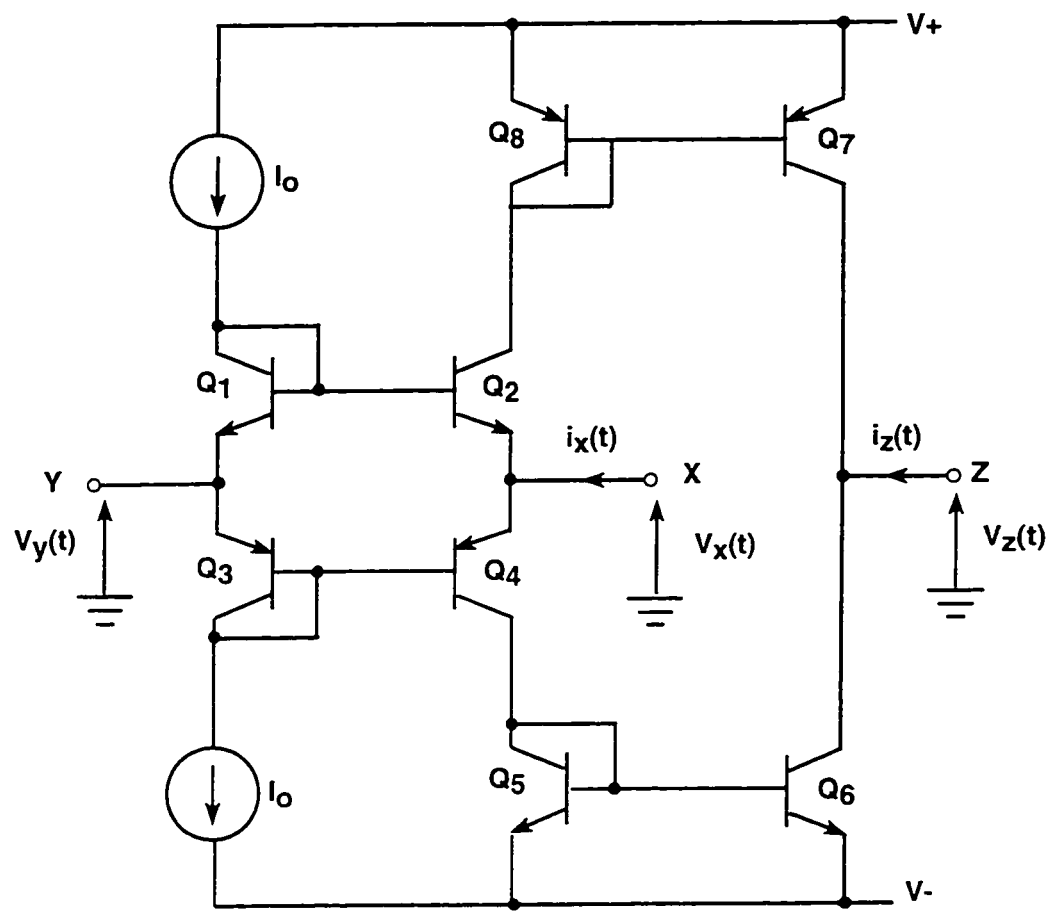


Figure 1.5: Translinear Cell based CCII+.

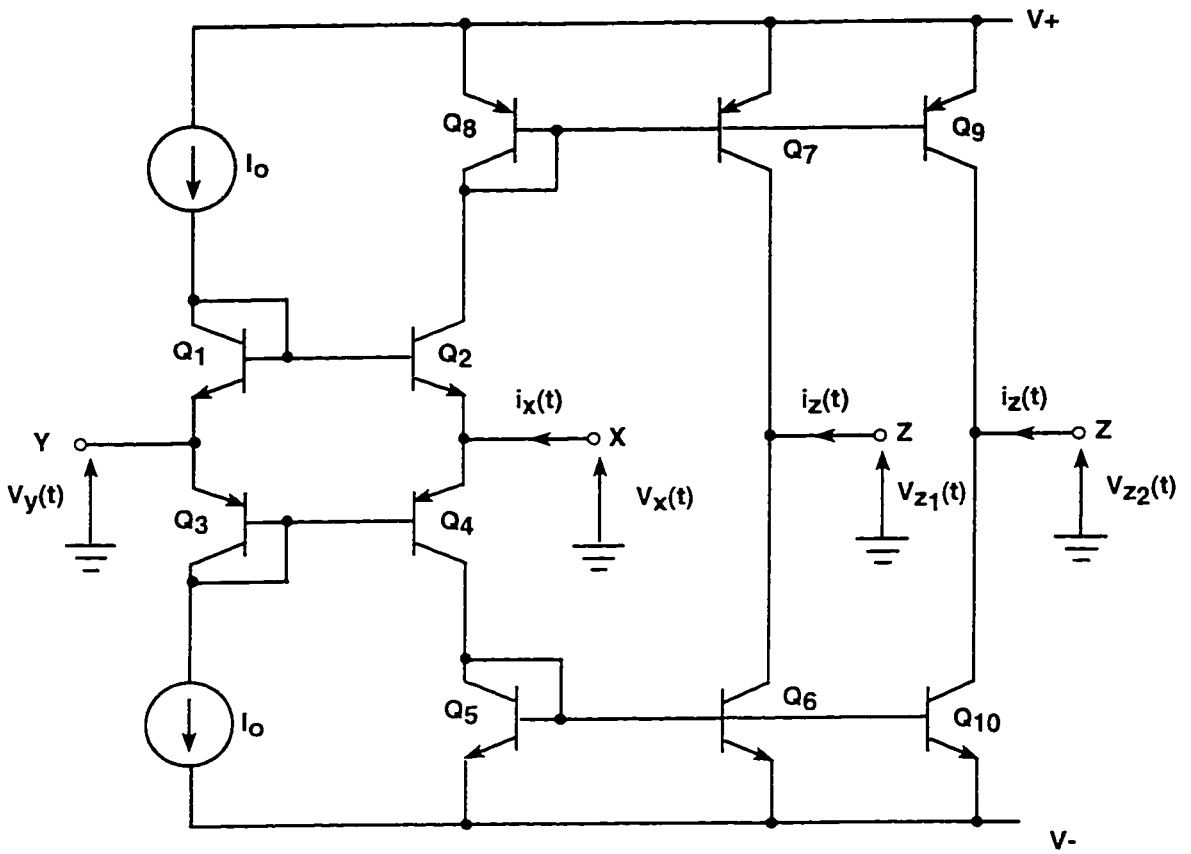


Figure 1.6: Multiple Output Translinear Cell based CCII+.

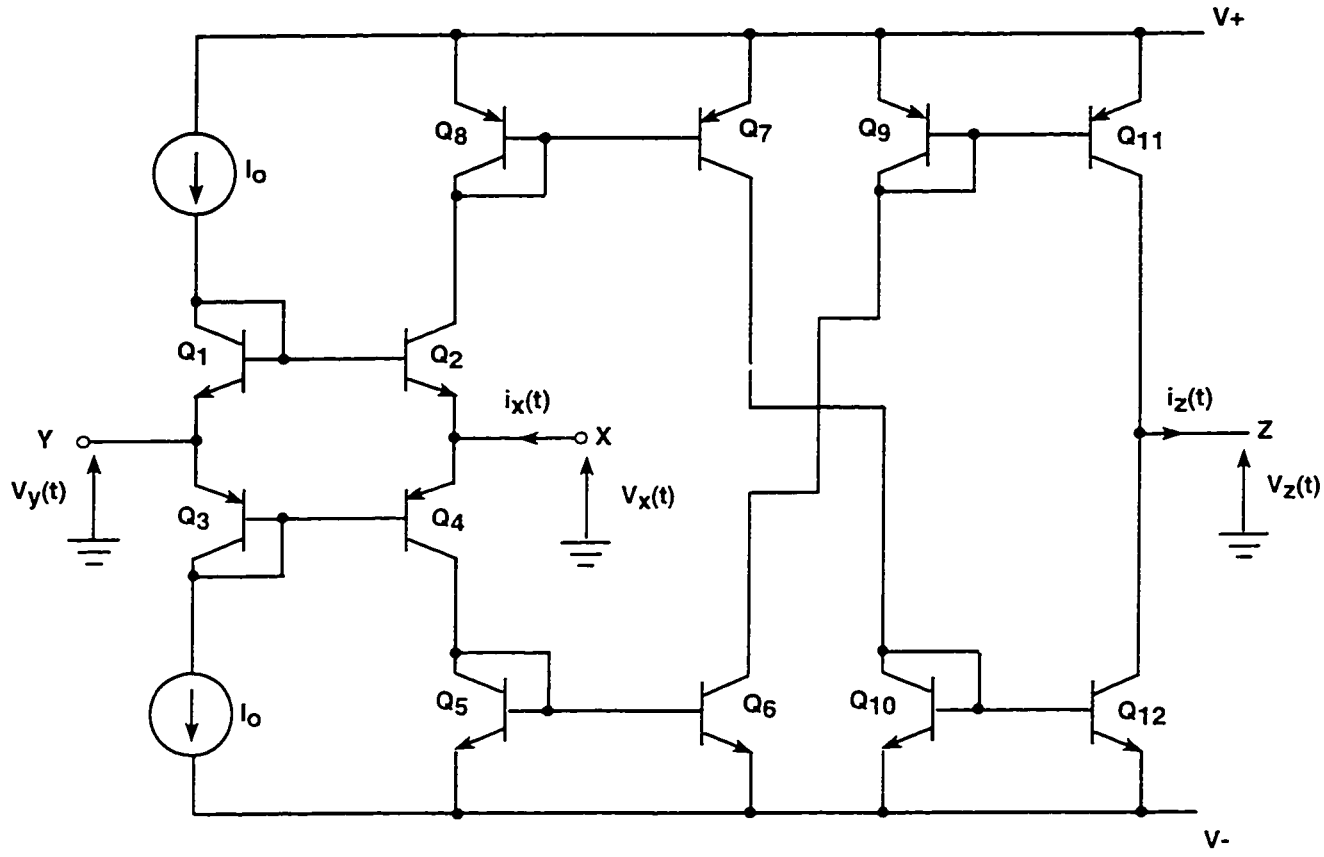


Figure 1.7: Translinear Cell based CCII-.

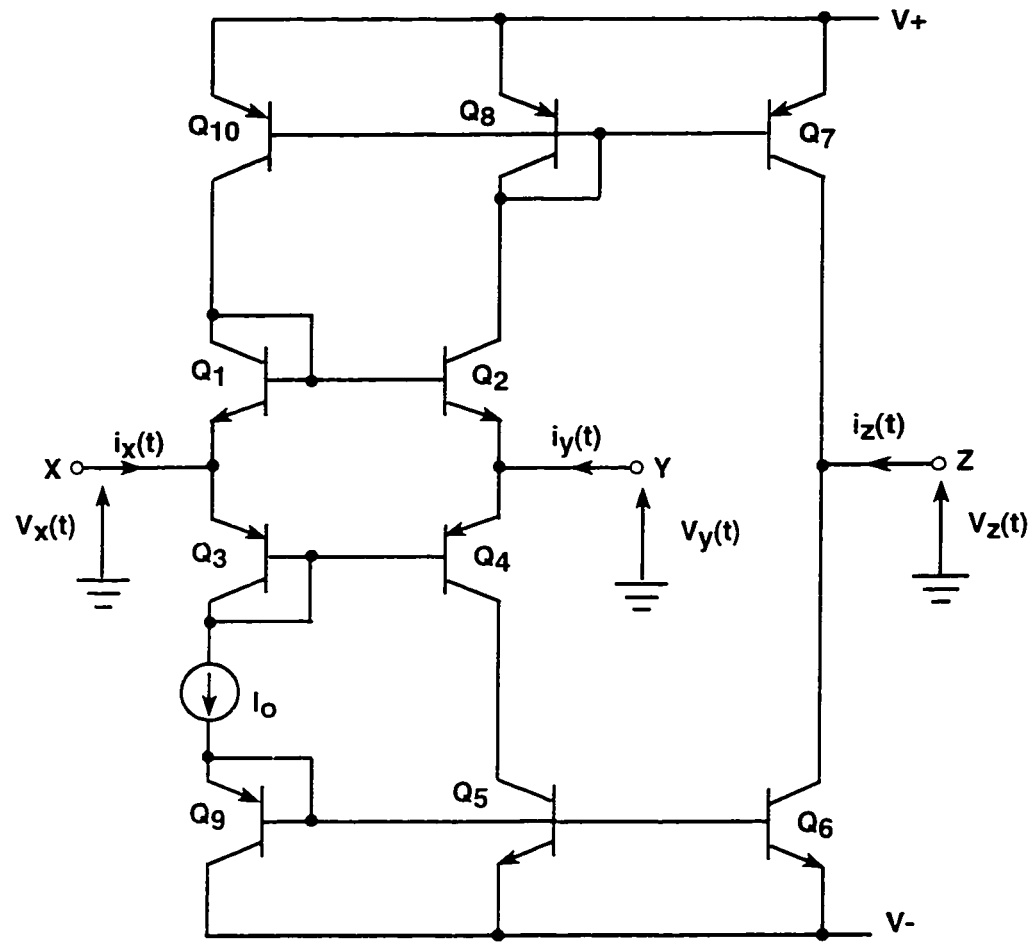


Figure 1.8: Circuit diagram of CCI+.

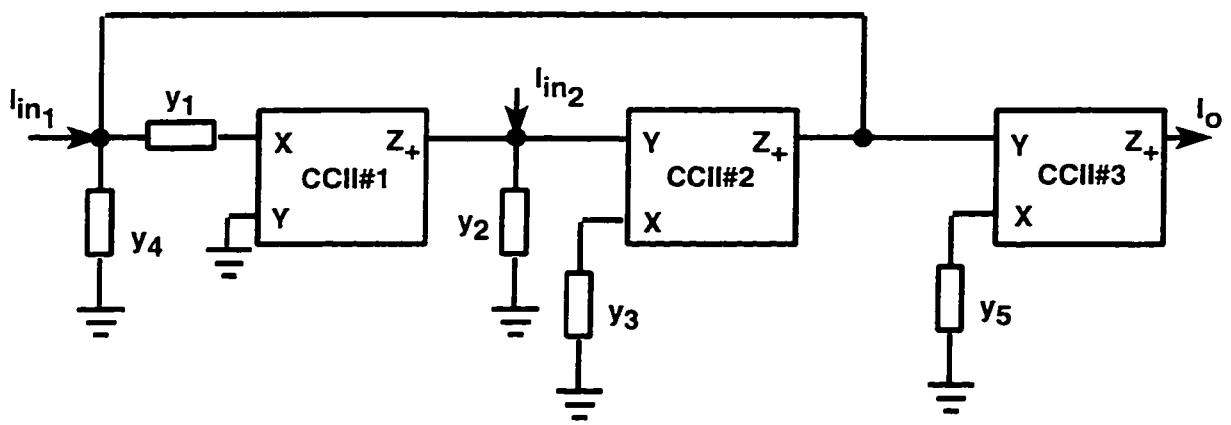


Figure 1.9: Multiple input single output CCII+ based filter

current transfer function.

$$I_o = -\frac{y_2 y_5 Iin_1 + y_3 y_5 Iin_2}{y_1 y_2 + y_1 y_3 + y_2 y_4} \tag{1.3}$$

For $I_{in_2} = 0$ and $y_2 = sC_2, y_4 = sC_4, y_1 = G_1, y_3 = G_3, y_5 = G_5$, a bandpass filter is realized, with the transfer function.

$$\frac{I_o}{I_{in_1}} = -\frac{G_5 C_2 s}{C_1 C_2 s^2 + G_1 C_2 s + G_1 G_3} \tag{1.4}$$

Similarly, for I_{in_1}=0 and other components remaining the same we obtain a lowpass filter with transfer function.

$$\frac{I_o}{I_{in_2}} = -\frac{G_3 G_5}{C_1 C_2 s^2 + G_1 C_2 s + G_1 G_3} \tag{1.5}$$

Similarly, by having $I_{in_2} = 0$, $y_5 = sC_5$ and other components remaining the same, we obtain a highpass function.

$$\frac{I_o}{I_{in_1}} = -\frac{C_2 C_5 s^2}{C_1 C_2 s^2 + G_1 C_2 s + G_1 G_3} \tag{1.6}$$

The center frequency w_o, bandwidth w_o/Q_o and quality factor Q_o are given by,

$$w_o = \sqrt{\frac{G_1 G_3}{C_2 C_4}} \tag{1.7}$$

$$\frac{w_o}{Q_o} = \frac{G_1}{C_4} \tag{1.8}$$

$$Q_o = \frac{1}{G_5}\sqrt{\frac{G_3 C_4}{G_1 C_2}} \tag{1.9}$$

Gain of highpass, lowpass and bandpass is approximately given by,

$$G_{LP} = \frac{G_5}{G_1}\ ,\ G_{HP} = \frac{C_5}{C_1}\ ,\ G_{BP} = \frac{G_5}{G_1} \tag{1.10}$$

It can be seen from equations (1.7) and (1.8) that the center frequency can be adjusted without disturbing the bandwidth by adjusting external grounded resistance R_3. Lowpass and bandpass gain can be adjusted by G_5 whereas, highpass gain can be adjusted by C_5, without disturbing the center frequency or bandwidth.

Experimental Results and Discussion

In order to validate the theoretical results, the filter is experimentally tested by using a breadboard realization. The AD844 current conveyor is used for experimental setup.

The lowpass filter experimental result, for 80kHz frequency, is shown in Figure 1.10, which confirms the theoretical analysis. The bandpass filter experimental result, for 35kHz center frequency, is shown in Figure 1.11, which also confirms the theoretical analysis. The internal resistances of the current conveyors can be added to the external resistances for predistortion design.

The highpass filter result, for 80kHz frequency, is shown in Figure 1.12. It can be seen that it does not confirm the theoretical result. In order to investigate the filter performance as a highpass filter, theoretical analysis is again performed by taking into account the parasitic resistance of current conveyor CCII#3. Only R_{x_3} is included in the analysis because it is in series with the capacitor C_5. Other internal

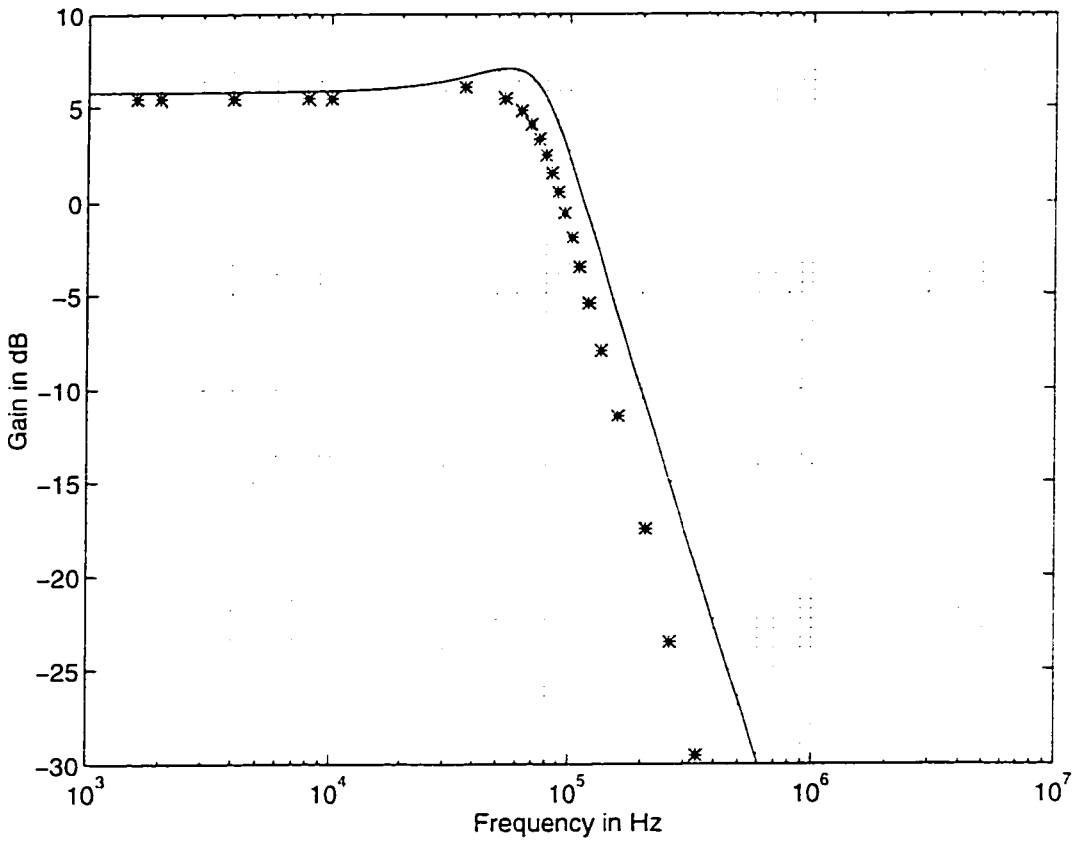


Figure 1.10: Experimental result for lowpass filter. theoretical, ***experimental, $R_1 = R_3 = 2k\Omega, R_5 = 1k\Omega, C_2 = C_4 = 1nF$

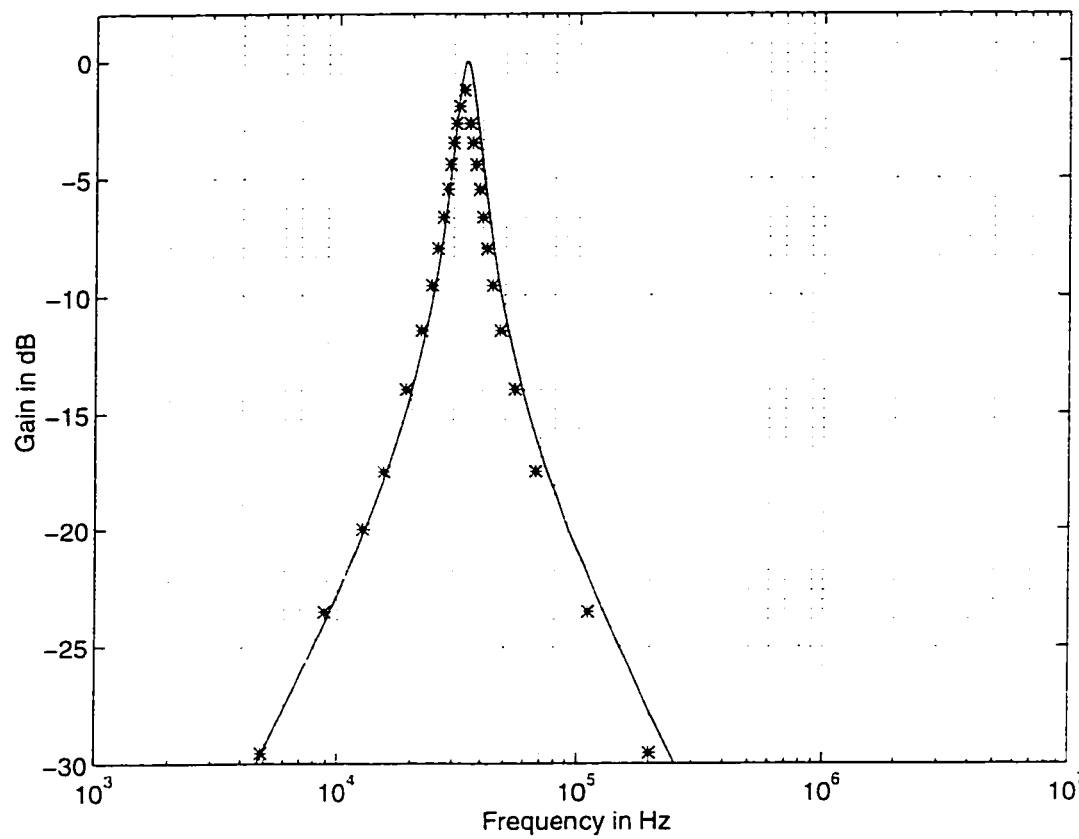


Figure 1.11: Experimental result for bandpass filter. theoretical, ***experimental, $R_1 = R_5 = 10k\Omega, R_3 = 1k\Omega, C_2 = 1nF, C_4 = 2nF$

resistacnes ($R_{x_1} and R_{x_2}$) can be easily added to the external resistances R_1 and R_3. The modified transfer function is.

$$\frac{I_o}{I_{in_1}} = -\frac{R_1 R_3 C_2 C_5 s^2}{R_1 R_3 R_{x_3} C_2 C_4 C_5 s^3 + R_3 C_2 (R_{x_3} C_5 + R_1 C_4) s^2 + (R_{x_3} C_5 + R_3 C_2) s + 1} \tag{1.11}$$

It can be seen from the modified transfer function that the filter transfer function is now a third order function. The theoretical result of equation (1.11) and the experimental result are again plotted in Figure 1.13. It can be seen that the curve for theoretical result also shows a rolloff after 100kHz, like the experimental result. This is due to the presence of internal resistance R_{x_3} in series with a capacitor. The effect of R_{x_3} is not advantageous in this circuit as a capacitor is present in series to it. So an extra condition is imposed on the proposed highpass filter i.e. $w \ll (R_{x_3} C_5)^{-1}$, otherwise erronous results will appear.

1.4 Current Controlled Conveyor

Recently, Fabre [36] exploited to advantage the parasitic resistance, as its value is dependent on the bias current. The CCII+ proposed has the parasitic resistance at port X which is current controlled, thus it introduces the concept of Current Controlled Current Conveyor (CCCII).

The basic circuit of the CCCII is the mixed translinear loop [27] shown in Figure 1.14. Applying translinear principle to the four transistors,

$$I_1 I_3 = I_2 I_4 \tag{1.12}$$

Assuming $\beta \gg 1$, the bias current $I_o = I_1 = I_3$, therefore

$$I_o^2 = I_2 I_4 \tag{1.13}$$

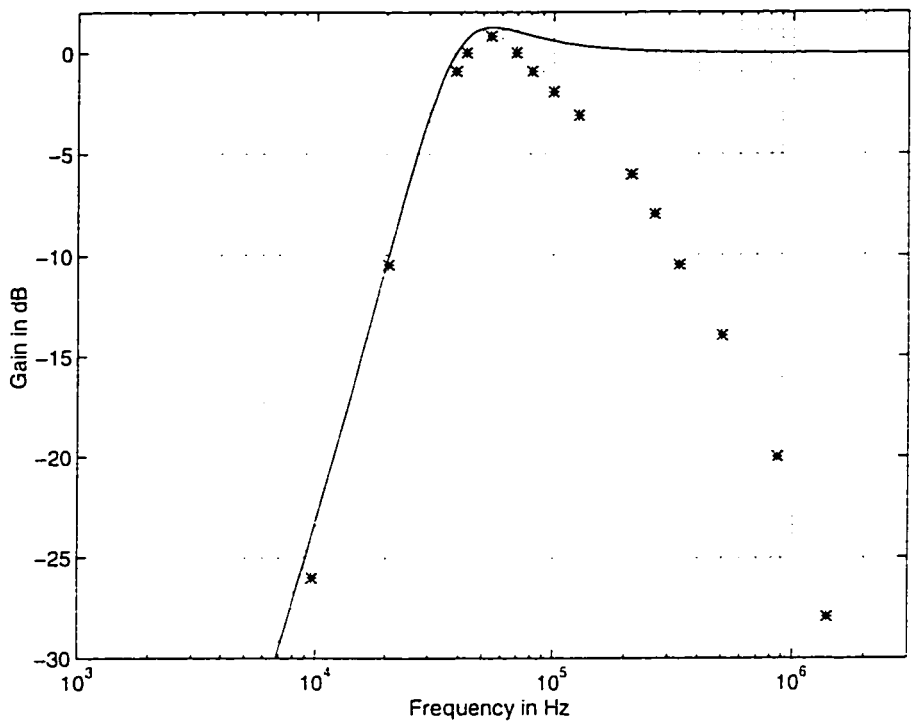


Figure 1.12: Experimental result for highpass filter. theoretical, ***experimental, $R_1 = R_3 = 2k\Omega, C_2 = C_4 = C_5 = 2nF$

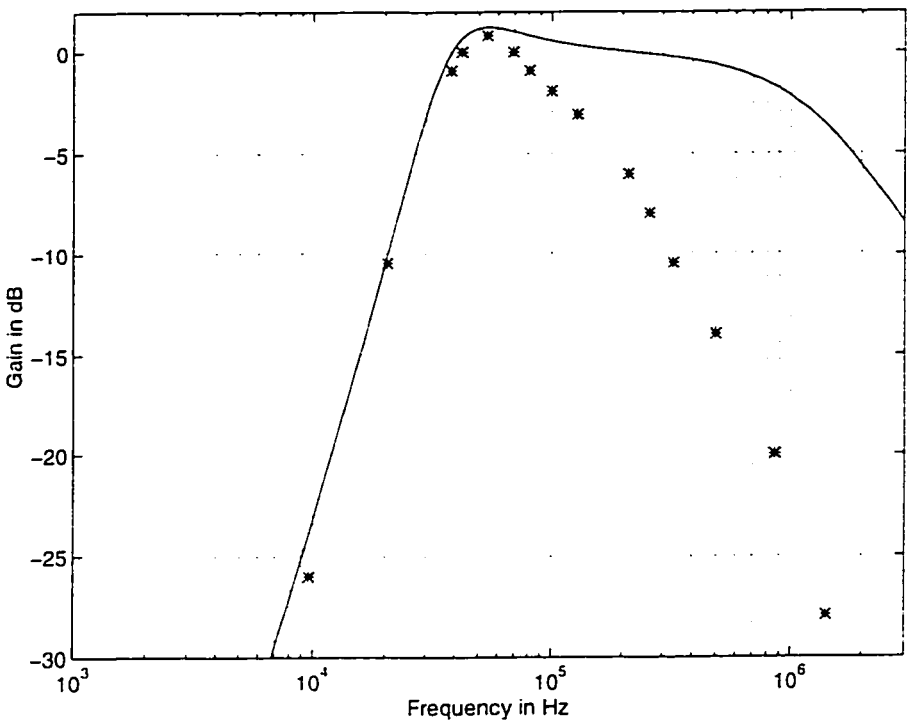


Figure 1.13: Experimental result for highpass filter with internal resistance. theoretical, ***experimental. $R_1 = R_3 = 2k\Omega, C_2 = C_4 = C_5 = 2nF$

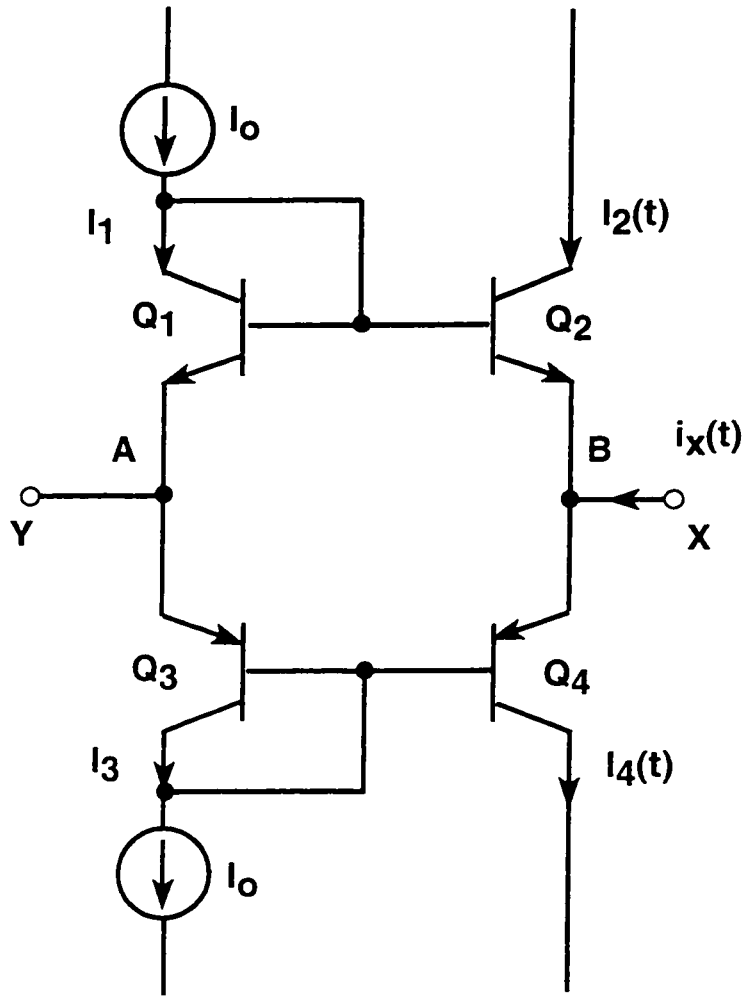


Figure 1.14: Circuit diagram of mixed translinear cell.

The expressions for I_2 and I_4 can be written in terms of $i_x(t)$ as,

$$I_2 = \frac{1}{2}[(i_x{}^2(t) + 4I_o{}^2)^{1/2} - i_x(t)] \tag{1.14}$$

$$I_4 = \frac{1}{2}[(i_x{}^2(t) + 4I_o{}^2)^{1/2} + i_x(t)] \tag{1.15}$$

The voltage difference between points A and B depends on the value of the current $i_x(t)$ and its expression is given by,

$$V_{BA} = -V_T log\frac{I_2}{I_o} \tag{1.16}$$

$$V_{BA} = -V_T log\left[-i_x(t)/2I_o + \sqrt{1 + (i_x(t)/2I_o)^2}\right] \tag{1.17}$$

$$V_{BA} = V_T sinh^{-1}(\frac{i_x(t)}{2I_o}) \tag{1.18}$$

Assuming the magnitude of current $i_x(t)$ much smaller than $2I_o$, V_{BA} is given by

$$V_{BA} = \frac{V_T}{2I_o} i_x \tag{1.19}$$

Thus R_x is calculated as follows

$$R_x = \frac{V_{BA}}{i_x} = \frac{V_T}{2I_o} \tag{1.20}$$

where V_T is the thermal voltage. Equation (1.20) shows that the small signal resistance R_x is dependent on the bias current. The mixed translinear implementation of a second generation current controlled conveyor (CCCII+) and its symbol are shown in Figure 1.15. The matrix relationship, by taking intrinsic resistance R_x into account becomes,

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{1.21}$$

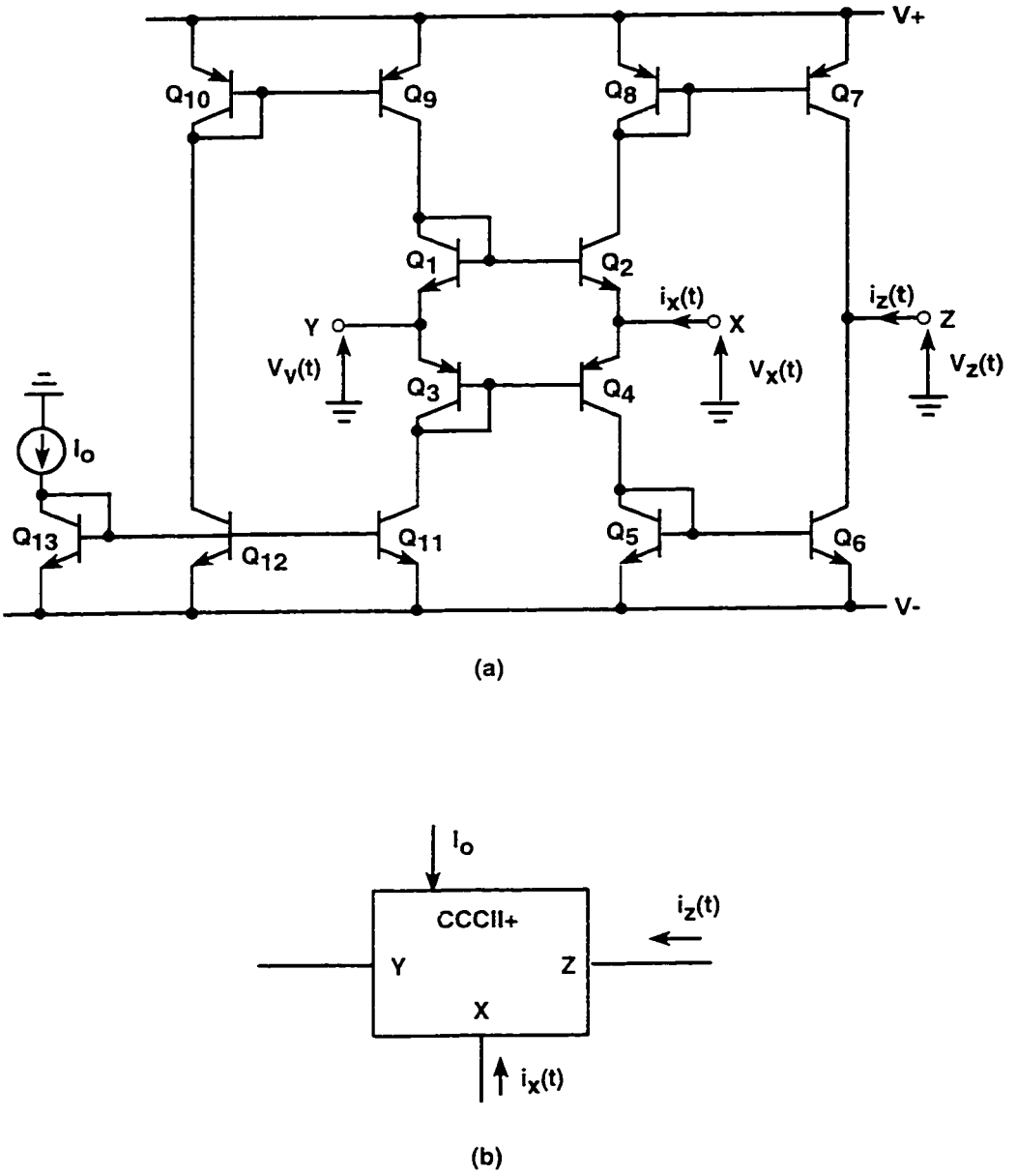


Figure 1.15: (a)Circuit diagram of CCCII+. (b) Symbol of CCCII+.

A negative current transfer ratio can be easily obtained by adding two cross coupled current mirrors.

This topology results in the following advantages.

- The parasitic resistance R_x is current controlled. Therefore circuits can be implemented using CCCII without external resistance. Such circuits could be programmed.
- Due to the use of monolithic implementation it has excellent frequency response.
- The number of active and passive components are very few and therefore require less silicon area in implementation.
- Because of low component count and no resistances, power dissipation is very low.
- Circuits using this CCCII will also take very less silicon area as no external resistances will be used.

Fabre et al. [36] performed a comparison between controlled conveyor (CCCII) and operational transconductance amplifier (OTA). This comparison shows that CCCII is a better option than OTA. For a conventional bipolar OTA the value of transconductance (g_m) is $I_o/2V_T$ [1], while $1/R_x$ for the CCCII is $2I_o/V_T$. Thus, for the same value of I_o the transconductance of OTA will be 4 times less than that of the controlled conveyor. This means that if a filter is designed by using only OTAs or only CCCIIs then for the same center frequency f_o, which is linearly proportional to the bias current I_o, the OTA implementation will result in higher

power consumption. Fabre showed that the implementation of voltage to current convertor using OTA results in 3 times greater power consumption than with the controlled conveyor. Also because of the use of high values of currents, the maximum frequency usable will be reached sooner. Therefore the frequency response and power dissipation of the CCCII based circuits is expected to be better than OTA based circuits.

Like the transconductance of operational transconductance amplifier (OTA), internal resistance of controlled conveyor is temperature dependent ($R_x = V_T/(2I_o)$). Its temperature dependence can be reduced by using a PTAT current source [37].

The most important deviation in the value of internal resistance R_x occurs for very low or very high values of bias current. These deviations occur because of the difference between the collector and bias current of the transistors Q_1 and Q_3 (see Figure 1.10). These current deviations result from the low value of the current gain β of transistors Q_1 to Q_4 operating for very low or very high values of collector currents [36]. To reduce these deviations, transistors with higher values of β should be used in realizing CCCII.

1.5 Applications of Current Controlled Conveyor

Although current conveyors are used in many applications [1], in this thesis stress is upon universal filters, higher order filters, oscillator and impedance simulation circuits. These are discussed briefly.

1.5.1 Active-C Universal Filters

After the work of Nawrocki and Klein [38] the emphasis is on designing universal filters, as all the major filter functions can be implemented from the same structure and the higher orders can be implemented by cascading the second order function. Although the original design using operational transconductance amplifiers (OTAs) [39]-[42] is suitable for integration due to the absence of resistors in the circuit, performance limitations of OTAs such as poor bandwidth and poor output drive capabilities restrict the overall operating performance [43][44]. High performance current conveyors (CCs) become an attractive alternative to OTAs in this application because of their higher bandwidth and improved current drive capabilities [43]-[49]. But the disadvantage associated with current conveyors is lack of programmability. This limitation could be overcome by using current controlled conveyor, by taking advantage of its internal programmable resistance. At present only few circuits using the current controlled conveyor are available. However these suffer from certain disadvantages. The bandpass filter proposed by Fabre [36] does not possess independent control of frequency and bandwidth and the universal filter proposed by Kiranon et al. [50] uses floating capacitors and cannot realize allpass and notch functions.

1.5.2 Sinusoidal Oscillators

Over the past few years a number of schemes have been developed to realize sinusoidal oscillators [51]-[56]. Schemes using OTAs give the advantage of programmability over the simple current conveyors. Current controlled conveyor has the programmability feature and gives better performance in terms of frequency and power

dissipation. So far there are only two circuits in the literature that use current controlled conveyor for sinusoidal oscillator and are proposed by Kiranon et al. [57][50]. The disadvantage in the first circuit is that the condition of oscillation and the frequency of oscillation are not independently controllable. Whereas, the second circuit requires another current controlled conveyor for sensing the output current.

1.5.3 Impedance Simulation

Impedance realization finds wide application in the design of active filters and oscillators. There are lots of circuits realizing impedance with general impedance converter (GIC) and negative impedance converter (NIC) using operational amplifier [58][59], but they suffer from poor bandwidth. Schemes using OTA provide the programmability option but they also suffer from poor bandwidth [60]. Until now, there is only one circuit realizing floating inductor using current controlled conveyor [61].

1.5.4 Higher Order Filter Synthesis

Although there are many higher order structures in the literature but most of them are voltage mode and use large number of active and passive components. Some of the techniques in the literature are presented by Acar, Gunes and Jie Wu. The filters proposed by Acar [62][63] use floating and large number of passive and active components and are voltage mode and the one proposed by Gunes and Anday [64] and Jie Wu [65] can realize only low pass filter. The number of active and passive components is an important parameter for higher order filters. The number of active components is rapidly growing, for the above mentioned filter structures, as the filter

order increases. This results in greater power consumption and larger chip area. Also the use of floating capacitors increases the area. Thus reducing the number of elements and utilizing grounded capacitors becomes a major consideration in high frequency continuous time filter design.

Until now, there are no higher order filter structures in the literature using current controlled conveyor.

1.6 Problem Definition

According to the literature review, it is believed that current controlled conveyor is more versatile and flexible active device as compared to other available devices. It results in circuits without external resistances, with less power consumption and takes less area for implementation. However, only a little work has been done in designing application circuits like universal filters and sinusoidal oscillators using current controlled conveyor. The main objective of this thesis is to propose new universal filters, higher order filters, sinusoidal oscillator and impedance simulation circuits using current controlled conveyor.

Chapter 2

FILTERS,OSCILLATOR AND IMPEDANCE SIMULATION

An electric filter can be defined as an interconnected network of electrical components that shapes the spectrum of the input signal in order to obtain an output signal with the desired frequency content. Thus a filter has passbands where the frequency components are transmitted to the output and stopbands where they are rejected. The major types of such filters are lowpass(LP), highpass(HP), bandpass(BP), bandreject(BR) or notch, and allpass(AP).

The earliest filter designs use only resistors, inductors and capacitors and therefore are called passive RLC filters. With the growing pressure towards miniaturisation, inductors were found to be too bulky so that designers started to replace passive RLC filters by active RC circuits. Aside from their obvious size and weight advantages over equivalent passive RLC implementations, active filters provide the following additional advantages:

- Increased circuit reliability because all processing steps can be automated.

- In large quantities the cost of integrated circuit active filters are much lower than equivalent passive filters.
- Improvement in performance because high quality components can be readily manufactured.
- A reduction in parasitics because of smaller size.
- Active filters and digital circuitry can be integrated onto the same silicon chip.
- The design and tuning processes are simpler than those for passive filters.

Because of these advantages active filters are used for a wide variety of applications such as voice and video signal processing for the communication industry. Much of the motivation for considering active filters stems from the progress that has occured in integrated circuit technology.

2.1 Universal Second Order Filters

Second order active filters are of great interest because several cells of that kind can be connected in cascade to implement higher order filters. Cascade filter design is the approach most widely used to design active filters, because the individual filter sections are noninteracting.

For a voltage-mode second order filter it is advantageous to have infinite input impedance because several cells can be directly connected in cascade with no need to interpose active separating stages. Similarly for a current mode active filter it is desirable to have low input impedance and high output impedance.

A universal voltage or current-mode filter is capable of realizing the five different basic functions (LP, HP, BP, BR and AP filters). Advantage is that all the filter functions can be implemented from the same structure. There are two categories of universal filters: multiple input single output and single input multiple output. The former can realize each function separately by controlling the inputs while the latter can provide all the five functions simultaneously.

2.2 Design Requirements

An active filter should be designed by taking into consideration the following requirements.

- Independent control of center frequency w_o and the bandwidth w_o/Q_o, where Q_o is the quality factor.
- Use of grounded capacitors to overcome the effect of stray capacitance.
- It is advantageous if the center frequency and the bandwidth are programmable.
- Minimum number of active and passive components. This will result in filters with less power consumption, less silicon area and lower sensitivity.
- No matching/cancellation requirements for realizing different filtering functions.
- The sensitivity of filter parameters (w_o, w_o/Q_o) to active and passive components should be low (less than unity).
- Filters should be directly cascadable.

Current controlled conveyor is an excellent candidate for the above mentioned requirements. Its internal resistance can be controlled by bias current, therefore programmable filters are easy to design. Moreover, filters will have no external resistances which will result in less silicon area for implementation and low power consumption.

2.3 Proposed Circuits

Only a few universal filters are available that use the current controlled conveyor. All of them suffer from certain disadvantages. The bandpass filter proposed by Fabre [36] does not possess independent control of frequency and bandwidth and the universal filter proposed by Kiranon et al. [50] uses floating capacitors and cannot realize allpass and notch functions. In the following section unviversal filters are proposed that remove the disadvantages associated with the above mentioned work.

2.3.1 Universal Filter 1

The proposed circuit is shown in Figure 2.1 [66] (Appendix B). It is a current-mode circuit using current controlled conveyor (CCCII) with internal resistance R_x. This filter uses three multiple output CCCII, two capacitors and no external resistances. Routine analysis of the circuit assuming ideal CCCII ($v_x = v_y + i_x R_x, i_x = i_z$) gives the following current transfer functions.

$$\frac{I_{LP}}{I_{in}} = \frac{R_{x_3}}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_2}R_{x_3}C_1s + R_{x_3}} \tag{2.1}$$

$$\frac{I_{HP}}{I_{in}} = \frac{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_2}R_{x_3}C_1s + R_{x_3}} \tag{2.2}$$

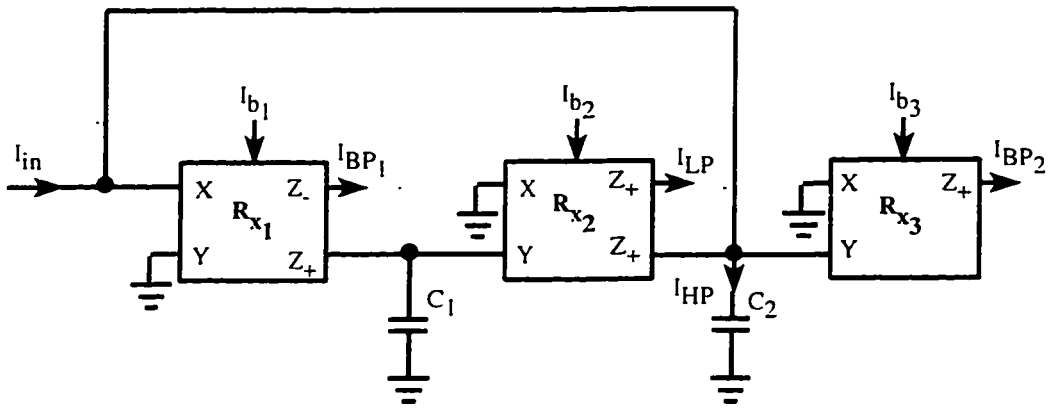


Figure 2.1: CCCII based Universal second order filter-1.

$$\frac{I_{BP_1}}{I_{in}} = \frac{R_{x_2}R_{x_3}C_1 s}{R_{x_1}R_{x_2}R_{x_3}C_1C_2 s^2 + R_{x_2}R_{x_3}C_1 s + R_{x_3}} \tag{2.3}$$

$$\frac{I_{BP_2}}{I_{in}} = \frac{R_{x_1}R_{x_2}C_1 s}{R_{x_1}R_{x_2}R_{x_3}C_1C_2 s^2 + R_{x_2}R_{x_3}C_1 s + R_{x_3}} \tag{2.4}$$

The high pass current is flowing through capacitor C_2. It can be sensed by connecting another CCCII as a current follower. A current mode notch signal is easily obtained by connecting the I_{HP} and I_{LP} output terminals. Let $I_{NH} = I_{HP} + I_{LP}$, we obtain the current-mode notch transfer function as,

$$\frac{I_{NH}}{I_{in}} = \frac{R_{x_1}R_{x_2}R_{x_3}C_1C_2 s^2 + R_{x_3}}{R_{x_1}R_{x_2}R_{x_3}C_1C_2 s^2 + R_{x_2}R_{x_3}C_1 s + R_{x_3}} \tag{2.5}$$

Similarly by connecting the I_{HP}, I_{BP_1} and I_{LP} output terminals, a current mode allpass response is obtained

$$\frac{I_{AP}}{I_{in}} = \frac{R_{x_1}R_{x_2}R_{x_3}C_1C_2 s^2 - R_{x_2}R_{x_3}C_1 s + R_{x_3}}{R_{x_1}R_{x_2}R_{x_3}C_1C_2 s^2 + R_{x_2}R_{x_3}C_1 s + R_{x_3}} \tag{2.6}$$

The center frequency w_o, bandwidth w_o/Q_o and quality factor Q_o are given by,

$$w_o = \sqrt{\frac{1}{R_{x_1}R_{x_2}C_1C_2}} \tag{2.7}$$

$$\frac{w_o}{Q_o} = \frac{1}{R_{x_1}C_2} \tag{2.8}$$

$$Q_o = \sqrt{\frac{R_{x_1}C_2}{R_{x_2}C_1}} \tag{2.9}$$

Gain of high pass, lowpass and bandpass are approximately given by,

$$G_{LP} = G_{HP} = G_{BP_1} = 1 \ , \ G_{BP_2} = \frac{R_{x_1}}{R_{x_3}} \tag{2.10}$$

It can be seen from equations (2.7) and (2.8) that the center frequency can be adjusted without disturbing the bandwidth. The center frequency w_o can be electronically tuned by adjusting I_{b_2}. The gain of bandpass function I_{BP_2} can be independently adjusted without disturbing w_o and w_o/Q_o by adjusting I_{b_3}. Another important advantage is that no matching condition is required for the realization of allpass and notch functions.

In summary the proposed circuit at most needs four multiple output CCCII for the realization of five basic filter functions, one grounded and one floating capacitor (for the realization of highpass filter) and uses no external resistance.

Sensitivity Analysis

Nonideal analysis is required to find the active sensitivities of the filter. Assuming that the nonideal port relations of the CCCII can be expressed as $v_x = \beta v_y + i_x R_x, i_z = \alpha i_x$, where $\alpha = 1 - \delta$ ($|\delta| \ll 1$) denotes the current tracking error, $\beta = 1 - \epsilon$ ($|\epsilon| \ll 1$) represents the voltage tracking error, the output currents can now be expressed as,

$$\frac{I_{LP}}{I_{in}} = \frac{\alpha_1 R_{x_3}}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_2}R_{x_3}C_1s + \alpha_1\alpha_2\beta_2R_{x_3}} \tag{2.11}$$

$$\frac{I_{HP}}{I_{in}} = \frac{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_2}R_{x_3}C_1s + \alpha_1\alpha_2\beta_2R_{x_3}} \tag{2.12}$$

$$\frac{I_{BP_1}}{I_{in}} = \frac{R_{x_2}R_{x_3}C_1s}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_2}R_{x_3}C_1s + \alpha_1\alpha_2\beta_2R_{x_3}} \tag{2.13}$$

$$\frac{I_{BP_2}}{I_{in}} = \frac{\alpha_3\beta_3 R_{x_1} R_{x_2} C_1 s}{R_{x_1} R_{x_2} R_{x_3} C_1 C_2 s^2 + R_{x_2} R_{x_3} C_1 s + \alpha_1\alpha_2\beta_2 R_{x_3}} \tag{2.14}$$

The center frequency w_o, bandwidth w_o/Q_o and quality factor Q_o are given by,

$$w_o = \sqrt{\frac{\alpha_1\alpha_2\beta_2}{R_{x_1} R_{x_2} C_1 C_2}} \tag{2.15}$$

$$\frac{w_o}{Q_o} = \frac{1}{R_{x_1} C_2} \tag{2.16}$$

$$Q_o = \sqrt{\frac{\alpha_1\alpha_2\beta_2 R_{x_1} C_2}{R_{x_2} C_1}} \tag{2.17}$$

By defining the sensitivity [58] of w_o and Q_o to the parameter F by,

$$S_F^{w_o} = \frac{dw_o}{dF}\frac{F}{w_o} \; and \; S_F^{Q_o} = \frac{dQ_o}{dF}\frac{F}{Q_o} \tag{2.18}$$

From equations (2.15) and (2.17) it is easy to show that the active and passive sensitivities of the parameters w_o and Q_o (i.e. per-unit change in w_o and Q_o due to a given per-unit change in F) are,

$$S_{\alpha_1}^{w_o} = S_{\alpha_2}^{w_o} = S_{\beta_2}^{w_o} = \frac{1}{2}\ ,\ S_{\alpha_3}^{w_o} = S_{\beta_1}^{w_o} = S_{\beta_3}^{w_o} = 0$$

$$S_{R_{x_1}}^{w_o} = S_{R_{x_2}}^{w_o} = S_{C_1}^{w_o} = S_{C_2}^{w_o} = -\frac{1}{2}\ ,\ S_{R_{x_3}}^{w_o} = 0$$

$$S_{\alpha_1}^{Q_o} = S_{\alpha_2}^{Q_o} = S_{\beta_2}^{Q_o} = \frac{1}{2}\ ,\ S_{\alpha_3}^{Q_o} = S_{\beta_1}^{Q_o} = S_{\beta_3}^{Q_o} = 0$$

$$S_{R_{x_1}}^{Q_o} = -S_{R_{x_2}}^{Q_o} = -S_{C_1}^{Q_o} = S_{C_2}^{Q_o} = \frac{1}{2}\ ,\ S_{R_{x_3}}^{Q_o} = 0$$

All of the active and passive sensitivities are small (no more than unity).

Simulation Results and Discussion

To validate the theoretical analysis, the proposed universal filter in Figure 2.1 is simulated using ICAPS circuit simulation program. The CCCII± is modelled by the schematic implementation of Figure 1.15, proposed by Fabre et al. [36] with dc

supply voltage of ±2.5V. The simulation results reported here were obtained using the transistors PR100N(PNP) and NR200N(NPN) of the bipolar arrays ALA400 from AT&T [67].

Figures 2.2 to 2.7 show the theoretical and simulation results of lowpass, highpass, bandpass, notch and allpass (gain and phase response) filters respectively. Lowpass, highpass, notch and allpass filters are simulated for (1)24.48kHz and (2)244.8kHz frequencies. Bandpass filter is simulated for (1)54.7kHz and (2)244.7kHz frequencies. It can be seen that the simulation results agree very well with the presented theory. Deviations less than 5% are obtained for these results. Figure 2.8 shows the effect of changing I_{b_1}. It can be seen that the bandpass gain of I_{BP_2} can be independently adjusted without disturbing the bandwidth and center frequency. The results are obtained by simulating the bandpass filter for gain=1,2,4 with 77.4kHz center frequency. In short the proposed circuit offers the following advantages.

- Arbitrary biquadratic transfer functions are realized with single input.
- With multiple outputs all the five basic filter functions can be obtained.
- Center frequency w_o can be independently adjusted.
- No external resistances are used.
- No matching conditions are required for the realization of allpass and notch transfer functions.
- Low active and passive sensitivities.

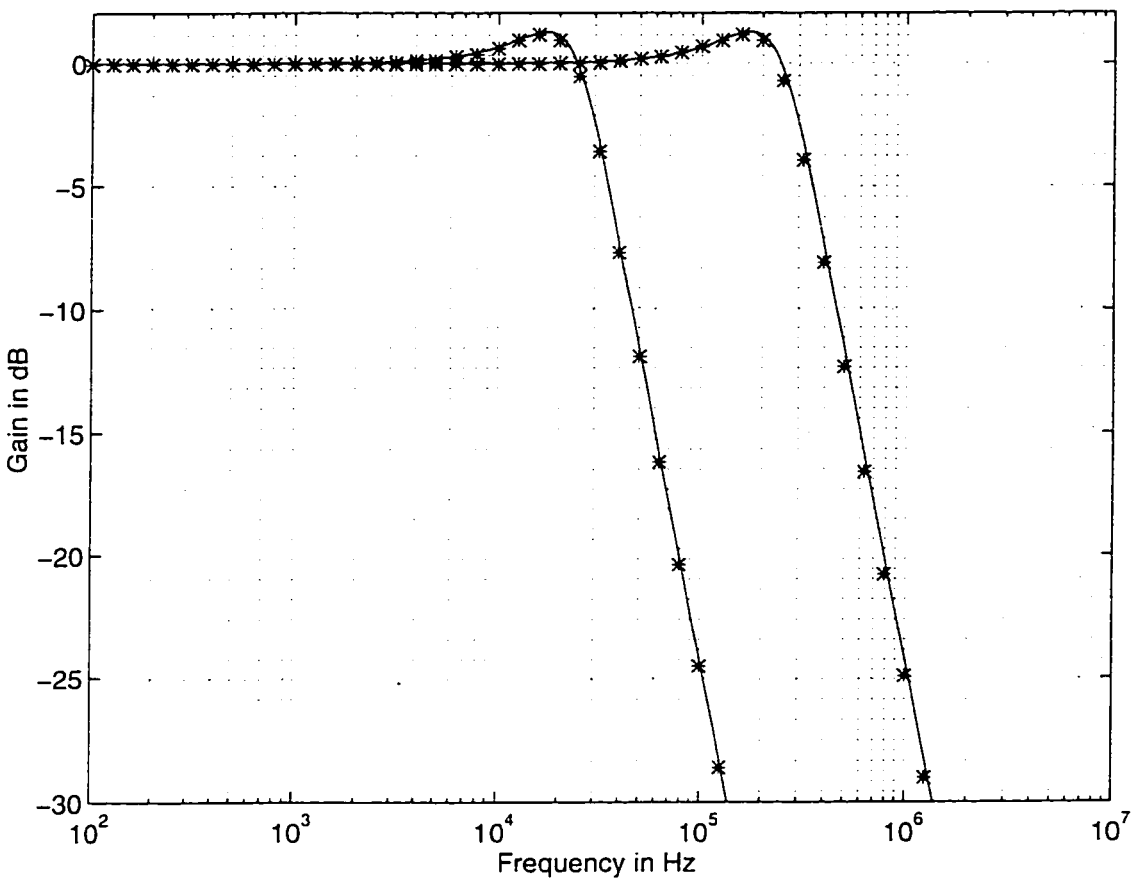


Figure 2.2: Simulation results of the lowpass filter. theoretical,***simulation (1) $I_1 = I_2 = I_3 = 10\mu A, C_1 = C_2 = 5nF$ (2) $I_1 = I_2 = I_3 = 100\mu A, C_1 = C_2 = 5nF$

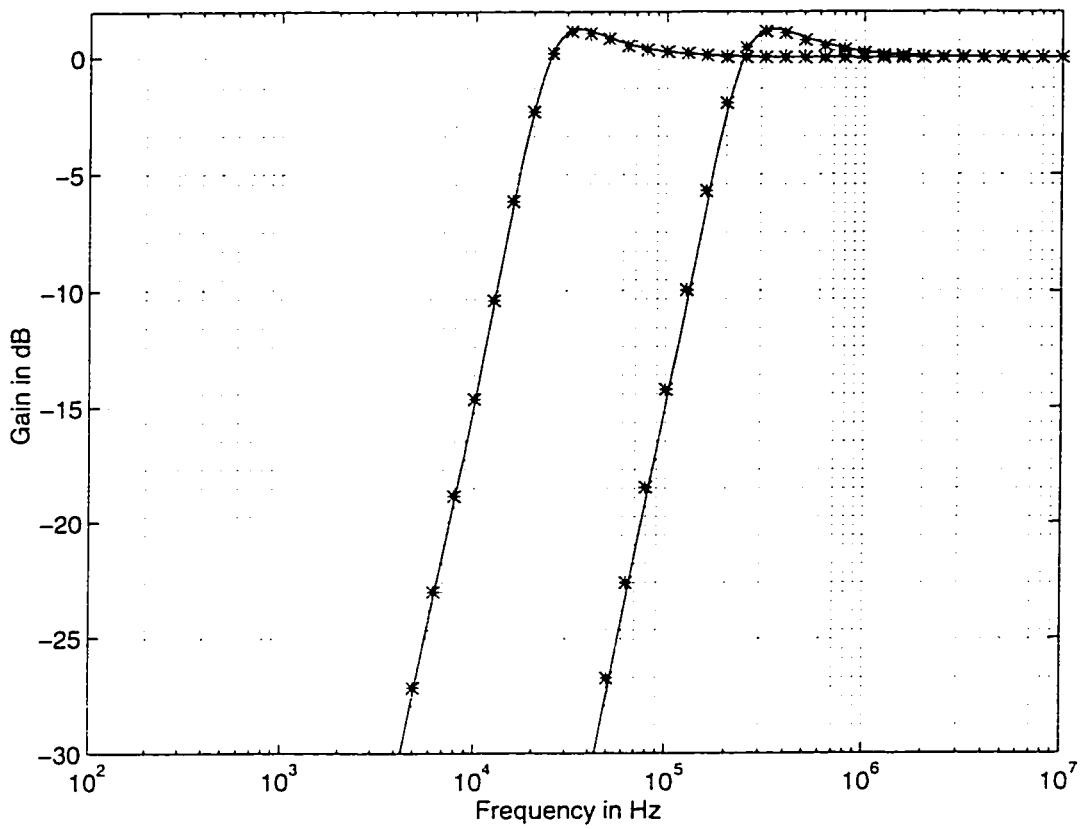


Figure 2.3: Simulation results of the highpass filter. theoretical,***simulation (1) $I_1 = I_2 = I_3 = 10\mu A, C_1 = C_2 = 5nF$ (2) $I_1 = I_2 = I_3 = 100\mu A, C_1 = C_2 = 5nF$

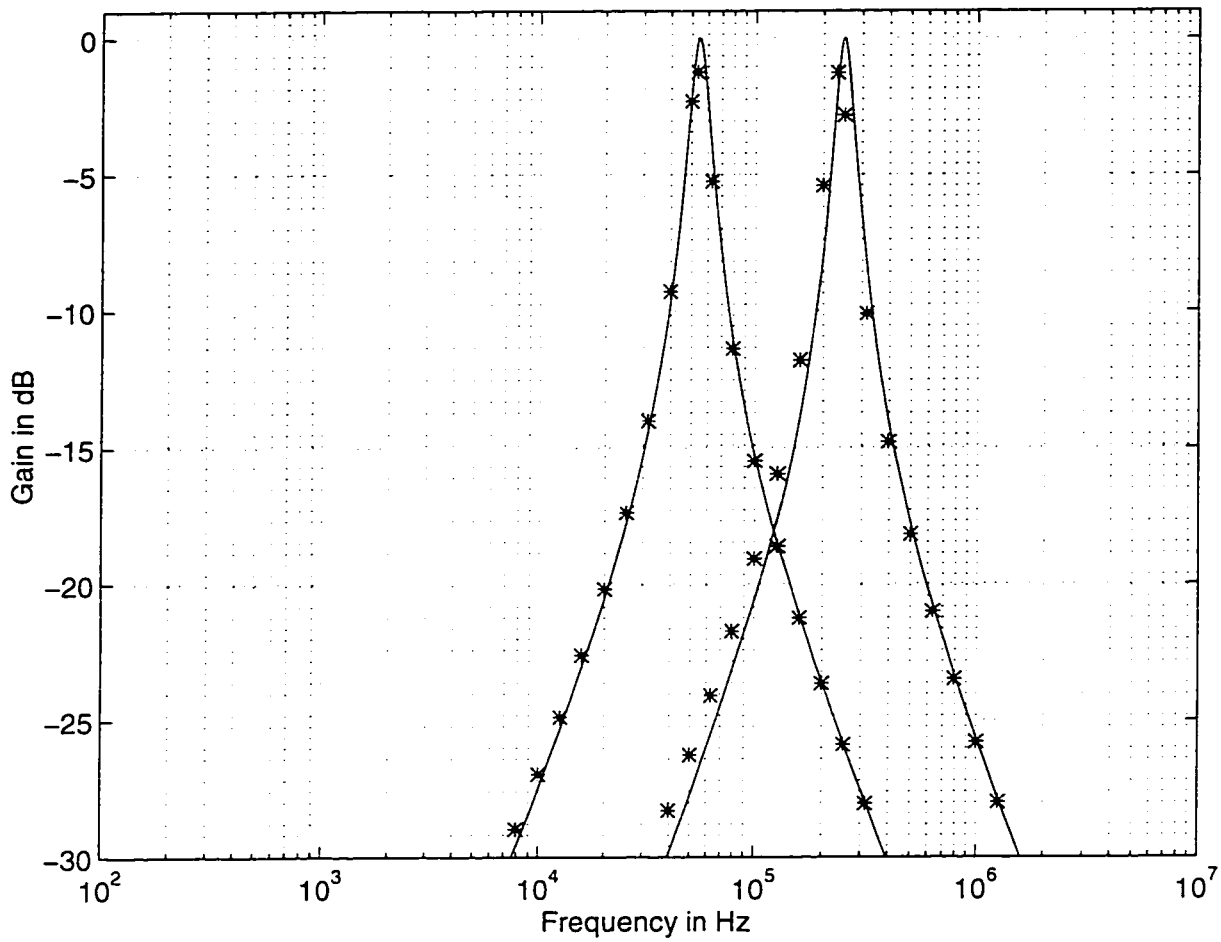


Figure 2.4: Simulation results of the bandpass filter. theoretical,***simulation (1) $I_1 = I_3 = 5\mu A, I_2 = 100\mu A, C_1 = C_2 = 5nF$ (2) $I_1 = I_3 = 20\mu A, I_2 = 520\mu A, C_1 = C_2 = 5nF$

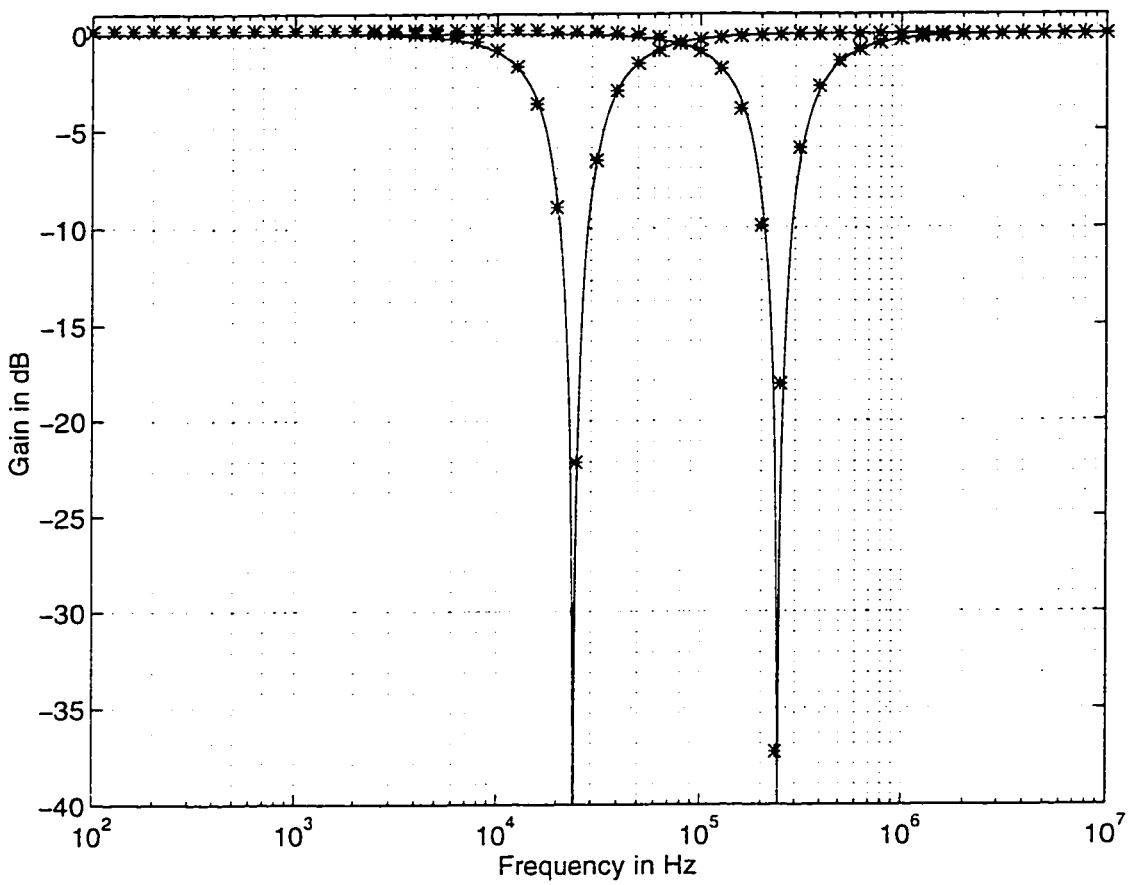


Figure 2.5: Simulation results of the notch filter. theoretical,***simulation (1) $I_1 = I_2 = I_3 = 10\mu A, C_1 = C_2 = 5nF$ (2) $I_1 = I_2 = I_3 = 100\mu A, C_1 = C_2 = 5nF$

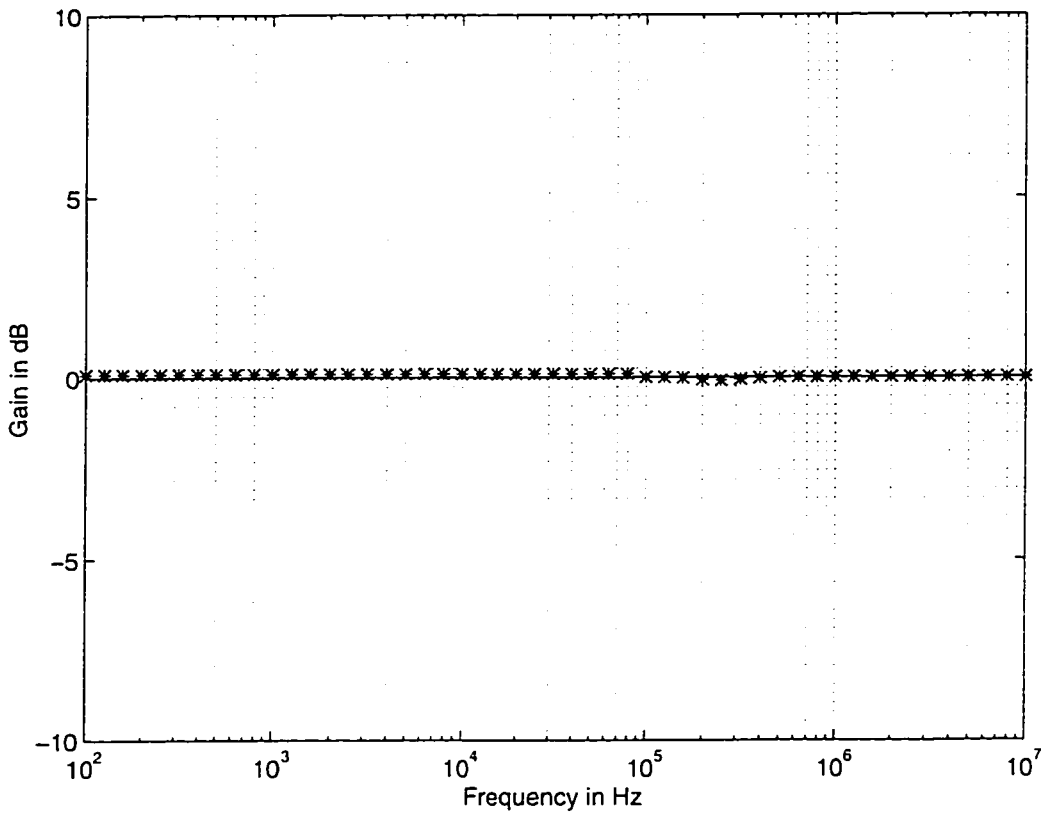


Figure 2.6: Simulation results of the gain of allpass filter. -theoretical.***simulation . $I_1 = I_2 = I_3 = 100\mu A. C_1 = C_2 = 5nF$

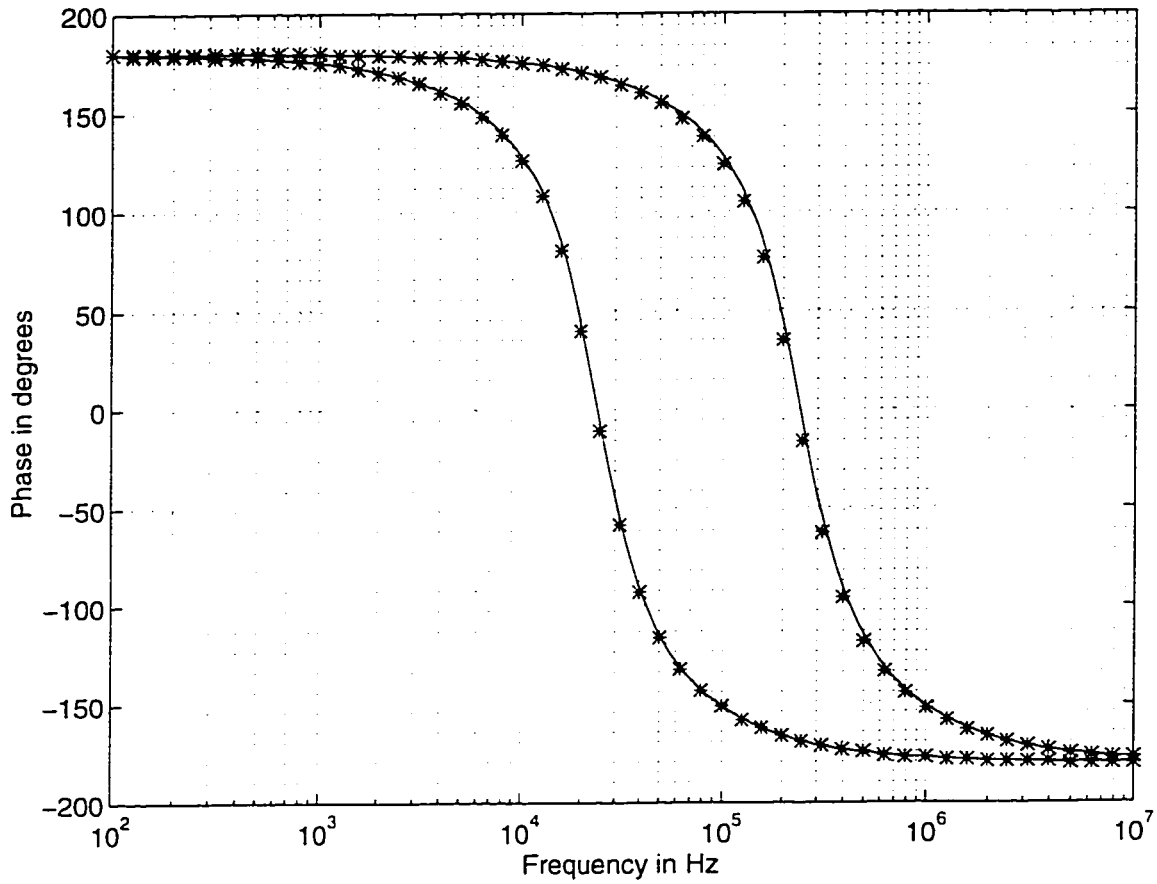


Figure 2.7: Simulation results of the phase of allpass filter. theoretical, ***simulation (1) $I_1 = I_2 = I_3 = 10\mu A, C_1 = C_2 = 5nF$ (2) $I_1 = I_2 = I_3 = 100\mu A, C_1 = C_2 = 5nF$

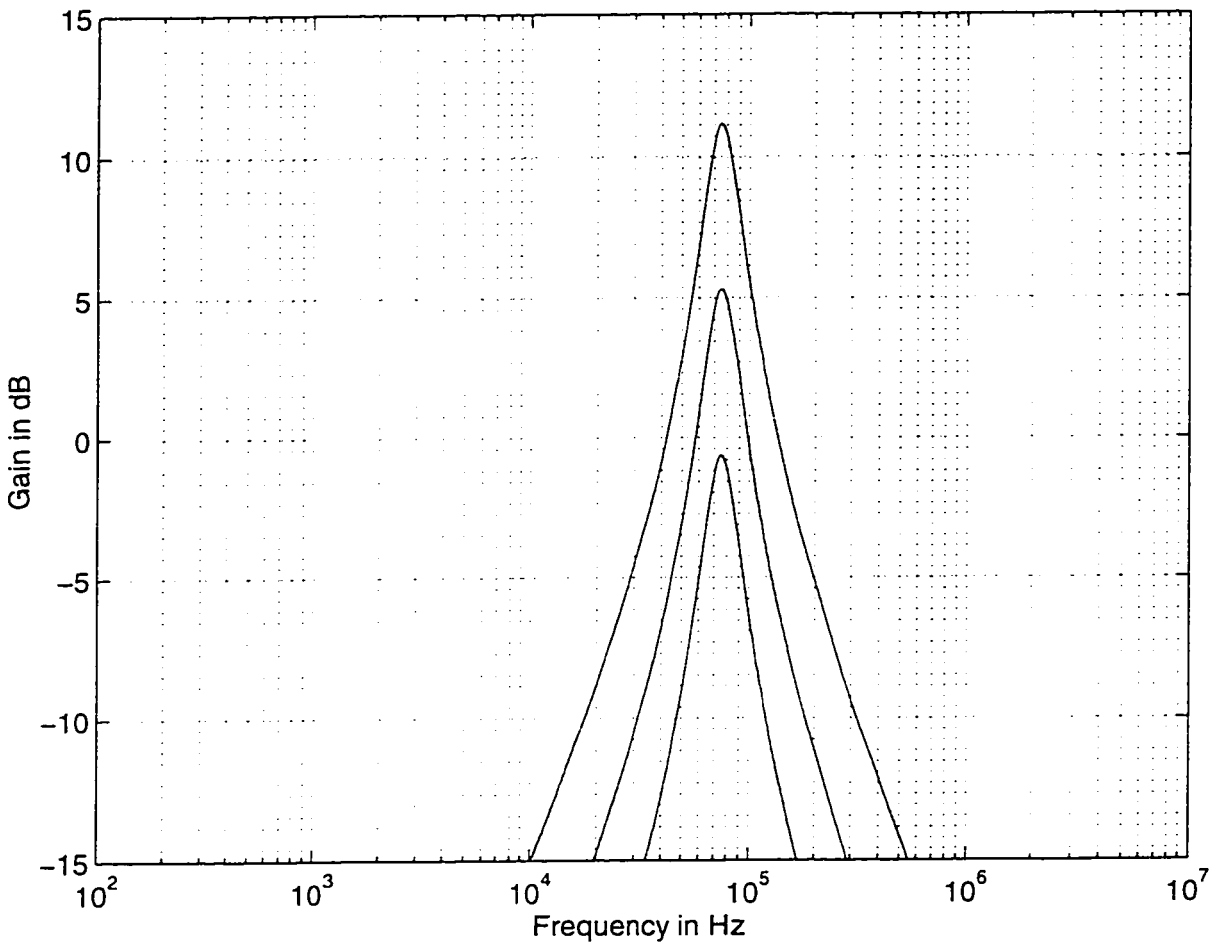


Figure 2.8: Simulation results of the variable gain of bandpass filter. (1) $I_1 = I_3 = 10\mu A, I_2 = 100\mu A, C_1 = C_2 = 5nF$ (2) $I_1 = 10\mu A, I_2 = 100\mu A, I_3 = 20\mu A, C_1 = C_2 = 5nF$ (3) $I_1 = 10\mu A, I_2 = 100\mu A, I_3 = 40\mu A, C_1 = C_2 = 5nF$

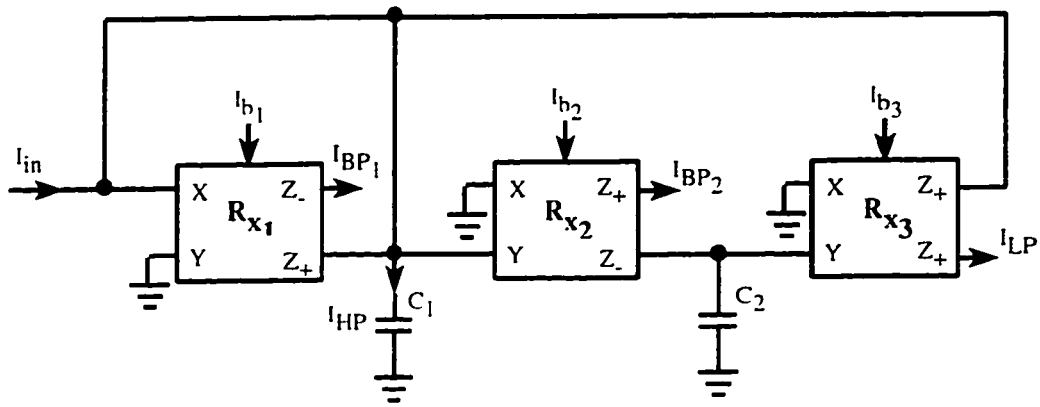


Figure 2.9: CCCII based Universal second order filter-2.

The disadvantage associated with this filter is that the high pass current is flowing through a capacitor. As a result the capacitor will be floating if this current needs to be sensed. Also the bandwidth ω_o/Q_o cannot be set independently without disturbing the center frequency. To make the bandwidth and center frequency independent, another filter is proposed with some modifications.

2.3.2 Universal Filter 2

The proposed circuit is shown in Figure 2.9. It is a current-mode circuit using current controlled conveyor (CCCII) with internal resistance R_x. This filter uses three multiple output CCCII, two capacitors and no external resistances. Assuming that the nonideal port relations of the CCCII can be expressed as $v_x = \beta v_y + i_x R_x, i_z = \alpha i_x$, where $\alpha = 1 - \delta$ ($|\delta| \ll 1$) denotes the current tracking error, $\beta = 1 - \epsilon$ ($|\epsilon| \ll 1$) represents the voltage tracking error, gives the following current transfer functions,

$$\frac{I_{LP}}{I_{in}} = \frac{\alpha_2\beta_2\beta_3 R_{x_1}}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + (1+\alpha_1)R_{x_2}R_{x_3}C_2s + \alpha_2\alpha_3\beta_2\beta_3 R_{x_1}} \quad (2.19)$$

$$\frac{I_{HP}}{I_{in}} = \frac{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + (1+\alpha_1)R_{x_2}R_{x_3}C_2s + \alpha_2\alpha_3\beta_2\beta_3 R_{x_1}} \quad (2.20)$$

$$\frac{I_{BP_1}}{I_{in}} = \frac{R_{x_2}R_{x_3}C_2s}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + (1+\alpha_1)R_{x_2}R_{x_3}C_2s + \alpha_2\alpha_3\beta_2\beta_3 R_{x_1}} \quad (2.21)$$

$$\frac{I_{BP_2}}{I_{in}} = -\frac{\beta_2 R_{x_1}R_{x_3}C_2s}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + (1+\alpha_1)R_{x_2}R_{x_3}C_2s + \alpha_2\alpha_3\beta_2\beta_3 R_{x_1}} \quad (2.22)$$

The high pass current is flowing through capacitor C_1. It can be sensed by connecting another CCCII as a current follower. A current mode notch signal is easily obtained by connecting the I_{HP} and I_{LP} output terminals. Similarly by connecting the $I_{HP}, I_{BP_1}, I_{BP_2}$ and I_{LP} output terminals, a current mode allpass response is obtained, but with the condition that $R_{x_1} = R_{x_2}$.

The center frequency w_o, bandwidth w_o/Q_o and quality factor Q_o are given by,

$$w_o = \sqrt{\frac{\alpha_2\alpha_3\beta_2\beta_3}{R_{x_2}R_{x_3}C_1C_2}} \quad (2.23)$$

$$\frac{w_o}{Q_o} = \frac{1+\alpha_1}{R_{x_1}C_1} \quad (2.24)$$

$$Q_o = \frac{R_{x_1}}{1+\alpha_1}\sqrt{\frac{\alpha_2\alpha_3\beta_2\beta_3 C_1}{R_{x_2}R_{x_3}C_2}} \quad (2.25)$$

Gain of high pass, lowpass and bandpass are approximately given by,

$$G_{LP} = G_{HP} = 1 \ . \ G_{BP_1} = \frac{1}{2} \ . \ G_{BP_2} = \frac{R_{x_1}}{2R_{x_2}} \quad (2.26)$$

It can be seen from equations (2.23) and (2.24) that the center frequency can be adjusted without disturbing the bandwidth. The center frequency w_o can be electronically tuned by adjusting I_{b_2},whereas the bandwidth w_o/Q_o can be separately adjusted by I_{b_1} without disturbing w_o.

In summary the proposed circuit at most needs four multiple output CCCII for the realization of five basic filter functions, one grounded and one floating capacitor (for the realization of highpass filter) and uses no external resistance.

Sensitivity Analysis

From equations (2.23) and (2.24) it is easy to show that the active and passive sensitivities of the parameters w_o and Q_o are,

$$\begin{aligned}
S_{\alpha_2}^{w_o} &= S_{\alpha_3}^{w_o} = S_{\beta_2}^{w_o} = S_{\beta_3}^{w_o} = \frac{1}{2}\ ,\ S_{\alpha_1}^{w_o} = S_{\beta_1}^{w_o} = 0 \\
S_{R_{x_2}}^{w_o} &= S_{R_{x_3}}^{w_o} = S_{C_1}^{w_o} = S_{C_2}^{w_o} = -\frac{1}{2}\ ,\ S_{R_{x_1}}^{w_o} = 0 \\
S_{\alpha_2}^{Q_o} &= S_{\alpha_3}^{Q_o} = S_{\beta_2}^{Q_o} = S_{\beta_3}^{Q_o} = \frac{1}{2}\ ,\ S_{\beta_1}^{Q_o} = 0\ ,\ S_{\alpha_1}^{Q_o} l - 1 \\
-S_{R_{x_2}}^{Q_o} &= -S_{R_{x_3}}^{Q_o} = -S_{C_2}^{Q_o} = S_{C_1}^{Q_o} = \frac{1}{2}\ ,\ S_{R_{x_1}}^{Q_o} = 1
\end{aligned}$$

All of the active and passive sensitivities are small (no more than unity).

Simulation Results and Discussion

To validate the theoretical analysis, the proposed universal filter in Figure 2.9 is simulated using ICAPS circuit simulation program. The CCCII± is modelled by the schematic implementation of Figure 1.15, proposed by Fabre et al. [36] with dc supply voltage of ±2.5V. The simulation results reported here were obtained using the transistors PR100N(PNP) and NR200N(NPN) of the bipolar arrays ALA400 from AT&T [67].

Figures 2.10 to 2.15 show the theoretical and simulation results of lowpass, highpass, bandpass, notch and allpass (gain and phase response) filters respectively. Lowpass, highpass and notch filter results are obatained for (1)24.48kHz and (2)244.8kHz frequencies. Bandpass filter is simulated for (1)50kHz and (2)244.8kHz center frequencies. Allpass filter results are obtained for (1)17.3kHz and (2)173.3kHz frequencies. It can be seen that the simulation results agree very well with the presented theory. Deviation less than 5% are obtained for these results. In short the

proposed circuit offers the following advantages.

- Arbitrary biquadratic transfer functions are realized with single input.
- With multiple outputs all the five basic filter functions can be obtained.
- Center frequency and bandwidth can be independently adjusted.
- No external resistances are used.
- Low active and passive sensitivities.

The disadvantage associated with this filter is that the high pass current is flowing through a capacitor. As a result the capacitor will be floating if this current needs to be sensed. Also the allpass transfer function requires matching condition. To remove these disadvantages another filter is proposed with some modifications.

2.3.3 Universal Filter 3

The proposed circuit is shown in Figure 2.16. It is a current-mode circuit using current controlled conveyor (CCCII) with internal resistance R_x. This filter has four multiple output CCCII, two grounded capacitors and no external resistances. Routine analysis of the circuit assuming ideal CCCII gives the following current transfer functions.

$$\frac{I_{LP}}{I_{in}} = \frac{R_{x_3}}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_1}R_{x_2}C_2s + R_{x_3}} \tag{2.27}$$

$$\frac{I_{HP}}{I_{in}} = \frac{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_1}R_{x_2}C_2s + R_{x_3}} \tag{2.28}$$

$$\frac{I_{BP_1}}{I_{in}} = \frac{R_{x_1}R_{x_2}C_2s}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_1}R_{x_2}C_2s + R_{x_3}} \tag{2.29}$$

$$\frac{I_{BP_2}}{I_{in}} = \frac{R_{x_2}R_{x_3}C_2s}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_1}R_{x_2}C_2s + R_{x_3}} \tag{2.30}$$

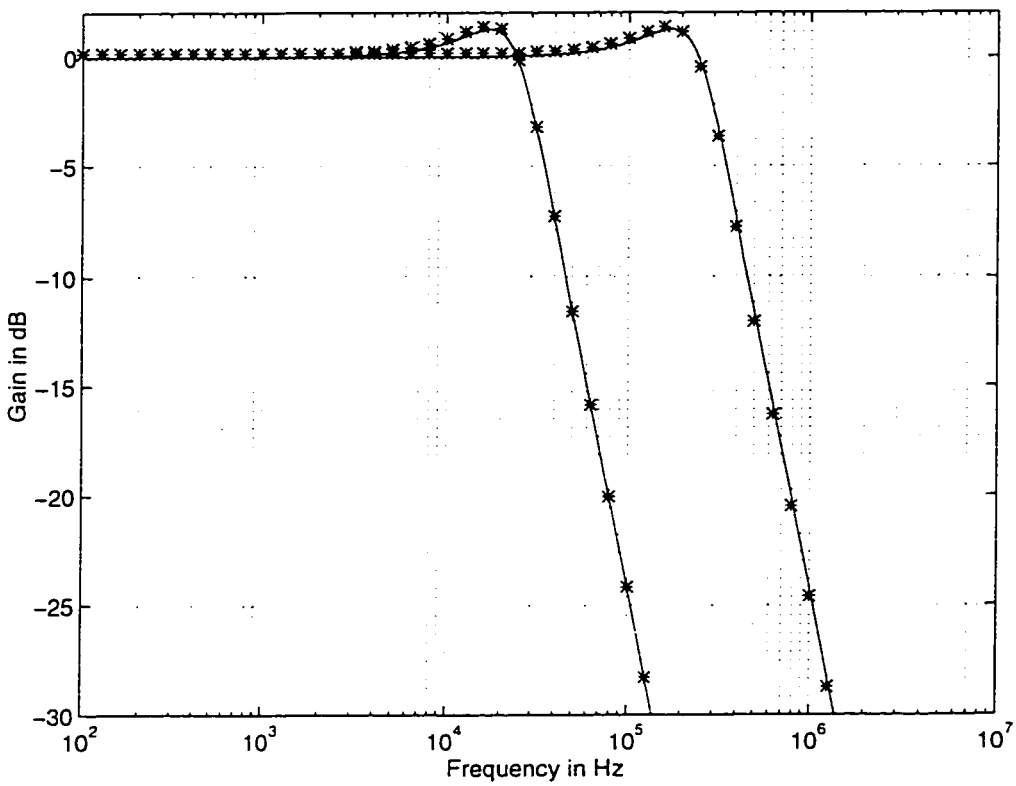


Figure 2.10: Simulation results of the lowpass filter. theoretical,***simulation (1) $I_2 = I_3 = 10\mu A, I_1 = 5\mu A, C_1 = C_2 = 5nF$ (2) $I_2 = I_3 = 100\mu A, I_1 = 50\mu A, C_1 = C_2 = 5nF$

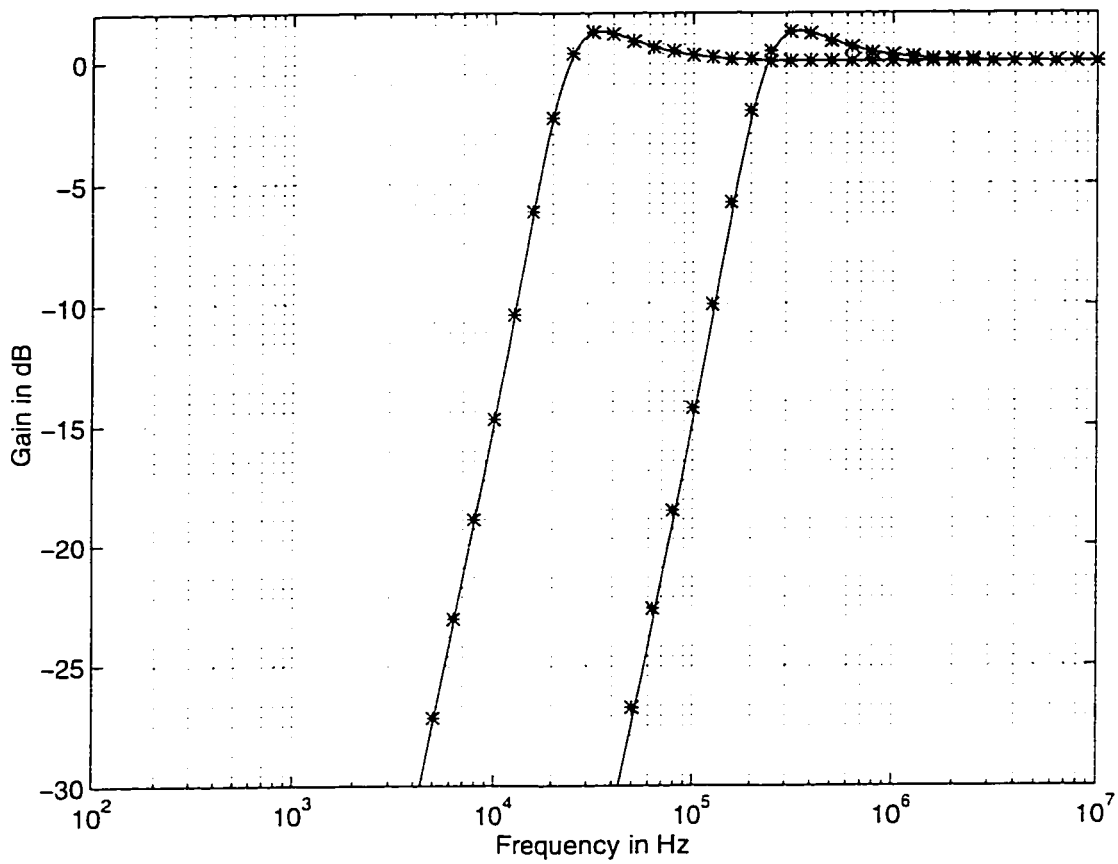


Figure 2.11: Simulation results of the high pass filter. theoretical,***simulation (1) $I_2 = I_3 = 10\mu A, I_1 = 5\mu A, C_1 = C_2 = 5nF$ (2) $I_2 = I_3 = 100\mu A, I_1 = 50\mu A, C_1 = C_2 = 5nF$

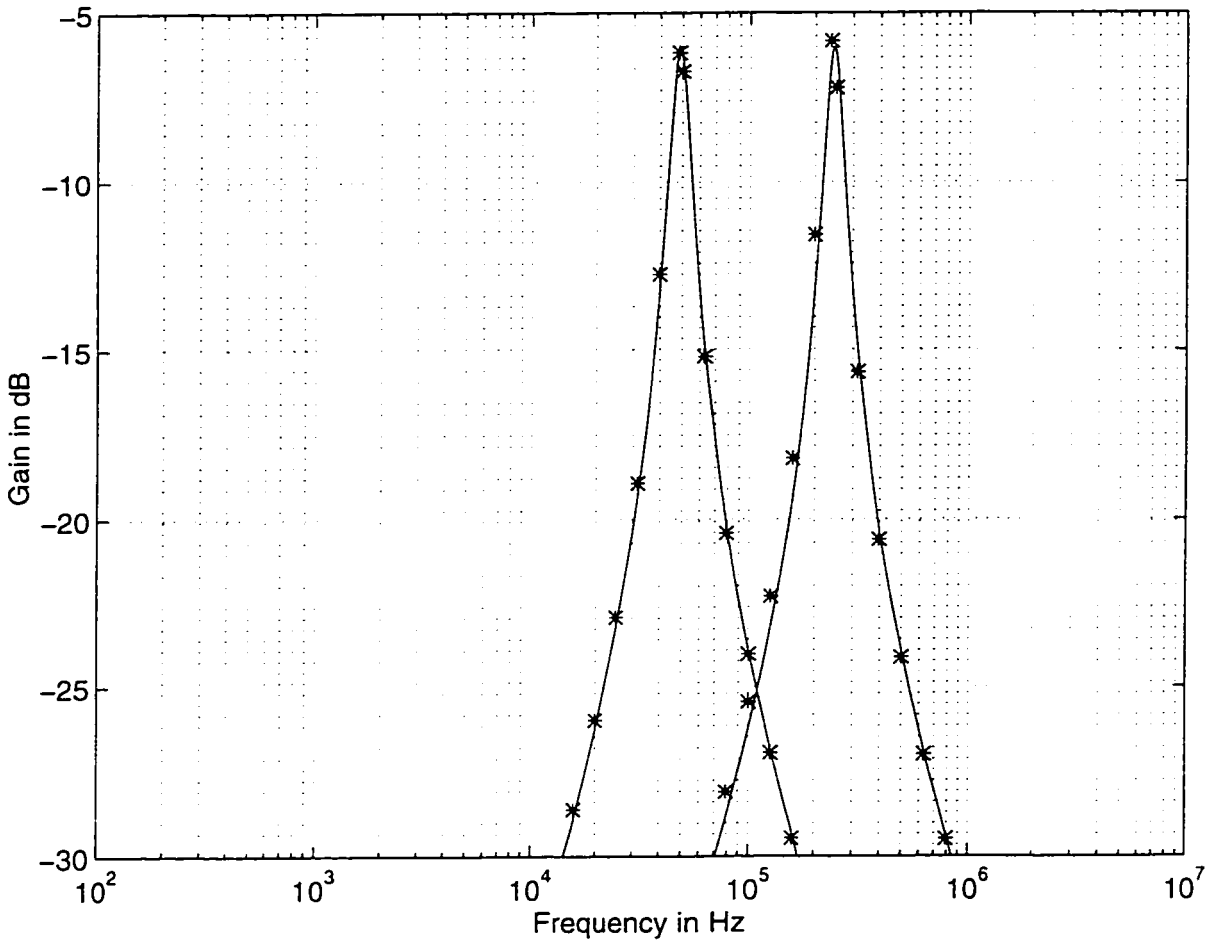


Figure 2.12: Simulation results of the bandpass filter. -theoretical,***simulation (1) $I_2 = I_3 = 20\mu A, I_1 = 2\mu A, C_1 = C_2 = 5nF$ (2) $I_2 = I_3 = 100\mu A, I_1 = 10\mu A, C_1 = C_2 = 5nF$

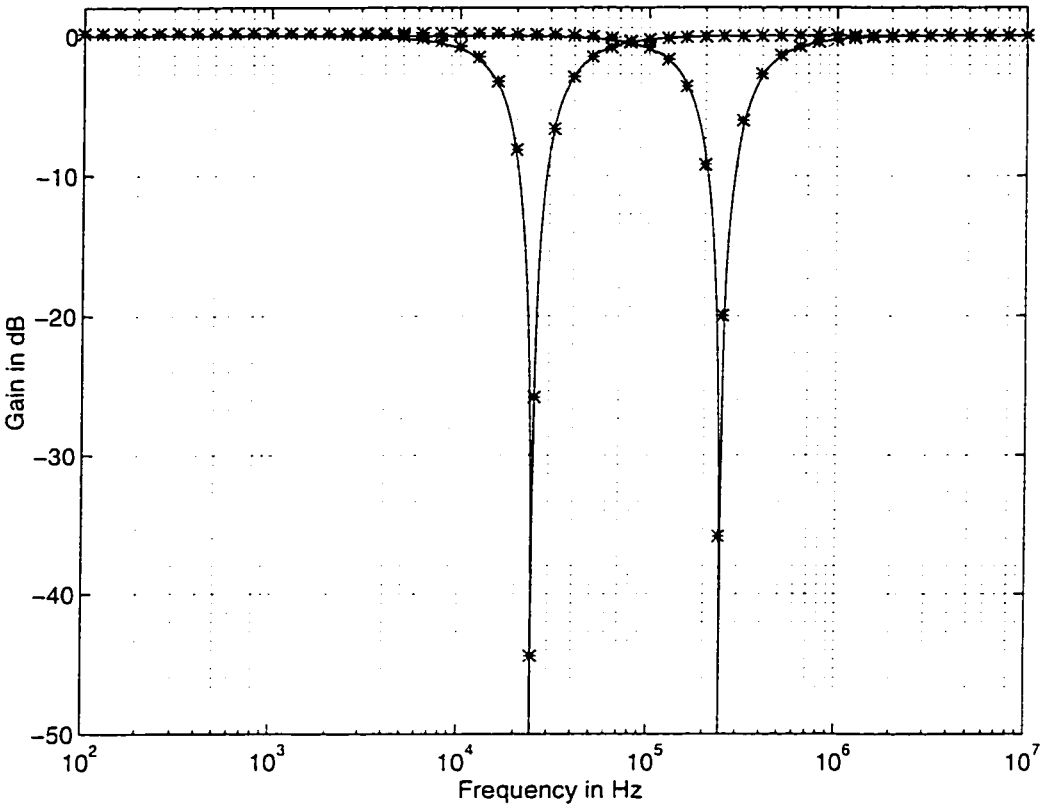


Figure 2.13: Simulation results of the notch filter. theoretical,***simulation (1) $I_2 = I_3 = 10\mu A, I_1 = 5\mu A, C_1 = C_2 = 5nF$ (2) $I_2 = I_3 = 100\mu A, I_1 = 50\mu A, C_1 = C_2 = 5nF$

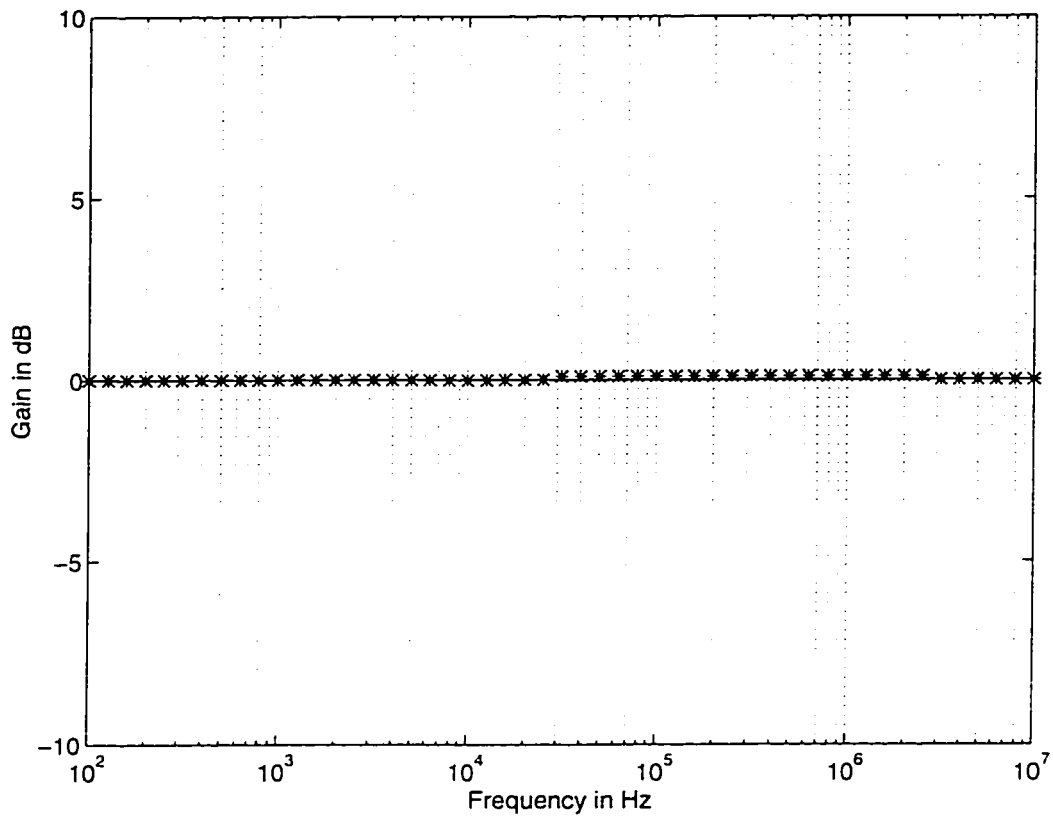


Figure 2.14: Simulation results of the gain of allpass filter. —theoretical, ***simulation. $I_2 = I_1 = 5\mu A, I_3 = 10\mu A, C_1 = C_2 = 5nF$

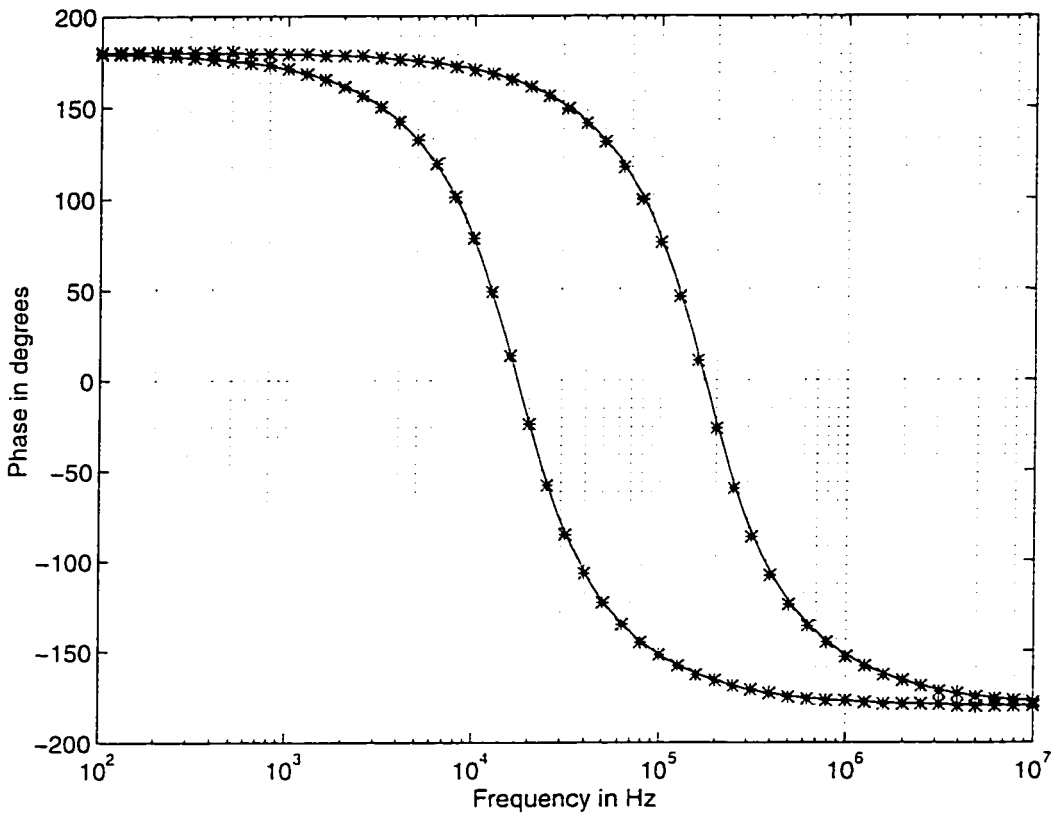


Figure 2.15: Simulation results of the phase of allpass filter. -theoretical, ***simulation (1) $I_2 = I_1 = 5\mu A, I_3 = 10\mu A, C_1 = C_2 = 5nF$ (2) $I_2 = I_1 = 50\mu A, I_3 = 100\mu A, C_1 = C_2 = 5nF$

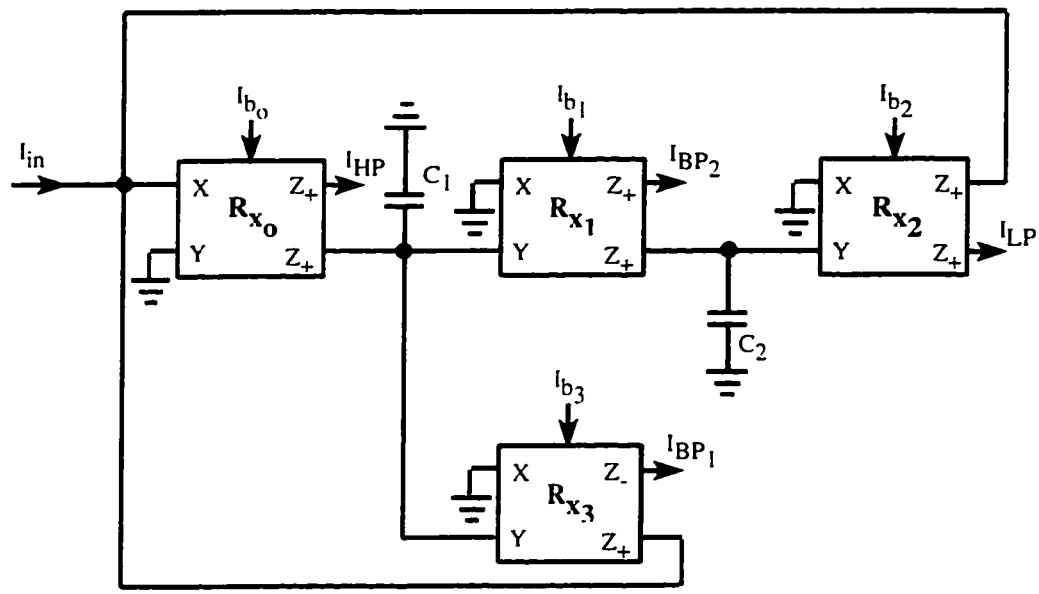


Figure 2.16: Improved CCCII based Universal second order filter-3.

A current mode notch signal is easily obtained by connecting the I_{HP} and I_{LP} output terminals. Let $I_{NH} = I_{HP}+I_{LP}$, we obtain the current-mode notch transfer function as,

$$\frac{I_{NH}}{I_{in}} = \frac{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_3}}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_1}R_{x_2}C_2s + R_{x_3}} \tag{2.31}$$

Similarly by connecting the I_{HP}, I_{BP_1} and I_{LP} output terminals, a current mode allpass response is obtained

$$\frac{I_{AP}}{I_{in}} = \frac{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 - R_{x_1}R_{x_2}C_2s + R_{x_3}}{R_{x_1}R_{x_2}R_{x_3}C_1C_2s^2 + R_{x_1}R_{x_2}C_2s + R_{x_3}} \tag{2.32}$$

The center frequency w_o, bandwidth w_o/Q_o and quality factor Q_o are given by,

$$w_o = \sqrt{\frac{1}{R_{x_1}R_{x_2}C_1C_2}} \tag{2.33}$$

$$\frac{w_o}{Q_o} = \frac{1}{R_{x_3}C_1} \tag{2.34}$$

$$Q_o = R_{x_3}\sqrt{\frac{C_1}{R_{x_1}R_{x_2}C_2}} \tag{2.35}$$

Gain of high pass, lowpass and bandpass are approximately given by,

$$G_{LP} = G_{HP} = G_{BP_1} = 1 \ , \ G_{BP_2} = \frac{R_{x_3}}{R_{x_1}} \tag{2.36}$$

It can be seen from equations (2.33) and (2.34) that the center frequency can be adjusted without disturbing the bandwidth. The center frequency w_o can be electronically tuned by adjusting I_{b_2},whereas the bandwidth w_o/Q_o can be separately adjusted by trimming I_{b_3} without disturbing w_o. Another important advantage is that no matching condition is required for the realization of allpass and notch functions. Also the proposed filter uses two grounded capacitors which can absorb the stray capacitances. This will result in high frequency operation and less silicon area for implementation. So the disadvantages associated with the previous two circuits are removed.

Sensitivity Analysis

Nonideal analysis is required to find the active sensitivities of the filter. Assuming that the nonideal port relations of the CCCII can be expressed as $v_x = \beta v_y + i_x R_x, i_z = \alpha i_x$, where $\alpha = 1 - \delta$ ($|\delta| \ll 1$) denotes the current tracking error, $\beta = 1 - \epsilon$ ($|\epsilon| \ll 1$) represents the voltage traking error. The output current can now be expressed as,

$$\frac{I_{LP}}{I_{in}} = \frac{\alpha_o \alpha_1 \beta_1 \beta_2 R_{x_3}}{R_{x_1} R_{x_2} R_{x_3} C_1 C_2 s^2 + \alpha_o \alpha_3 \beta_3 R_{x_1} R_{x_2} C_2 s + \alpha_o \alpha_1 \alpha_2 \beta_1 \beta_2 R_{x_3}} \tag{2.37}$$

$$\frac{I_{HP}}{I_{in}} = \frac{R_{x_1} R_{x_2} R_{x_3} C_1 C_2 s^2}{R_{x_1} R_{x_2} R_{x_3} C_1 C_2 s^2 + \alpha_o \alpha_3 \beta_3 R_{x_1} R_{x_2} C_2 s + \alpha_o \alpha_1 \alpha_2 \beta_1 \beta_2 R_{x_3}} \tag{2.38}$$

$$\frac{I_{BP_1}}{I_{in}} = \frac{\alpha_o \beta_3 R_{x_1} R_{x_2} C_2 s}{R_{x_1} R_{x_2} R_{x_3} C_1 C_2 s^2 + \alpha_o \alpha_3 \beta_3 R_{x_1} R_{x_2} C_2 s + \alpha_o \alpha_1 \alpha_2 \beta_1 \beta_2 R_{x_3}} \tag{2.39}$$

$$\frac{I_{BP_2}}{I_{in}} = \frac{\alpha_o \beta_1 R_{x_2} R_{x_3} C_2 s}{R_{x_1} R_{x_2} R_{x_3} C_1 C_2 s^2 + \alpha_o \alpha_3 \beta_3 R_{x_1} R_{x_2} C_2 s + \alpha_o \alpha_1 \alpha_2 \beta_1 \beta_2 R_{x_3}} \tag{2.40}$$

The center frequency w_o, bandwidth w_o/Q_o and quality factor Q_o are given by,

$$w_o = \sqrt{\frac{\alpha_o\alpha_1\alpha_2\beta_1\beta_2}{R_{x_1}R_{x_2}C_1C_2}} \tag{2.41}$$

$$\frac{w_o}{Q_o} = \frac{\alpha_o\alpha_3\beta_3}{R_{x_3}C_1} \tag{2.42}$$

$$Q_o = \frac{R_{x_3}}{\alpha_3\beta_3}\sqrt{\frac{\alpha_1\alpha_2\beta_1\beta_2C_1}{\alpha_oR_{x_1}R_{x_2}C_2}} \tag{2.43}$$

From equations (2.41) and (2.43) it is easy to show that the active and passive sensitivities of the parameters w_o and Q_o are,

$$S_{\alpha_o}^{w_o} = S_{\alpha_1}^{w_o} = S_{\alpha_2}^{w_o} = S_{\beta_1}^{w_o} = S_{\beta_2}^{w_o} = \frac{1}{2}\ ,\ S_{\alpha_3}^{w_o} = S_{\beta_o}^{w_o} = S_{\beta_3}^{w_o} = 0$$

$$S_{R_{x_1}}^{w_o} = S_{R_{x_2}}^{w_o} = S_{C_1}^{w_o} = S_{C_2}^{w_o} = -\frac{1}{2}\ ,\ S_{R_{x_3}}^{w_o} = 0$$

$$S_{\alpha_o}^{Q_o} = S_{\alpha_1}^{Q_o} = S_{\alpha_2}^{Q_o} = S_{\beta_1}^{Q_o} = S_{\beta_2}^{Q_o} = \frac{1}{2}\ ,\ S_{\alpha_3}^{Q_o} = S_{\beta_3}^{Q_o} = -1\ ,\ S_{\beta_o}^{Q_o} = 0$$

$$-S_{R_{x_1}}^{Q_o} = -S_{R_{x_2}}^{Q_o} = S_{C_1}^{Q_o} = -S_{C_2}^{Q_o} = \frac{1}{2}\ ,\ S_{R_{x_3}}^{Q_o} = 1\ ,\ S_{C_1}^{Q_o} = \frac{1}{2}$$

All of the active and passive sensitivities are small (no more than unity).

Simulation Results and Discussion

To validate the theoretical analysis, the proposed universal filter in Figure 2.16 is simulated using ICAPS circuit simulation program. The CCCII± is modelled by the schematic implementation of Figure 1.15, proposed by Fabre et al. [36] with dc supply voltage of ±2.5V. The filter characteristics here were obtained using the transistors PR100N(PNP) and NR200N(NPN) of the bipolar arrays ALA400 from AT&T [67].

Figures 2.17 to 2.22 show the theoretical and simulation results of lowpass, highpass, bandpass, notch and allpass (gain and phase response) filters respectively. Lowpass, highpass, notch and allpass filters are simulated for (1)24.48kHz

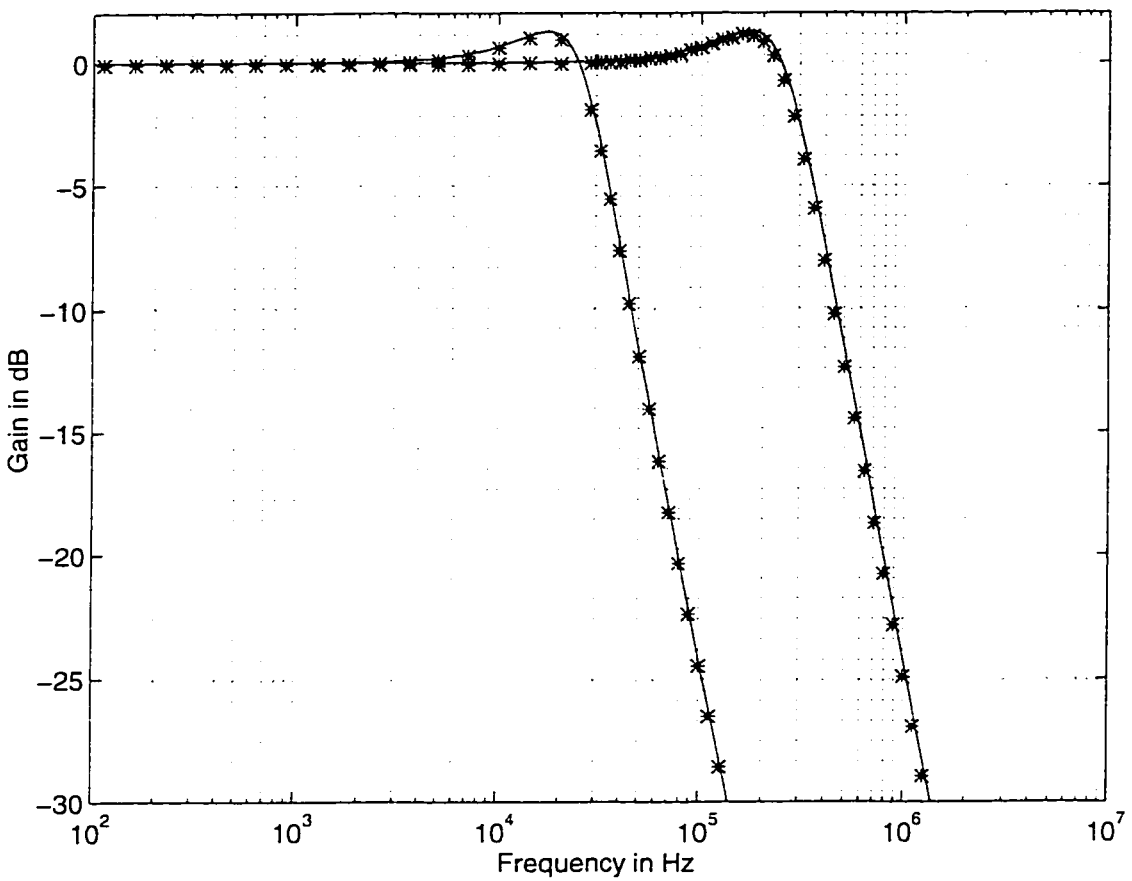


Figure 2.17: Simulation results of the lowpass filter. —theoretical,***simulation (1) $I_o = 100\mu A, I_1 = I_2 = I_3 = 10\mu A, C_1 = C_2 = 5nF$ (2) $I_o = 100\mu A, I_1 = I_2 = I_3 = 100\mu A, C_1 = C_2 = 5nF$

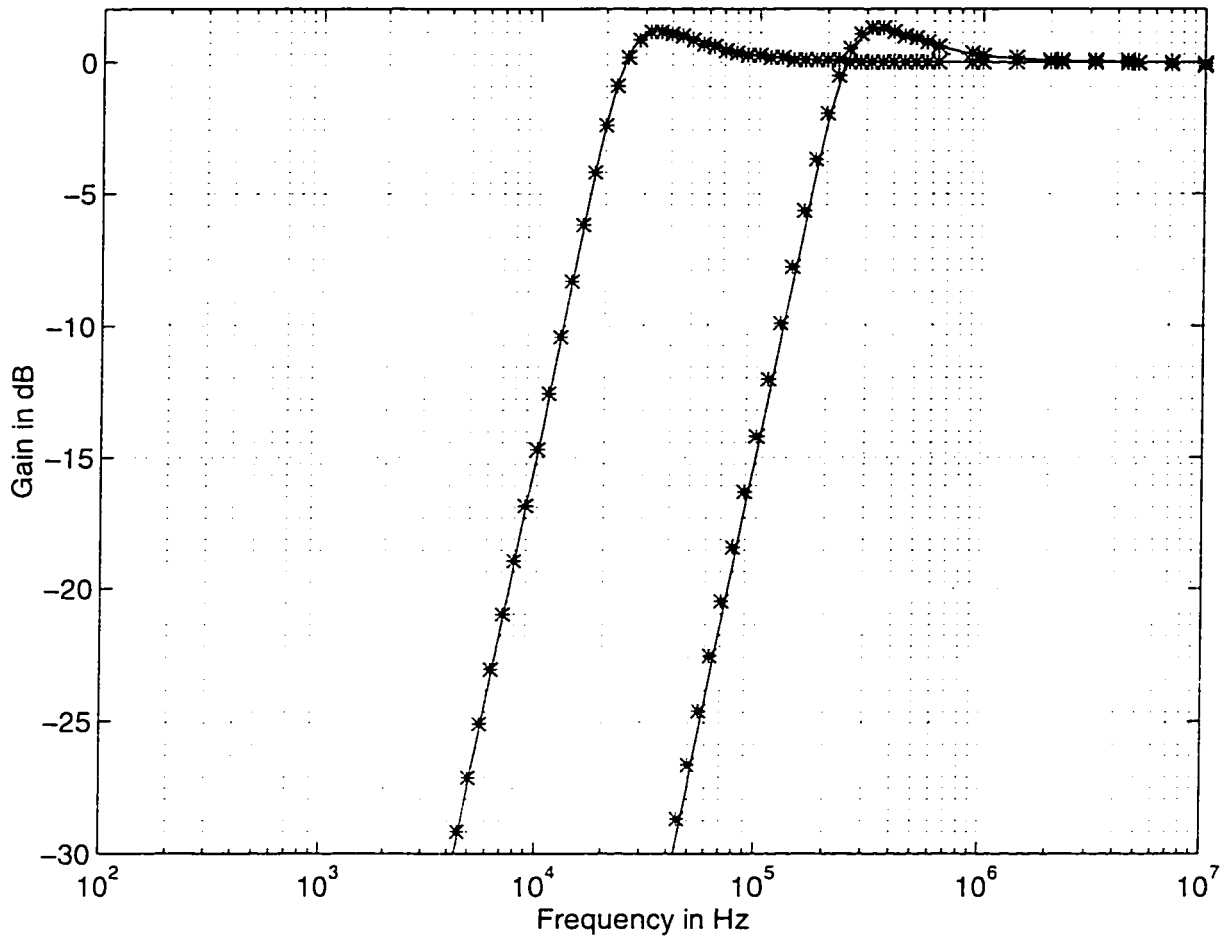


Figure 2.18: Simulation results of the highpass filter. theoretical.***simulation (1) $I_o = 100\mu A, I_1 = I_2 = I_3 = 10\mu A, C_1 = C_2 = 5nF$ (2) $I_o = 100\mu A, I_1 = I_2 = I_3 = 100\mu A, C_1 = C_2 = 5nF$

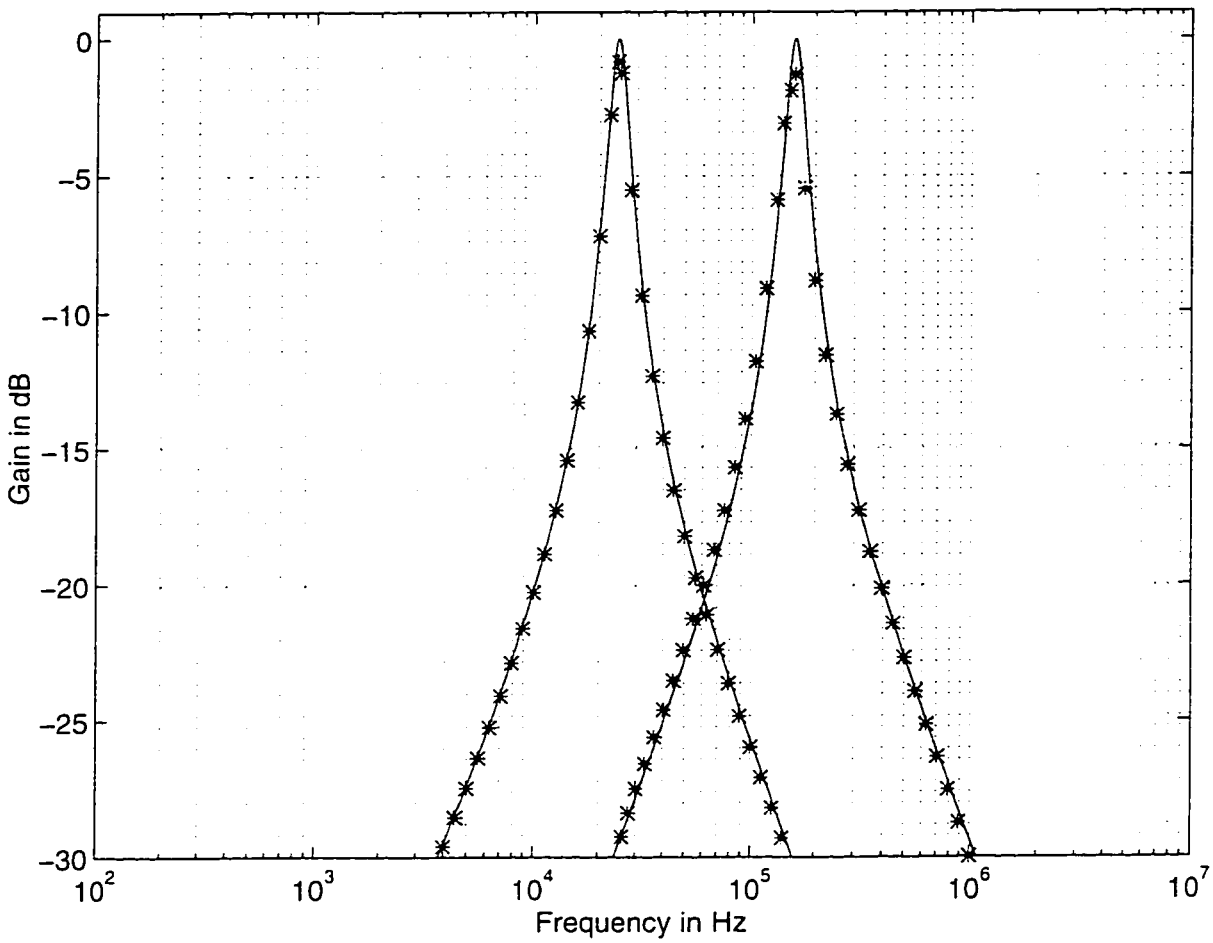


Figure 2.19: Simulation results of the bandpass filter. theoretical, ***simulation (1) $I_o = 100\mu A, I_1 = I_2 = 10\mu A, I_3 = 2\mu A, C_1 = C_2 = 5nF$ (2) $I_o = 100\mu A, I_1 = 10\mu A, I_2 = 520\mu A, I_3 = 15\mu A, C_1 = C_2 = 5nF$

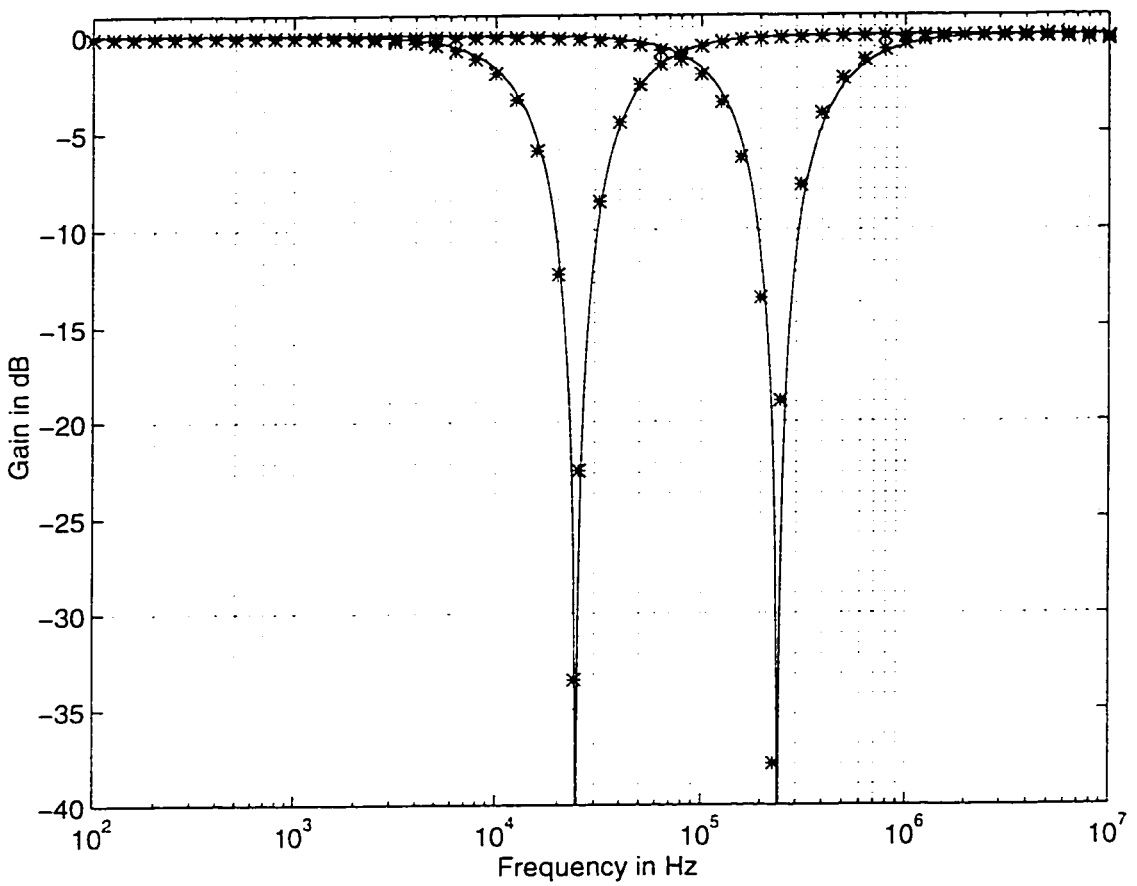


Figure 2.20: Simulation results of the notch filter. theoretical. ***simulation (1) $I_o = 100\mu A, I_1 = I_2 = 10\mu A, I_3 = 14.14\mu A, C_1 = C_2 = 5nF$ (2) $I_o = 100\mu A, I_1 = I_2 = 100\mu A, I_3 = 141.4, \mu A, C_1 = C_2 = 5nF$

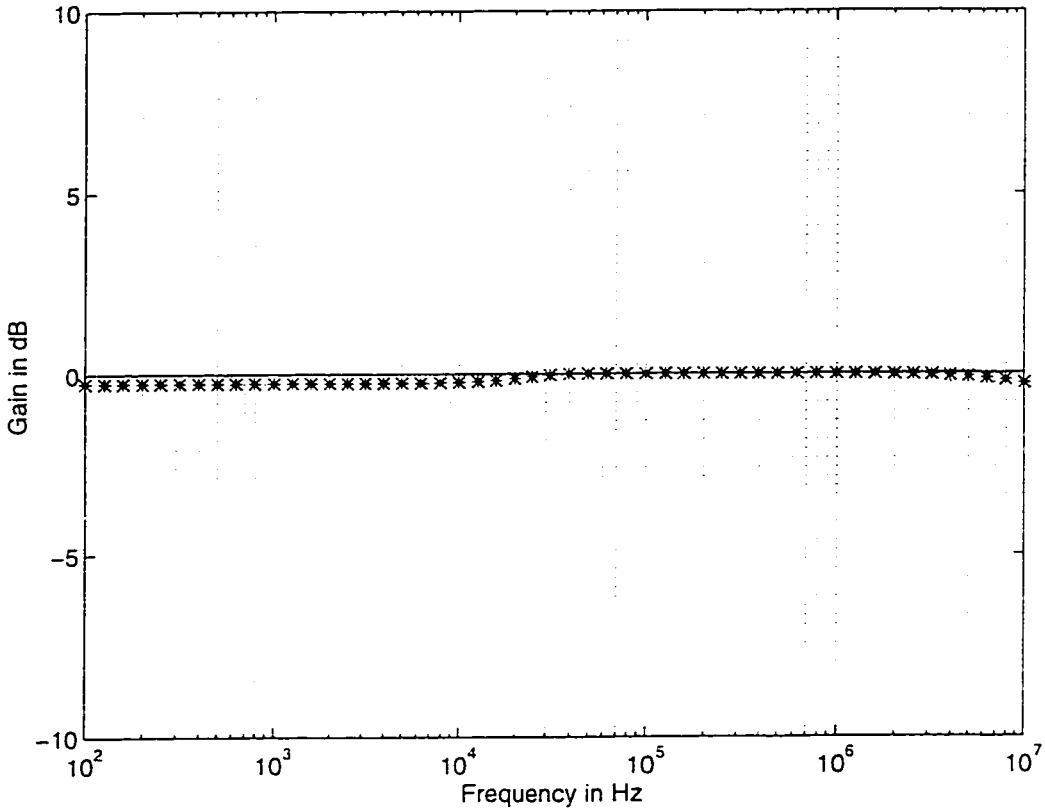


Figure 2.21: Simulation results of the gain of allpass filter. theoretical, ***simulation. $I_o = 100\mu A, I_1 = I_2 = 10\mu A, I_3 = 14.14\mu A, C_1 = C_2 = 5nF$

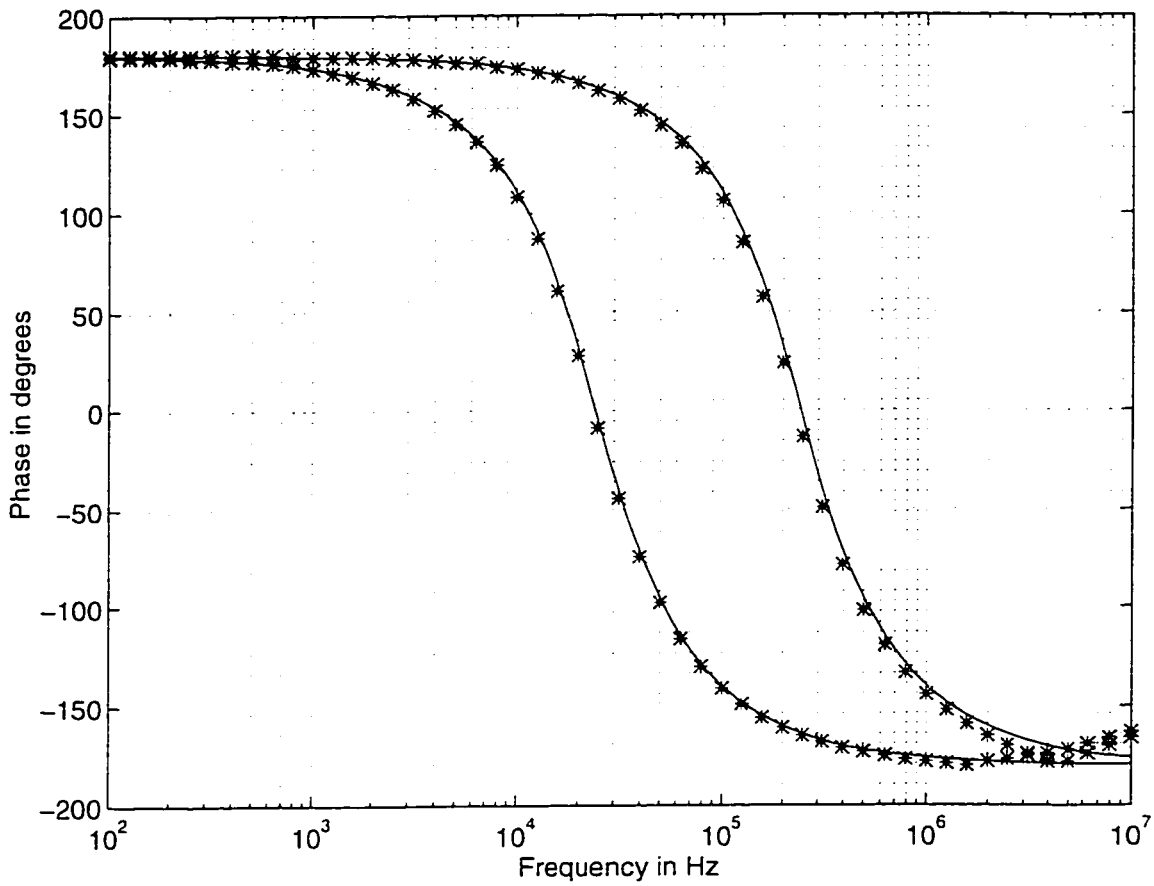


Figure 2.22: Simulation results of the phase of allpass filter. - theoretical, ***simulation (1) $I_o = 100\mu A, I_1 = I_2 = 10\mu A, I_3 = 14.14\mu A, C_1 = C_2 = 5nF$ (2) $I_o = 100\mu A, I_1 = I_2 = 100\mu A, I_3 = 141.4\mu A, C_1 = C_2 = 5nF$

and (2)244.8kHz frequencies. Bandpass filter is simulated for (1)24.48kHz and (2)176.56kHz frequencies. It can be seen that the simulation results agree very well with the presented theory. Deviation less than 5% are obtained for these results. In short the proposed circuit offers the following advantages.

- Arbitrary biquadratic transfer functions are realized with single input.
- With multiple outputs all the five basic filter functions can be obtained.
- Center frequency w_o and bandwidth w_o/Q_o can be independently adjusted.
- No external resistances are used.
- grounded capacitors are used.
- No matching conditions are required for the realization of allpass and notch transfer functions.
- Low active and passive sensitivities.

To show the merits and demerits of the proposed filter designs, Table 2.1 shows a comparison with the most recently published CCCII programmable current mode universal filter [50]. Comparison shows that the proposed filter is a better option for universal filter as it uses grounded capacitors and can realize all five transfer functions without any realization conditions.

2.3.4 Universal Filter 4

A new interesting universal filter can be obtained by connecting two more multiple output current controlled conveyors in parallel to the CCCII-0 and CCCII-2. The

	Universal Filter 1997[50]	Proposed CCCII Filter 1	Proposed CCCII Filter 3
w_o and w_o/Q_o relation	Independent	Dependent	Independent
No. of active elements	Five	Four	Four
No. of capacitors	Two	Two	Two
No. of floating capacitors	Two	One	None
Controlling w_o	Biasing current	Biasing current	Biasing current
Controlling w_o/Q_o	Biasing current	--	Biasing current
Active/passive sensitivity	Low	Low	Low
Notch/allpass functions	Not realizable	Realizable	Realizable
Realization conditions		None	None

Table 2.1: Comparison between the proposed CCCII unviersal filters and the previously published filter.

resulting circuit is shown in Figure 2.23. Routine analysis of the circuit assuming ideal CCCII gives the following current transfer functions.

$$\frac{I_{LP_1}}{I_{in}} = \frac{R_{x_4}}{R_{x_2}R_{x_3}R_{x_4}C_1C_2s^2 + R_{x_2}R_{x_3}C_2s + R_{x_4}} \tag{2.44}$$

$$\frac{I_{LP_2}}{I_{in}} = \frac{I_{LP_3}}{I_{in}} = \frac{R_{x_3}}{R_{x_6}}I_{LP_1} \tag{2.45}$$

$$\frac{I_{HP_1}}{I_{in}} = \frac{R_{x_2}R_{x_3}R_{x_4}C_1C_2s^2}{R_{x_2}R_{x_3}R_{x_4}C_1C_2s^2 + R_{x_2}R_{x_3}C_2s + R_{x_4}} \tag{2.46}$$

$$\frac{I_{HP_2}}{I_{in}} = -\frac{I_{HP_3}}{I_{in}} = \frac{R_{x_1}}{R_{x_5}}I_{HP_1} \tag{2.47}$$

$$\frac{I_{BP_1}}{I_{in}} = \frac{R_{x_2}R_{x_3}C_2s}{R_{x_2}R_{x_3}R_{x_4}C_1C_2s^2 + R_{x_2}R_{x_3}C_2s + R_{x_4}} \tag{2.48}$$

$$\frac{I_{BP_2}}{I_{in}} = \frac{R_{x_3}R_{x_4}C_2s}{R_{x_2}R_{x_3}R_{x_4}C_1C_2s^2 + R_{x_2}R_{x_3}C_2s + R_{x_4}} \tag{2.49}$$

The gains of these transfer functions are approximately given by,

$$G_{LP_1} = G_{HP_1} = G_{BP_1} = 1.\ G_{LP_2} = G_{LP_3} = \frac{R_{x_3}}{R_{x_6}}, \tag{2.50}$$

$$G_{HP_2} = -G_{HP_1} = \frac{R_{x_1}}{R_{x_5}},\ G_{BP_2} = \frac{R_{x_4}}{R_{x_2}} \tag{2.51}$$

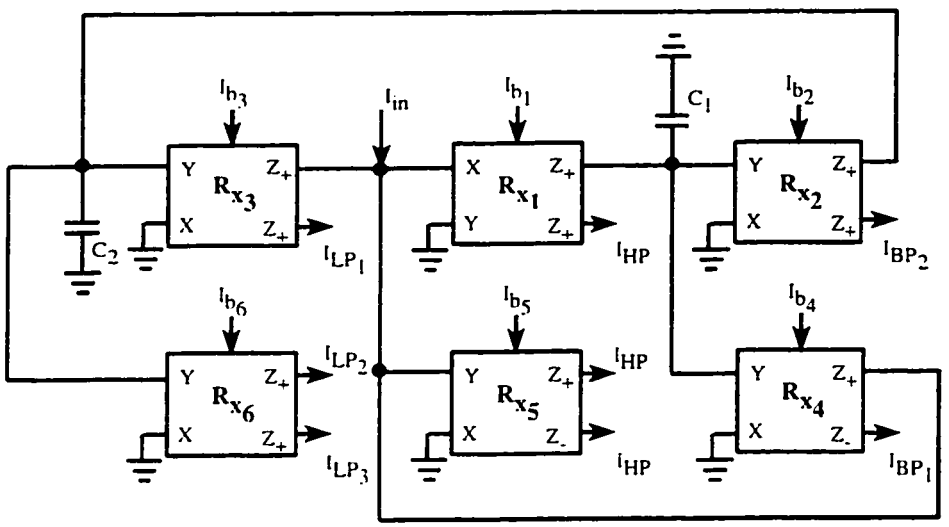


Figure 2.23: Multiple filter functions. CCCII based Universal second order filter-4.

The outputs of I_{LP_2}, I_{HP_2} and I_{BP_2} can be used for lowpass, highpass and bandpass filters with adjustable gain. The outputs of I_{LP_1}, I_{HP_1} and I_{BP_1} can be connected together for allpass response with a gain of unity and without any matching conditions. The outputs of I_{LP_3} and I_{HP_3} can be connected together to get the notch function with adjustable gain. In this way all the five basic transfer functions are available simultaneously.

The center frequency ω_o, bandwidth ω_o/Q_o and quality factor Q_o are given by,

$$\omega_o = \sqrt{\frac{1}{R_{x_2}R_{x_3}C_1C_2}} \tag{2.52}$$

$$\frac{\omega_o}{Q_o} = \frac{1}{R_{x_4}C_1} \tag{2.53}$$

$$Q_o = R_{x_4}\sqrt{\frac{C_1}{R_{x_2}R_{x_3}C_2}} \tag{2.54}$$

It can be seen that the center frequency and bandwidth are independently adjustable. In addition to all the advantages available in the previous filter such as grounded capacitors, no matching conditions, low sensitivity etc. this filter has

some more advantages. The gain of lowpass, highpass and notch is independently adjustable by R_{x_6} and R_{x_5} respectively. The gain of bandpass filter is orthogonally adjustable. All five functions are simultaneously available.

Simulation Results and Discussion

To validate the theoretical analysis, the proposed universal filter is simulated using ICAPS circuit simulation program. The CCCII± is modelled by the schematic implementation of Figure 1.15, proposed by Fabre et al. [36] with dc supply voltage of ±2.5V. The filter characteristics here were obtained using the transistors PR100N(PNP) and NR200N(NPN) of the bipolar arrays ALA400 from AT&T [67].

Figures 2.24 to 2.26 show the theoretical and simulation results of lowpass, highpass, bandpass, notch and allpass (gain and phase response) filters respectively. It can be seen that the simulation results agree very well with the presented theory.

2.4 SINUSOIDAL OSCILLATORS

An oscillator circuit generates some form of time-varying output. Most electronic systems use an oscillator of some form. Probably the most frequently encountered type of oscillator, however is the sine wave generator. Audio test signals, radio frequency carriers and communication signals of many types are sine waves. In most cases, the amplitude of the generated sine wave is limited automatically by the nonlinear characteristics of the active devices involved. However, sometimes a separate circuit is added to perform amplitude limitation.

For any circuit to oscillate and produce a true or perfect sine wave output, three requirements must be satisfied.

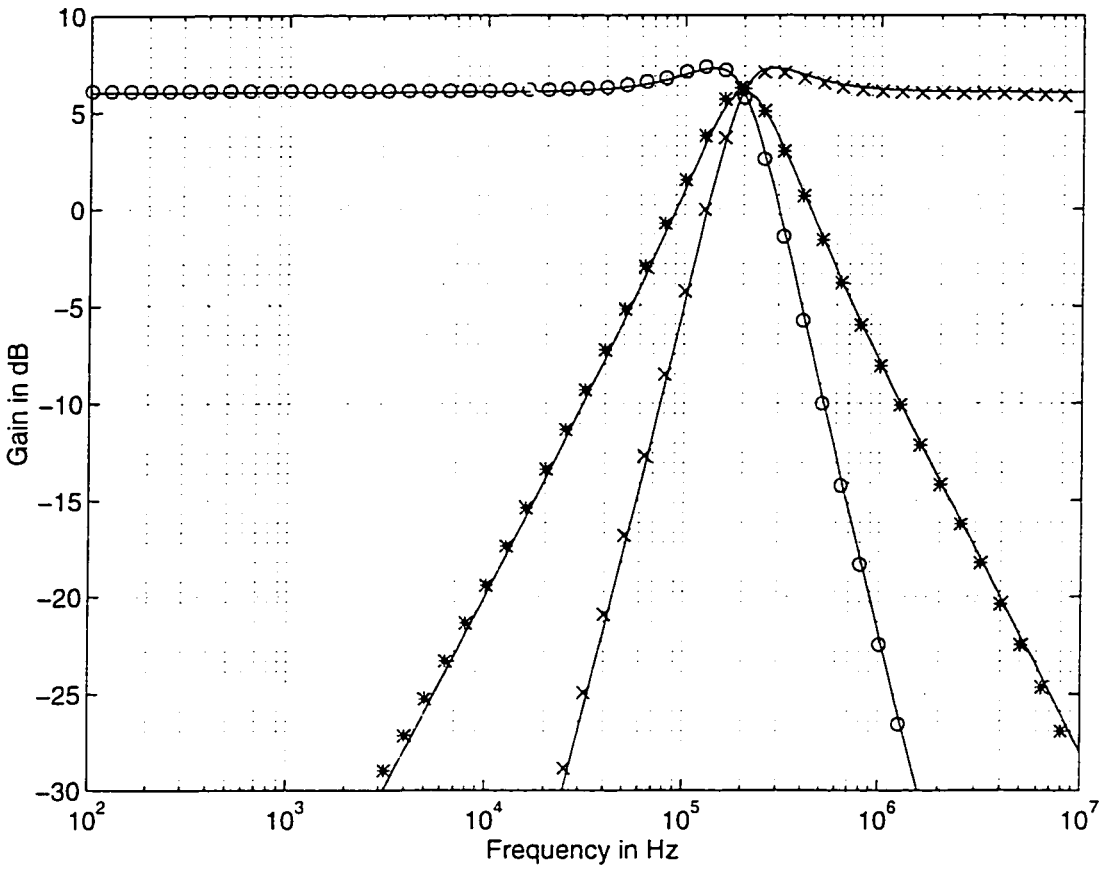


Figure 2.24: Simulation results of bandpass, lowpass and highpass filter.

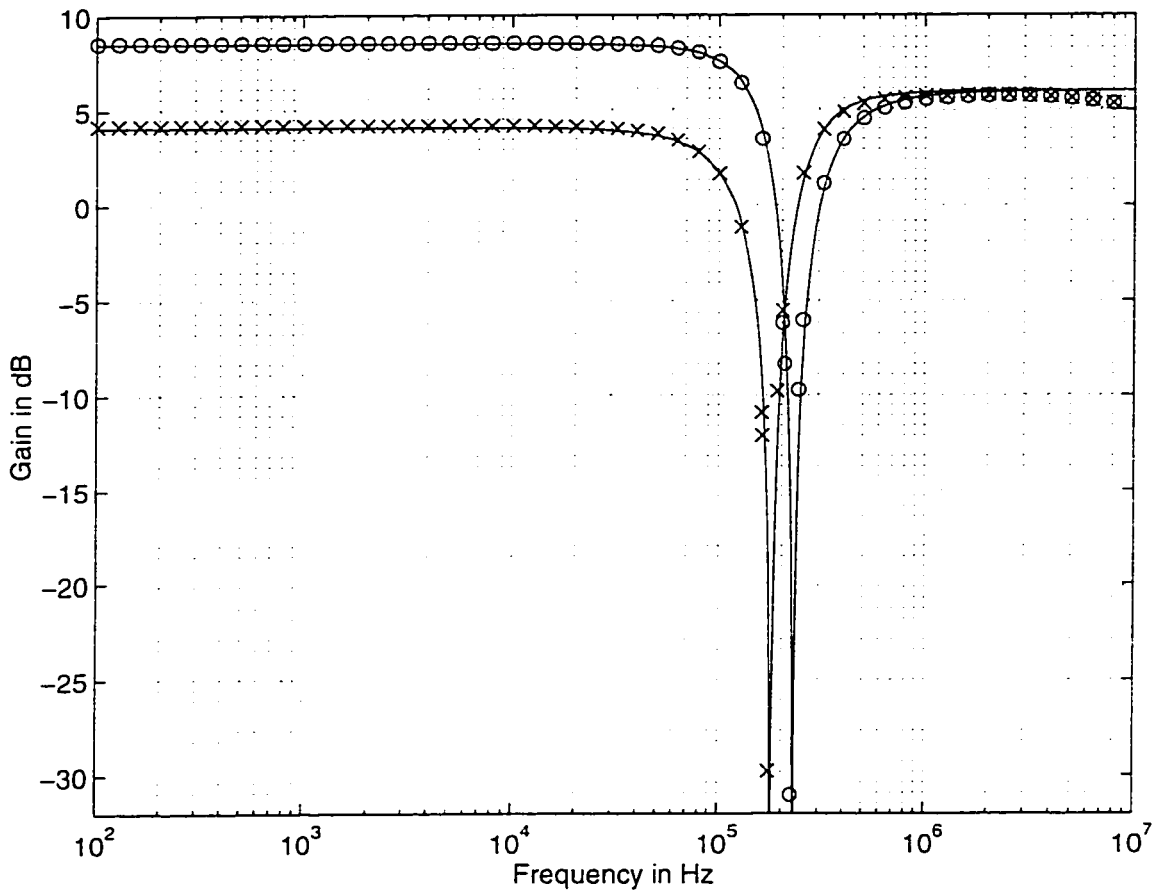


Figure 2.25: Simulation results of lowpass notch and highpass notch filter.

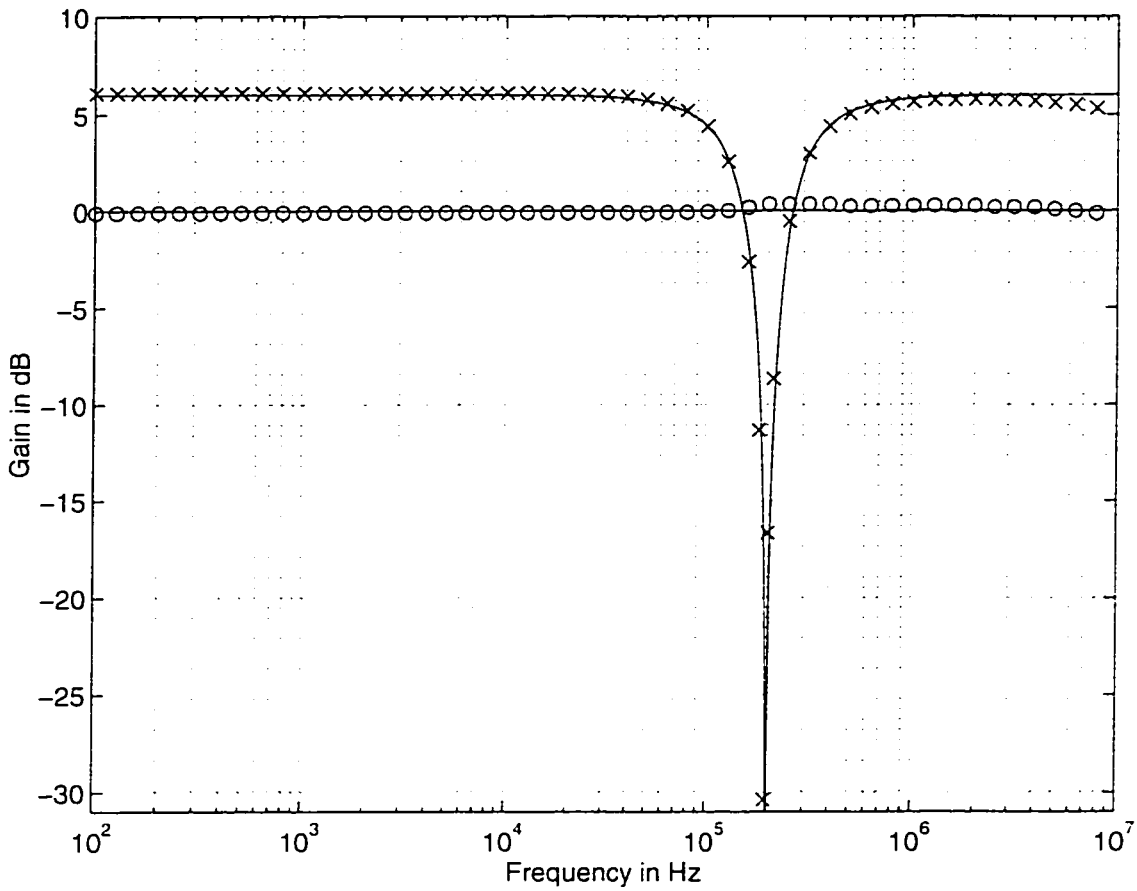


Figure 2.26: Simulation results of the gain of allpass and notch filter.

- There must be positive feedback in the circuit.
- The product of feedback factor and the circuit open loop gain must be exactly unity.
- There must be some frequency selection network in the circuit such that a 0 (or 360) phase shift occurs for only one frequency.

These conditions are known as Barkhausen criteria [68].

Over the years sinusoidal oscillators were designed using active integrated circuits such as the operational amplifier, current conveyor and the operational transconductance amplifier (OTA). Among these OTA has the advantage of programmability. Now the controlled conveyor is a better option because of its low supply voltage, low power consumption and improved performance.

2.4.1 Design Requirements

A sinusoidal oscillator should be designed by taking into consideration the following requirements.

- The frequency of oscillation (ω_o) and the condition of oscillation (C.O.) should be independently adjustable. (C.O. can be used to change the amplitude of the output).
- Use of grounded capacitors to overcome the effect of stray capacitance.
- It is advantageous if the oscillation frequency and condition of oscillation are programmable.
- Minimum number of active and passive components.

- The sensitivity of frequency of oscillation to passive and active components should be low (less than unity).

2.4.2 Proposed Circuit

So far there are not many circuits available using current controlled conveyor. Only two circuits are available in the literature that use current controlled conveyor for sinusoidal oscillator and both are proposed by Kiranon et al. [57][50]. The first circuit has the disadvantage that the condition of oscillation and the frequency of oscillation are not independently controllable and the second circuit needs another current conveyor for sensing the output current.

The proposed sinusoidal oscillator is shown in Figure 2.27. It consists of three current controlled conveyors (CCCII), two grounded capacitors and no external resistances. Assuming an ideal CCCII+ ($v_x = v_y + i_x R_x$, $i_z = i_x$ where $R_x = V_T/(2I_o)$), routine analysis shows that the characteristic equation of the circuit can be expressed as,

$$s^2 R_{x_1} R_{x_2} R_{x_3} C_1 C_2 + s R_{x_2}(R_{x_3} - R_{x_1}) C_2 + R_{x_3} = 0 \tag{2.55}$$

Using the Barkhausen principle, equating the imaginary and real parts of equation (2.55) to zero, the frequency of oscillation and the condition of oscillation can be expressed as,

$$w_o^2 = \frac{1}{R_{x_1} R_{x_2} C_1 C_2} \tag{2.56}$$

and

$$R_{x_3} = R_{x_1} \tag{2.57}$$

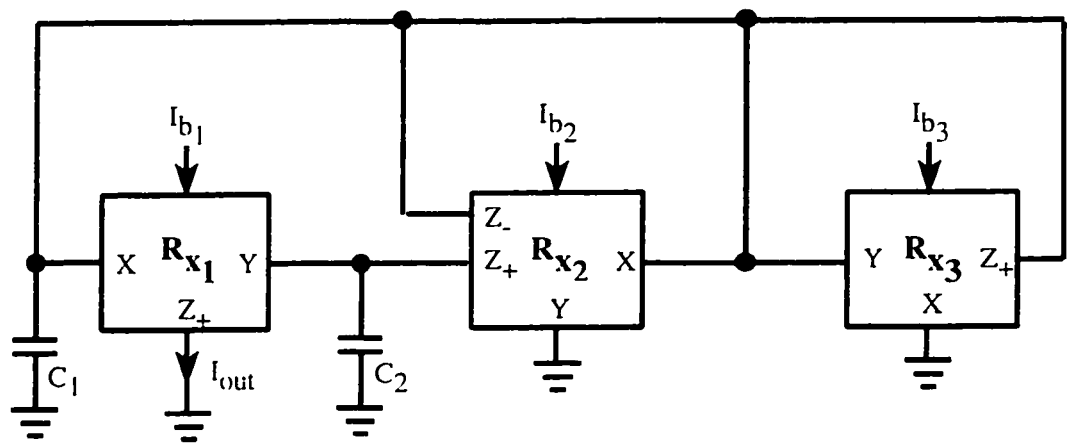


Figure 2.27: Circuit diagram for proposed sinusoidal oscillator.

Replacing internal resistance R_x by its equivalent expression, equations (2.56) and (2.57) can be expressed as,

$$w_o^2 = \frac{4I_{b_1}I_{b_2}}{V_T^2 C_1 C_2} \tag{2.58}$$

and

$$I_{b_1} = I_{b_1} \tag{2.59}$$

From equations (2.58) and (2.59) it can be seen that the frequency of oscillation can be controlled by adjusting the bias current I_{b_2} without disturbing the condition of oscillation, while the condition of oscillation can be controlled by adjusting the bias current I_{b_1}, without disturbing the frequency of oscillation. Output current I_{out} is available at a high impedance node. Moreover, by defining the sensitivity of the frequency of oscillation w_o to the parameter F by,

$$S_F^{w_o} = \frac{dw_o}{dF}\frac{F}{w_o}$$

the different sensitivities of w_o, are given by,

$$S_{C_1}^{w_o} = S_{C_2}^{w_o} = -S_{I_{b_1}}^{w_o} = -S_{I_{b_2}}^{w_o} = -\frac{1}{2}, S_{V_T}^{w_o} = -1 \tag{2.60}$$

Thus the proposed circuit enjoys low active and passive sensitivities.

2.4.3 Simulation Results and Discussion

To validate the theoretical analysis, the proposed universal filter in Figure 2.27 is simulated using ICAPS circuit simulation program. The CCCII± is modelled by the schematic implementation of Figure 1.15, proposed by Fabre et al. [36] with dc supply voltage of ±2.5V. The oscillator characteristics here are obtained using the transistors PR100N(PNP) and NR200N(NPN) of the bipolar arrays ALA400 from AT&T [67].

The oscillator circuit is simulated for a frequency of $612kHz$, by using $C_1 = C_2 = 2nF$ and $I_{b_1} = I_{b_2} = 100\mu A$. To ensure the start of the oscillation it is essential to have I_{b_1} slightly greater than I_{b_1}. This condition is attributed to the nonideal characteristics of the transistors used to simulate the current conveyors. The simulation result is shown in Figure 2.28. It gives an error of less than 3%. The plot of the simulated oscillation frequencies against the bias current is shown in Figure 2.29. The deviation in oscillation frequency for large values of current occurs due to the β error and the frequency limitation of the transistor models. The error can be reduced if improved high frequency models of transistor are used.

The advantage of the circuit circuit can be summarized as follows.

- Frequency of oscillation w_o and the condition of oscillation can be independently adjusted.

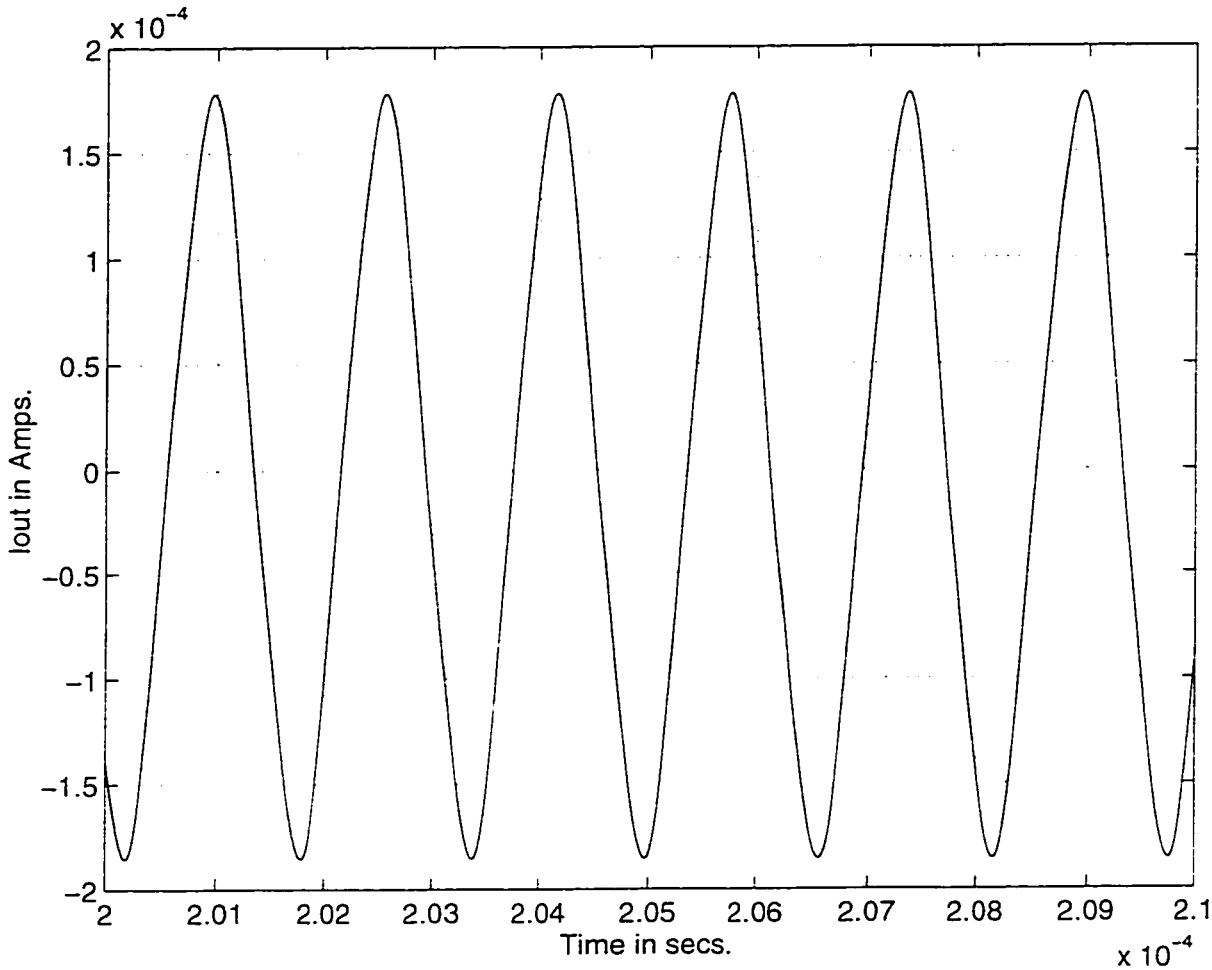


Figure 2.28: Simulation results of the sinusoidal oscillation. $C_1 = C_2 = 2nF$, $I_{b_1} = I_{b_2} = 100\mu A$

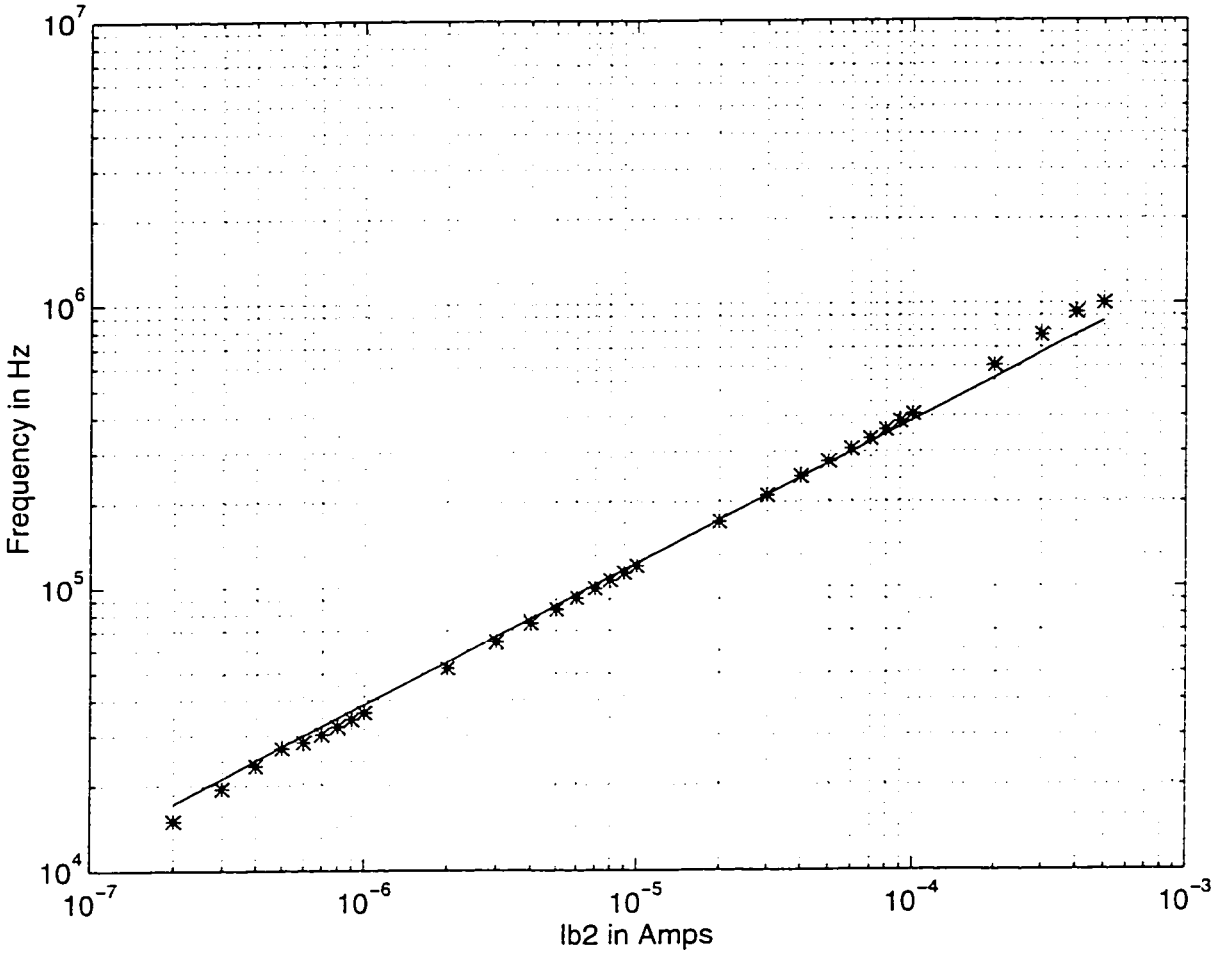


Figure 2.29: Oscillation frequencies against bias current. theoretical. ***simulation $C_1 = C_2 = 1nF, I_{b_1} = 10\mu A, I_{b_2} = 10.1\mu A$

- No external resistances are used.
- Grounded capacitors are used.
- Output current is available at high impedance node.
- Low active and passive sensitivities.

2.5 Impedance Simulation

Simulation of impedances is important for the design of active filters and oscillators and is well known in technical literature. Simulated inductors, variable capacitors and other more exotic devices such as FDNRs have been traditionally implemented with classical general impedance convertors (GIC) and negative impedance convertors (NIC) [58]. Such circuits have been extensively used in both discrete and integrated circuits, their most important drawback being the poor achievable bandwidth they exhibit because of the use of operational amplifiers.

These circuits are not programmable and can only be used for fixed impedances, making tuning of filters difficult. Current controlled conveyor, because of its programmable internal resistance, can introduce the controlling option and because of its high frequency operation can also remove the limitation of bandwidth.

From the literature survey, it has been observed that specific structures for the simulation of impedances other than inductors are very limited. The circuits proposed here can realize a nonideal grounded and floating capacitace multiplier and a grounded nonideal frequency dependent negative resistor (FDNR) element.

2.5.1 Capacitance Multiplier and FDNR Element

Capacitance multiplication schemes can be used to multiply the value of a small capacitor by a large positive constant to obtain a large effective capacitance. In filter applications the value of the multiplying constant can be made programmable for tuning.

Operational transcoductance amplifier (OTA) based circuits also provide the programmability feature, but they suffer from poor bandwidth [69][60]. The circuit proposed in [69] does not provide the C-attenuation option and uses floating external capacitor. The circuit proposed in [60] uses operational amplifier, therefore it has bandwidth limitation. Also the circuit for floating capacitance multiplier requires a floating external capacitor and matching conditions. This limitation is removed by using current controlled conveyor.

The proposed circuit is shown in Figure 2.30. It uses current controlled conveyor (CCCII+) with internal resistance R_x. Routine analysis of the circuit assuming ideal CCCII ($v_x = v_y + i_x R_x, i_x = i_z$) gives the following transfer function.

$$\frac{V_{in}}{I_{in}} = Z_{in} = (R_{x_1} + R_{x_2}) + \frac{Z_1 Z_2}{R_{x_3}} \tag{2.61}$$

For $Z_1 = R$ and $Z_2 = 1/sC$, the circuit simulates a series grounded RC impedance.

$$Z_{in} = (R_{x_1} + R_{x_2}) + \frac{R}{sR_{x_3}C} \tag{2.62}$$

where, $R_{eq} = R_{x_1} + R_{x_2}$ and $C_{eq} = \frac{R_{x_3}C}{R}$

Equation (2.62) shows that the equivalent resistance (R_{eq}) and capacitance (C_{eq}) are independently adjustable. Also if we take R as another current controlled conveyor the capacitance becomes temperature insensitive. The multiplying factor for

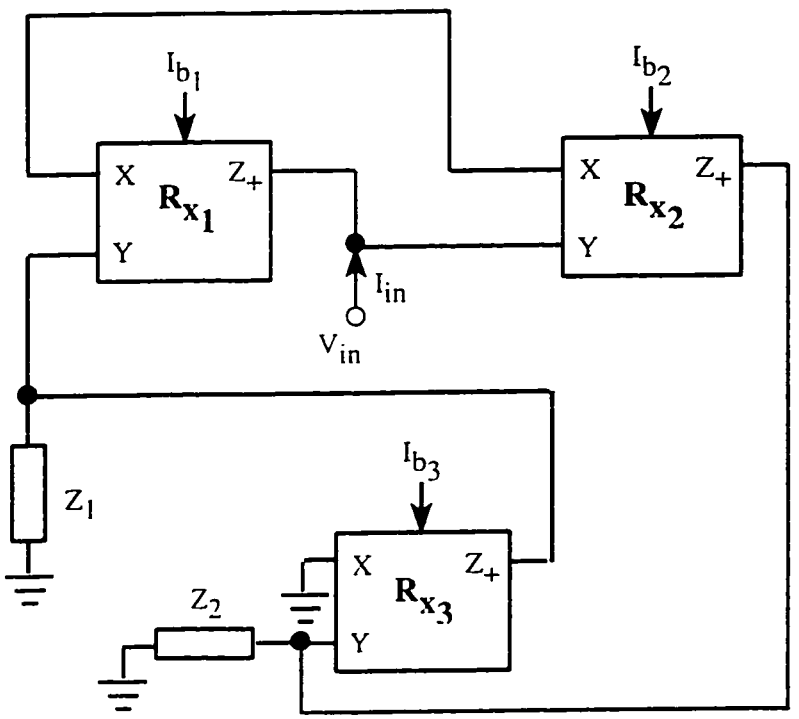


Figure 2.30: CCCII+ based impedance simulator.

C_{eq} is current controlled. The external capacitance is grounded, therefore the parasitic capacitance effect can be minimized.

Simulation results for this capacitance multiplier is shown in Figure 2.31. The controlled conveyor is implemented by using transistor PR100N(PNP) and NR200N(NPN) of the bipolar arrays ALA400 from AT&T [67]. The simulation result agrees well with the theory. It is obtained by varying the biasing current I_{b_3}. The deviation in capacitance for large values of biasing current occurs due to the beta error.

A grounded series R-FDNR can also be realized from the circuit of Figure 2.30 by taking $Z_1 = 1/sC_1$ and $Z_2 = 1/sC_2$. The input impedance will now become,

$$Z_{in} = (R_{x_1} + R_{x_2}) + \frac{1}{s^2 C_1 C_2 R_{x_3}} \tag{2.63}$$

where, $R_{eq} = R_{x_1} + R_{x_2}$ and $D = C_1 C_2 R_{x_3}$

The equivalent resistance (R_{eq}) and FDNR (D) are independently adjustable. The value of FDNR can be adjusted by varying R_{x_3}.

To verify the theoretical result, a highpass filter is constructed as shown in Figure 2.32. The filter is simulated by using the transistor PR100N(PNP) and NR200N(NPN) of the bipolar arrays ALA400 from AT&T [67]. The simulation result shown in Figure 2.33, for 100kHz frequency, agrees well with the theory.

The circuit of Figure 2.30 can be easily modified to a floating series R-C realization and is shown in Figure 2.34. Routine analysis of the circuit assuming ideal CCCII ($v_x = v_y + i_x R_x, i_x = i_z$) gives the following transfer function.

$$\frac{V_{in}}{I_{in}} = Z_{in} = (R_{x_1} + R_{x_2}) + \frac{R_{x_3}}{R_{x_4} C_2 s} \tag{2.64}$$

where, $R_{eq} = R_{x_1} + R_{x_2}$ and $C_{eq} = \frac{R_{x_4} C}{R_{x_3}}$

The equivalent resistance (R_{eq}) and capacitance (C_{eq}) are independently adjustable and there are no matching conditions. Also the simulated capacitance is

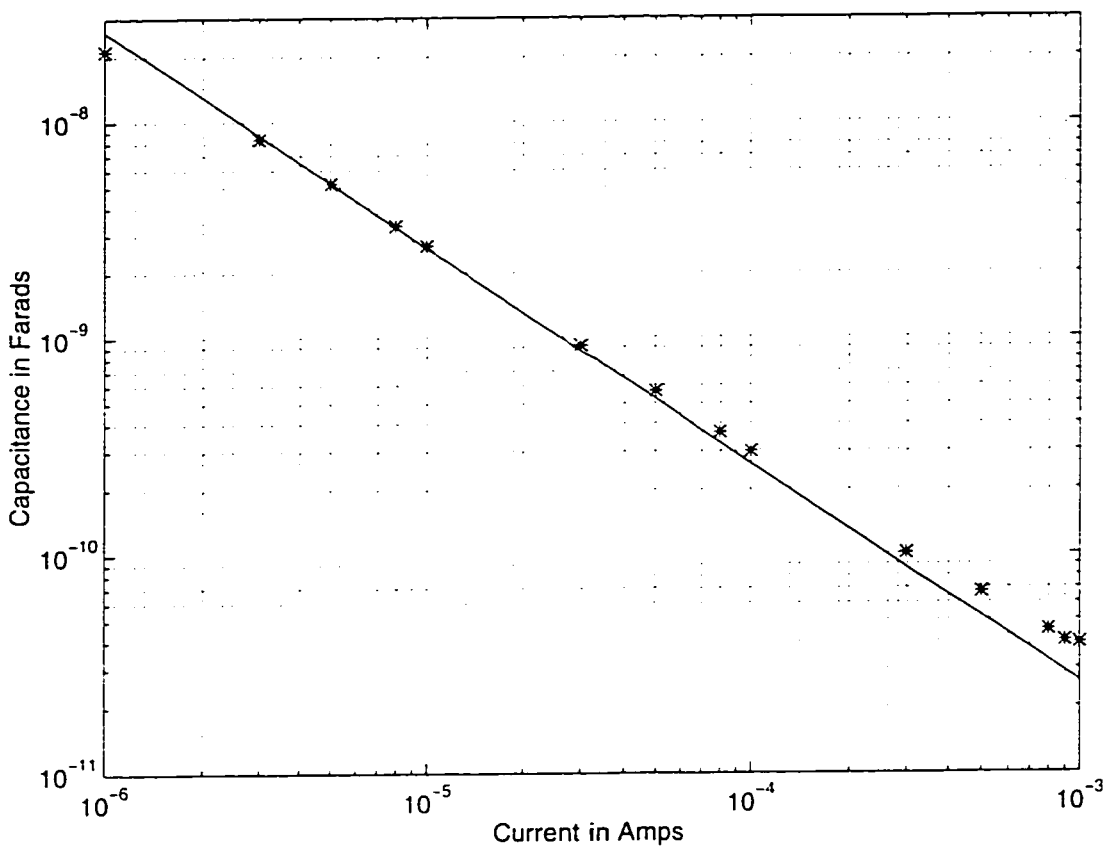


Figure 2.31: Simulation result of grounded capacitance multiplier. theoretical. ***simulation. $R = 500\Omega, R_{x_1} = R_{x_2} = 250\Omega, C = 1nF$

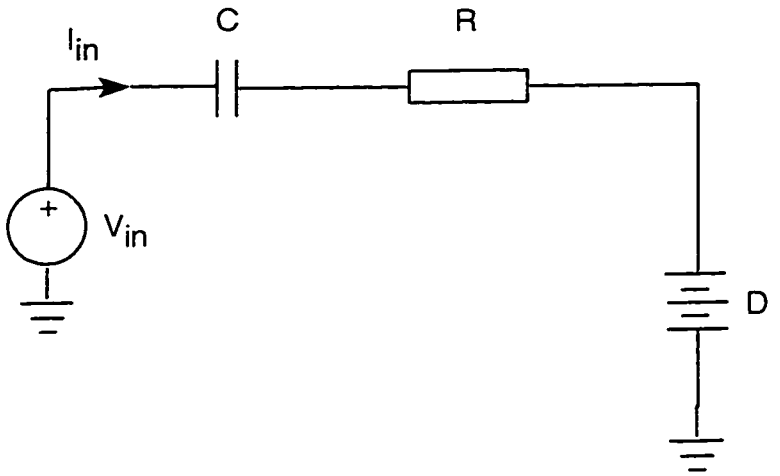


Figure 2.32: Highpass filter using FDNR.

temperature insensitive. The multiplying factor for C_{eq} is current controlled. The external capacitance is grounded, therefore the parasitic capacitance effect can be minimized.

Simulation results for this capacitance multiplier is shown in Figure 2.35. The controlled conveyor is implemented by using transistor PR100N(PNP) and NR200N(NPN) of the bipolar arrays ALA400 from AT&T [67]. The simulation result agrees well with the theory and is obtained by varying the bias current I_{b_4}. The deviation in capacitance for large values of biasing current occurs due to the beta error.

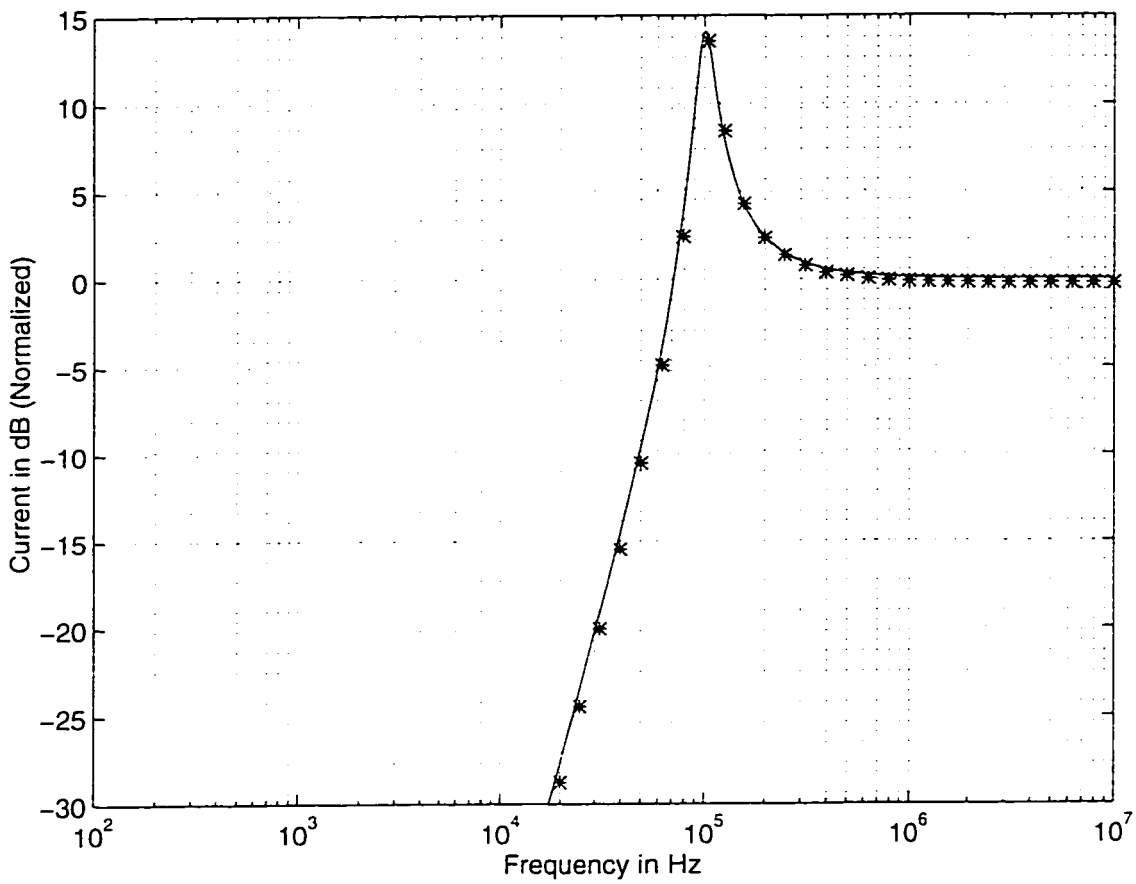


Figure 2.33: Simulation result of highpass filter using FDNR.

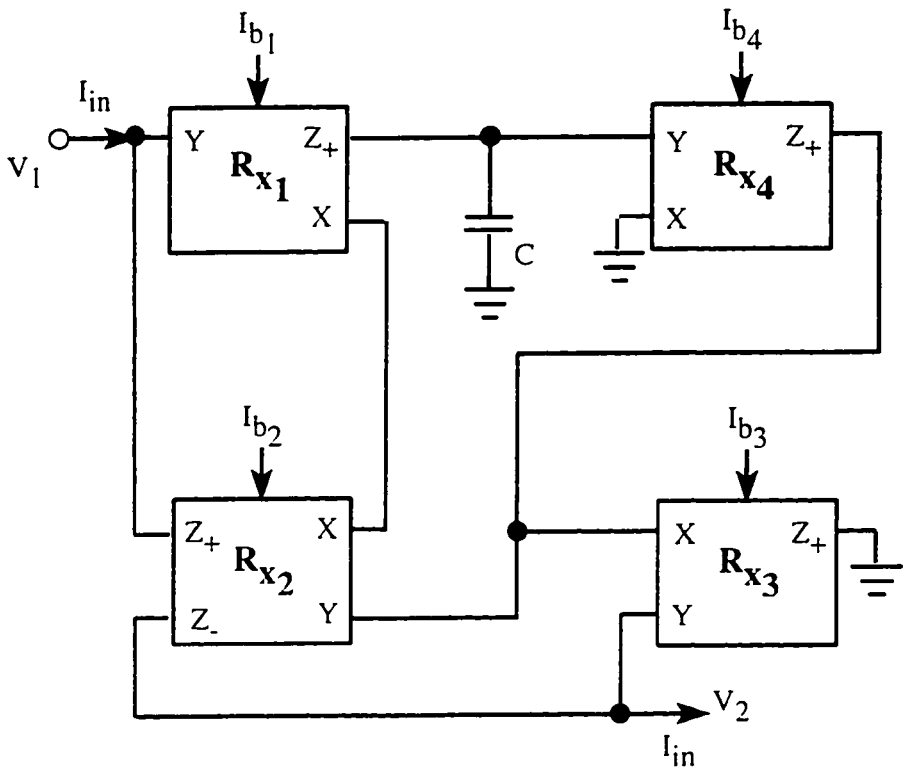


Figure 2.34: CCCII based floating capacitance simulator.

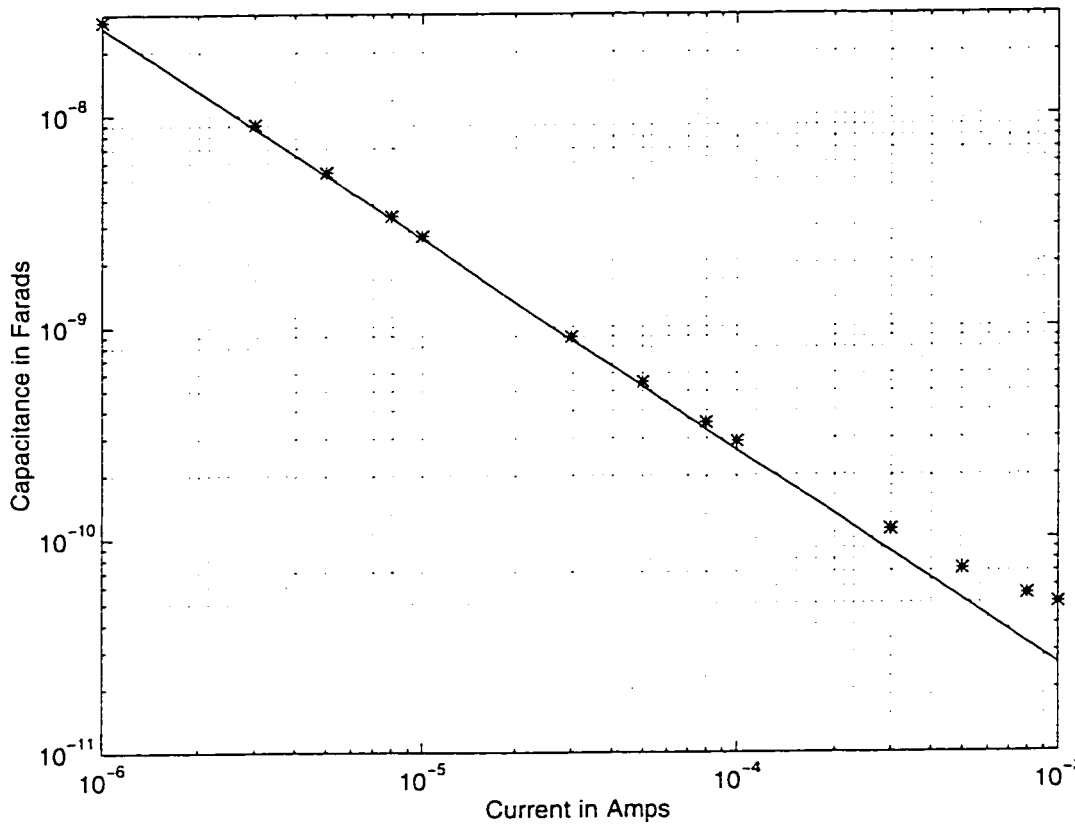


Figure 2.35: Simulation result of floating capacitance multiplier. theoretical, ***simulation. $R_{x_1} = R_{x_2} = 250\Omega, R_{x_3} = 500\Omega, C_2 = 1nF$

Chapter 3

Higher Order Filter Synthesis

As discussed in chapter one, higher order filters can be realized by cascading isolated second order filter sections. It gives the advantage of noninteracting sections, i.e. the coefficients of one section do not alter the coefficients of any other section. This is achieved at the expense of increased number of components which increases the chip area and power dissipation.

Instead of cascading second order sections, higher order filters can also be synthesized by signal flow graph. Signal flow graph is an important tool in designing higher order filters. It is based on realizing the general transfer function by a signal flow graph and then obtaining the active circuit. The n^{th} order active circuit is obtained by representing a single branch of signal flow graph with an active block and then cascading these blocks to get the required order.

Various current and voltage mode n^{th} order filters have been proposed [62]-[65] using the current conveyor. But there has been, so far, no attempt to present n^{th} order filters using controlled conveyors (CCCIIs). Moreover most of these circuits require large number of active and passive elements and use floating resistors and

capacitors or can realize only an all pole transfer function.

For higher order filters it is important to have small number of components and simple architecture. This is due to the fact that, as the filter order will increase the number of components will also increase. The large number of components generally increases power consumption, the occupied chip area, noise and circuit parasitics. The filter structure should also have grounded capacitors because the grounded capacitors can be implemented on a smaller area than the floating capacitors and can also absorb parasitic capacitance, which is important for high frequency operation.

The filter proposed here is designed by keeping in mind the above mentioned requirements. This architecture has no external resistances because of the use of controlled conveyors, grounded and minimum number of capacitances and minimum number of active elements.

First the synthesis of n^{th} order low pass function will be explained and then the general transfer function will be carried out.

3.1 Low Pass n^{th} order Transfer Function

The n^{th} order low pass current transfer function can be represented as,

$$\frac{I_{LP}(s)}{I_{in}(s)} = \frac{K}{B_n s^n + B_{n-1} s^{n-1} + \cdots + B_2 s^2 + B_1 s + B_o} \tag{3.1}$$

where I_{LP} and I_{in} are the output and input currents respectively. The denominator is a Hurwitz Polynomial with positive real coefficients. This transfer function can be represented by a signal flow graph (Appendix A) shown in Figure 3.1. The graph transfer function from the input node to the output node can be easily verified by using the well known Mason gain formula.

Using this signal flow graph the n^{th} order low pass current transfer function can be realized using the active circuit involving controlled conveyor (CCCII). For this realization it is sufficient to know the active subcircuit corresponding to the subgraph. The subgraph and its active subcircuit realization is shown in Figure 3.2. The subcircuit consists of a multiple output CCCII and a single capacitor. Feedback current necessitates the use of multiple output current conveyor. The negative current output can be obtained from the basic CCCII circuit by crosscoupled transistors.

The active circuit realizing any n^{th} order low pass transfer function can easily be obtained by interconnecting the subcircuit of Figure 3.2 according to the overall signal flow graph. The circuit thus obtained is shown in Figure 3.3. The feedbacks are realized by just using a shorting wire. Unity feedback current makes it possible to realize filter with grounded capacitors. The design equations can be written as follows:

$$\begin{aligned} B_o &= 1 : B_1 = C_n R_{x_n} : \frac{B_2}{B_1} = C_{n-1} R_{x_{n-1}} : \cdots \frac{B_{n-1}}{B_{n-2}} = C_2 R_{x_2} : \frac{B_n}{B_{n-1}} = C_1 R_{x_1} \\ K &= -1. \end{aligned} \tag{3.2}$$

Resistances $R_{x_1}, R_{x_2}, \ldots, R_{x_n}$ are the internal resistances of the current conveyors. The circuit has no external resistances and the number of capacitors and controlled conveyors (CCCIIs) is equal to 'n', i.e. the order of the filter, which is the minimum number of components. The cutoff frequency is programmable and can be changed by selecting different values of bias currents.

The circuit of Figure 3.3 uses negative current output for feedback. To realize a negative current mirror from simple current mirror six transistors are required, whereas, positive current mirror can be easily realized by using only two transistors.

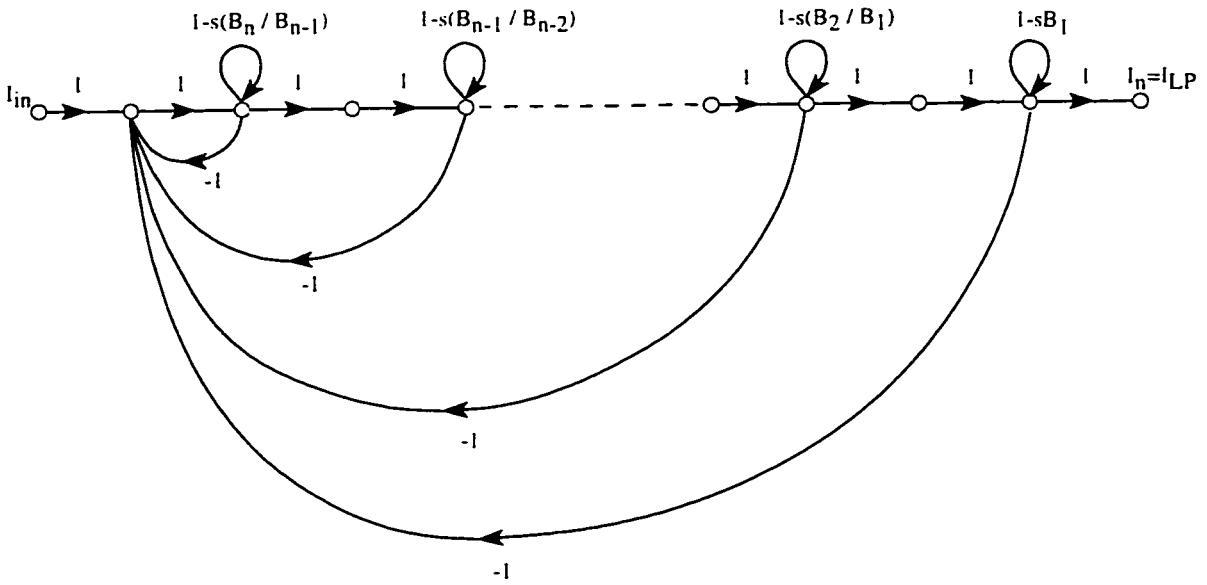


Figure 3.1: n^{th} order low pass signal flow graph.

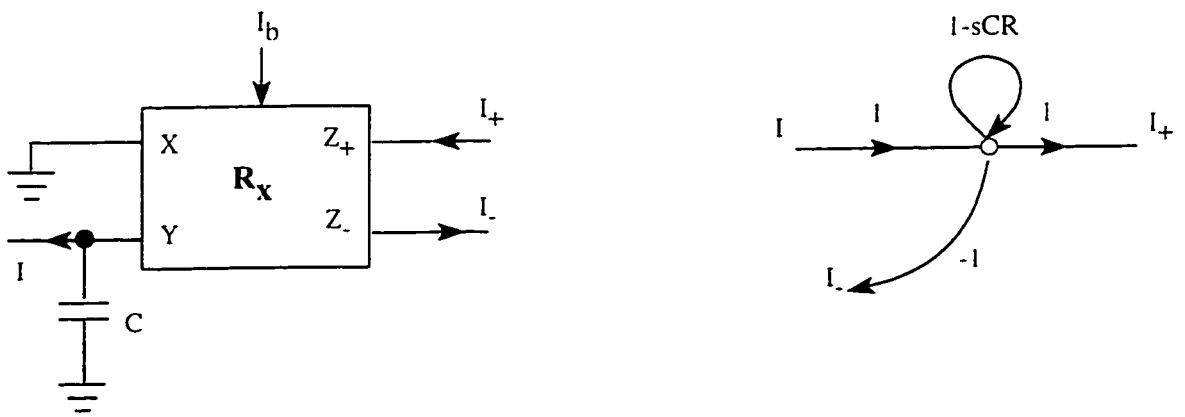


Figure 3.2: Correspondence between subgraph and subcircuit for low pass function.

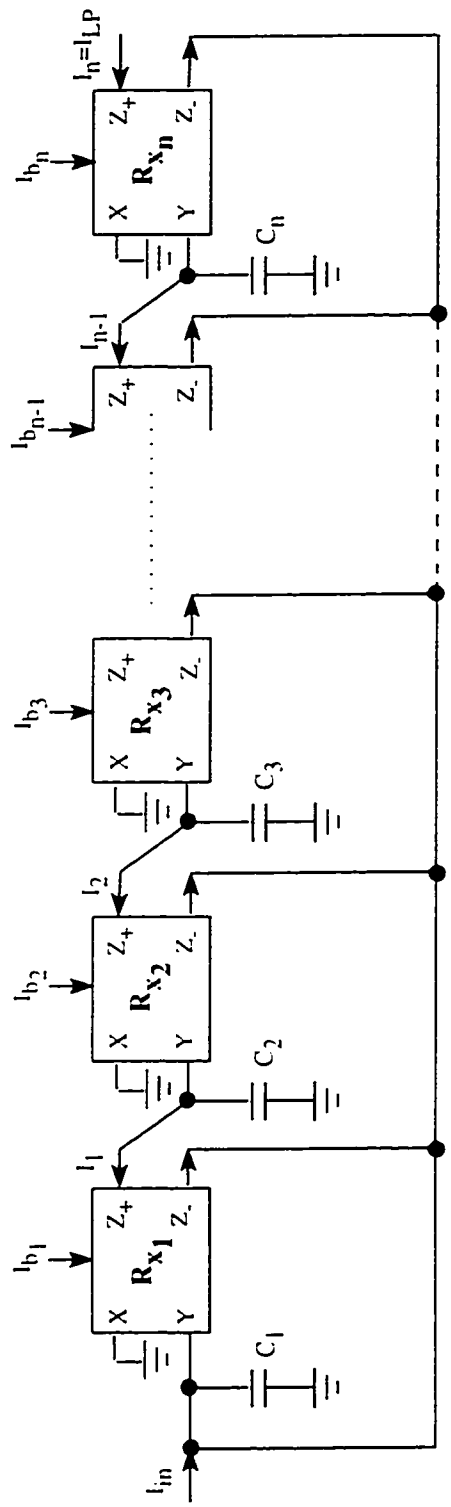


Figure 3.3: CCCII± network realizing n^{th} order current mode low pass transfer function.

This situation becomes worse when four transistor Wilson current mirrors are used. Addition of one more controlled conveyor (CCCII) can make it possible to realize the transfer function by multiple output conveyors with only positive current outputs. Instead of summing all the currents at the input node of the first CCCII, sum it at the input of another conveyor and connect its output to capacitor C_1. The resulting circuit is shown in Figure 3.4. This circuit can also realize any n^{th} order low pass allpole transfer function without the use of external resistances. Design equations are same as in equation (3.2) except that $K = +1$. The circuit now consists of $'n+1'$ controlled conveyors with only positive outputs and $'n'$ number of grounded capacitors, where $'n'$ is the order of the low pass filter.

3.2 General n^{th} order Transfer Function

The n^{th} order current transfer function can be represented as,

$$\frac{I_{out}(s)}{I_{in}(s)} = K\frac{A_n s^n + A_{n-1}s^{n-1} + \cdots + A_2 s^2 + A_1 s + A_o}{B_n s^n + B_{n-1}s^{n-1} + \cdots + B_2 s^2 + B_1 s + B_o} \tag{3.3}$$

where I_{out} and I_{in} are the output and input currents respectively. The zeros of equation (3.3) can be accommodated in the basic signal flow graph of Figure 3.1 by using feedforward paths (Appendix A). The resulting signal flow graph is shown in Figure 3.5. The graph transfer function can be easily verified by using the well known Mason gain formula.

To realize the graph by active circuit, subgraph realization is first carried out as in section 3.1. The resulting subgraph and subcircuit are shown in Figure 3.6. Cascading of subcircuit gives the complete active circuit for the realization of equation (3.3) and is shown in Figure 3.7. Coefficients of the denominator are realized by

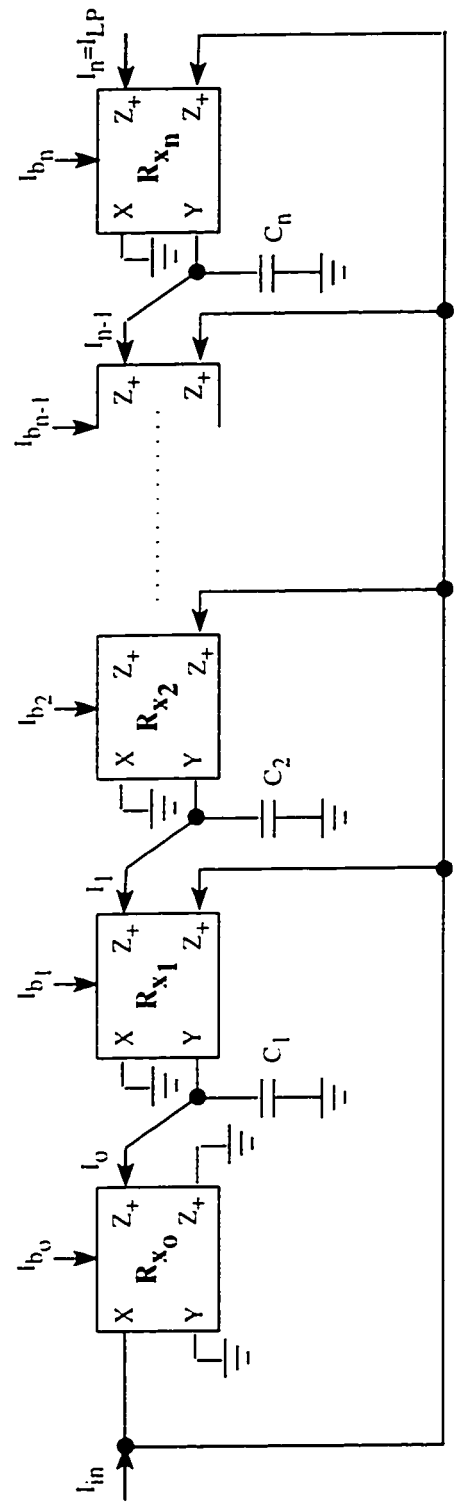


Figure 3.4: Multiple output CCCII+ network realizing n^{th} order current mode low pass transfer function

controlled conveyors with internal resistances $'R_x'$ and are required to be multiple output with positive and negative current outputs. The coefficients of numerator are realized by controlled conveyors with internal resistances $'r_x'$. These conveyors are not necessarily required to be multiple output. The design equations can be written as follows.

$$\begin{aligned} B_o &= 1 : B_1 = C_n R_{x_n} : \frac{B_2}{B_1} = C_{n-1} R_{x_{n-1}} \cdots \frac{B_{n-1}}{B_{n-2}} = C_2 R_{x_2} : \frac{B_n}{B_{n-1}} = C_1 R_{x_1} \\ \frac{A_o}{B_o} &= \frac{R_{x_n}}{r_{x_n}} : \frac{A_1}{B_1} = \frac{R_{x_{n-1}}}{r_{x_{n-1}}} \cdots \frac{A_{n-1}}{B_{n-1}} = \frac{R_{x_1}}{r_{x_1}} : A_n = 0 : K = -1. \end{aligned} \tag{3.4}$$

It can be seen that the circuit of Figure 3.7 uses no external resistances and only grounded capacitors are used which is a great advantage. Also the number of active components is minimum. It requires at most '$2n$' CCCIIs and 'n' grounded capacitors to realize a transfer function with $A_n = 0$. The cutoff frequency is programmable as controlled conveyors are used and can be selected by using different values of bias currents. It can realize Chebyshev, Butterworth and Elliptic filters.

The filter of Figure 3.7 cannot realize transfer function with $A_n \neq 0$. This discrepancy can be removed by making use of the signal flow graph of Figure 3.5. The coefficient of s^n is enabled by the summing input node which is not used in the circuit realization of Figure 3.7. The summing current flowing through C_1 can be directly connected to the output node to have s^n coefficient, but in this case C_1 will no more remain grounded. Another approach is to sum the input current and output feedback currents in a separate multiple output CCCII and connect its output to the capacitor C_1. The resulting circuit is shown in Figure 3.8. Multiple outputs are now all positive current type and thus results in the saving of number

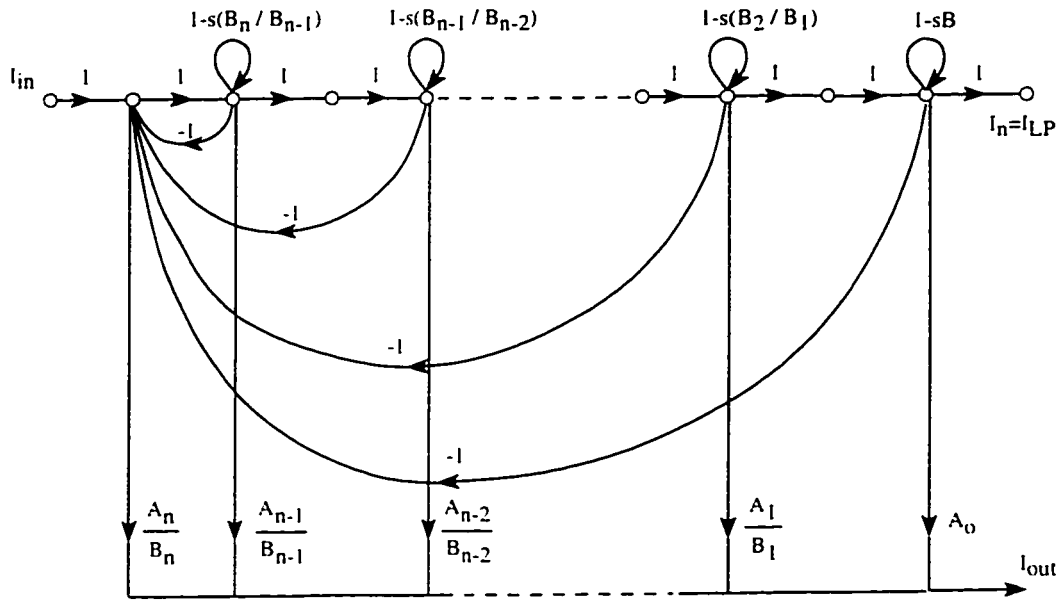


Figure 3.5: n^{th} order signal flow graph of general transfer function.

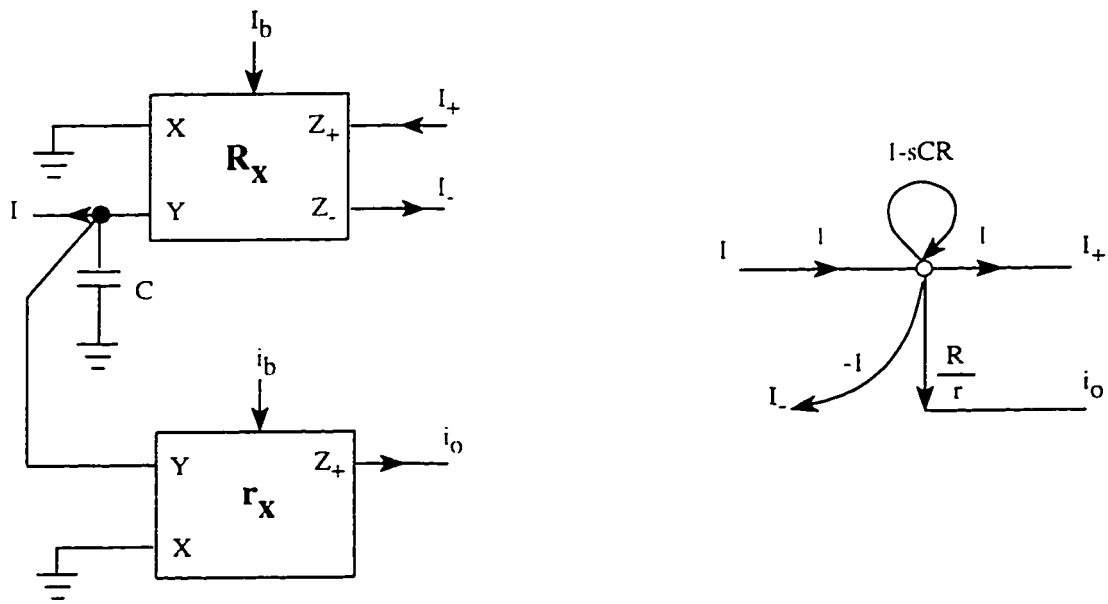


Figure 3.6: Correspondence between subgraph and subcircuit for general transfer function.

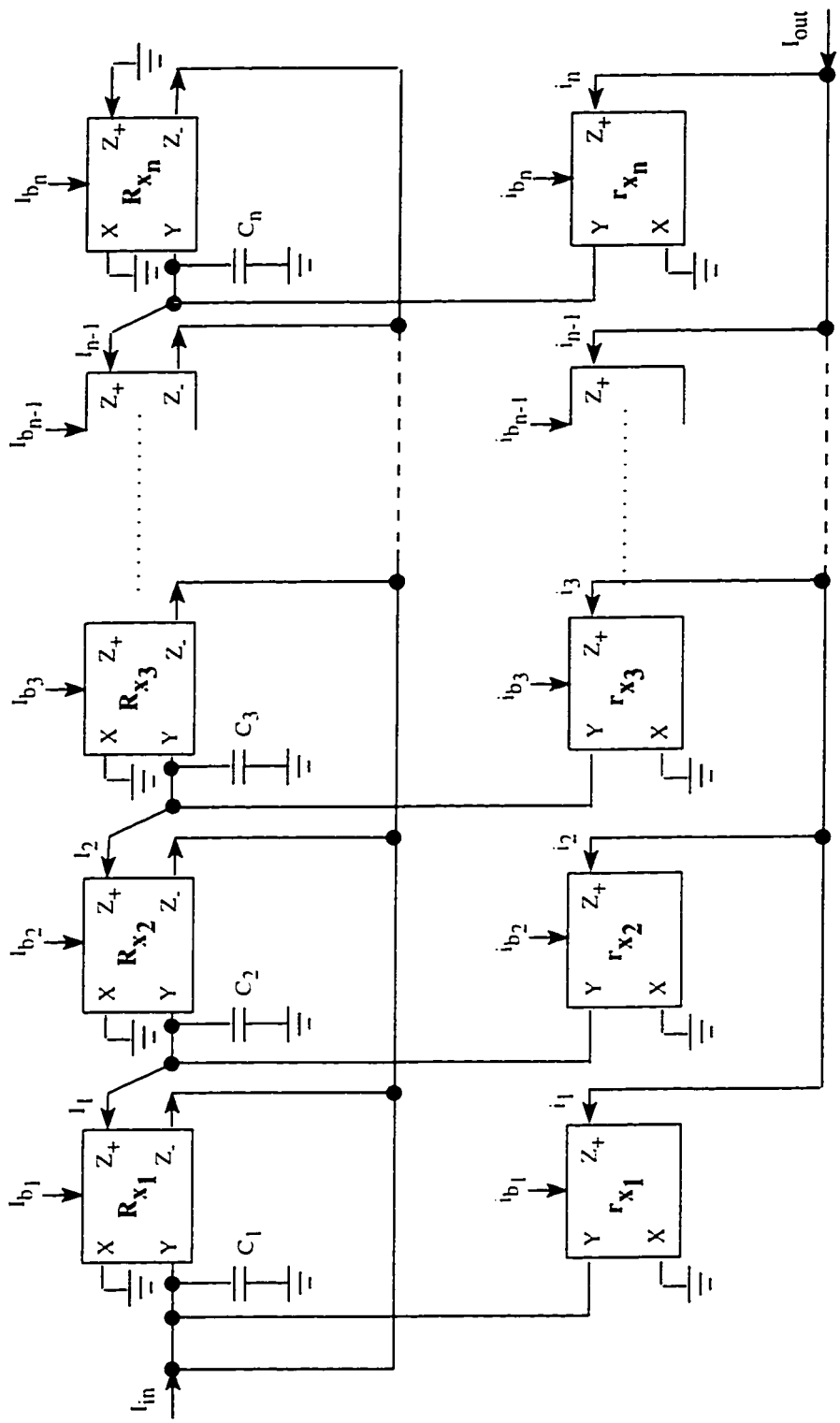


Figure 3.7: CCCII± network realizing n^{th} order current mode general transfer function

of transistors. Design equations are,

$$\begin{aligned} B_o &= 1 : B_1 = C_n R_{x_n} : \frac{B_2}{B_1} = C_{n-1} R_{x_{n-1}} \cdots \frac{B_{n-1}}{B_{n-2}} = C_2 R_{x_2} : \frac{B_n}{B_{n-1}} = C_1 R_{x_1} \\ \frac{A_o}{B_o} &= \frac{R_{x_n}}{r_{x_n}} : \frac{A_1}{B_1} = \frac{R_{x_{n-1}}}{r_{x_{n-1}}} \cdots \frac{A_{n-1}}{B_{n-1}} = \frac{R_{x_1}}{r_{x_1}} : A_n = B_n : K = +1. \end{aligned} \tag{3.5}$$

To have different A_n and B_n an amplifier can be easily added at the summing node. It can be observed from equation (3.5) that the circuit can realize any special transfer function, since any coefficient A_i of the numerator can be enabled to any value including zero by properly choosing the values of $r_i, 1 \leq i \leq n$. For any $A_i = 0$, its associated CCCII should be removed. On the other hand, for any $A_i < 0$, simply use a negative current output for that related CCCII. Similarly any special biquadratic filter can be realized by appropriately selecting CCCIIs.

3.3 Simulation Results and Discussion

To validate the theoretical analysis, different high order filter transfer functions are simulated. Same schematic implementation and bipolar transistor models are used for CCCII as for universal filters of chapter two.

Figure 3.9 shows the circuit diagram for a third order elliptic filter. It is simulated for a cutoff frequency of 500kHz. The theoretical and simulation results are compared in the graph of Figure 3.10. It can be seen that they are in good agreement to each other.

Figure 3.11 shows the circuit diagram for a third order highpass elliptic filter. It is simulated for a cutoff frequency of 100kHz. It can be seen from the graphical results of Figure 3.12 that theoretical and simulation results are comparable to each other.

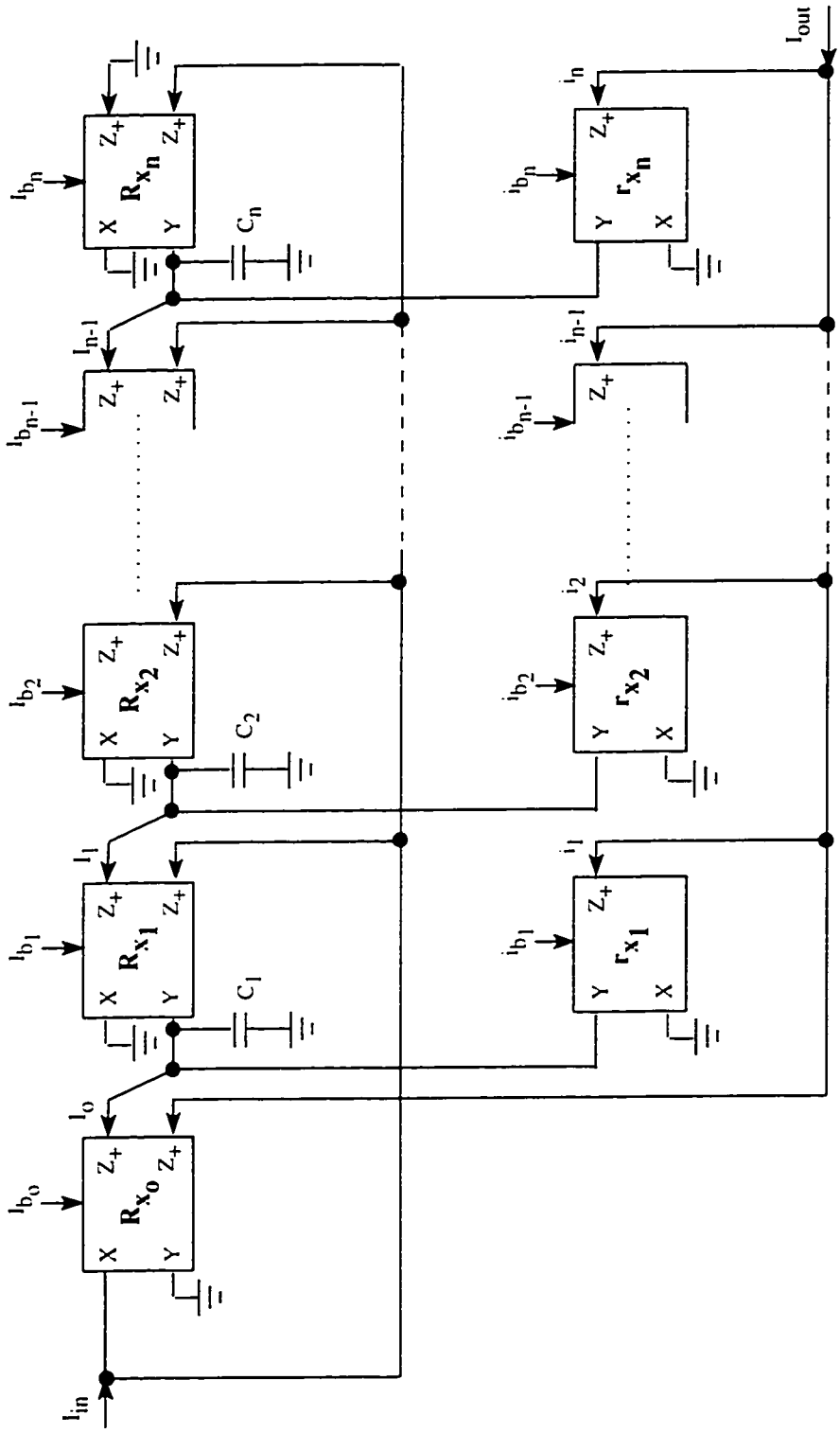


Figure 3.8: Multiple output CCCII+ network realizing n^{th} order current mode general transfer function

Similar simulations are done for the fifth order lowpass butterworth filter, fourth order highpass butterworth filter and fourth order allpass filter transfer functions (for 100kHz frequency). The results are shown in the graphs of Figure 3.13 to 3.16 respectively. The simulation results agree with the theoretical one with slight deviation.

The deviation for higher frequencies comes because of the cutoff frequency of the transistors. To reduce these deviations, transistors with higher cutoff frequencies should be used. Also to reduce the deviation due to the diminutions of the beta for high currents, transistors with high value beta should be used.

In short the circuit offers the following advantages.

- Any n^{th} order transfer function can be realized.
- No external resistances are used.
- At most 'n' capacitors and '$n+1$' active elements are required.
- Only grounded capacitors are used.

If these advantages are compared with the circuit proposed by Acar [63], it can be seen that the Acar's circuit needs at most $2n+3$ resistors (most of them floating), n capacitors (most of them floating) and $n+2$ active devices. This shows that the proposed circuit is a good candidate for the realization of high order filters.

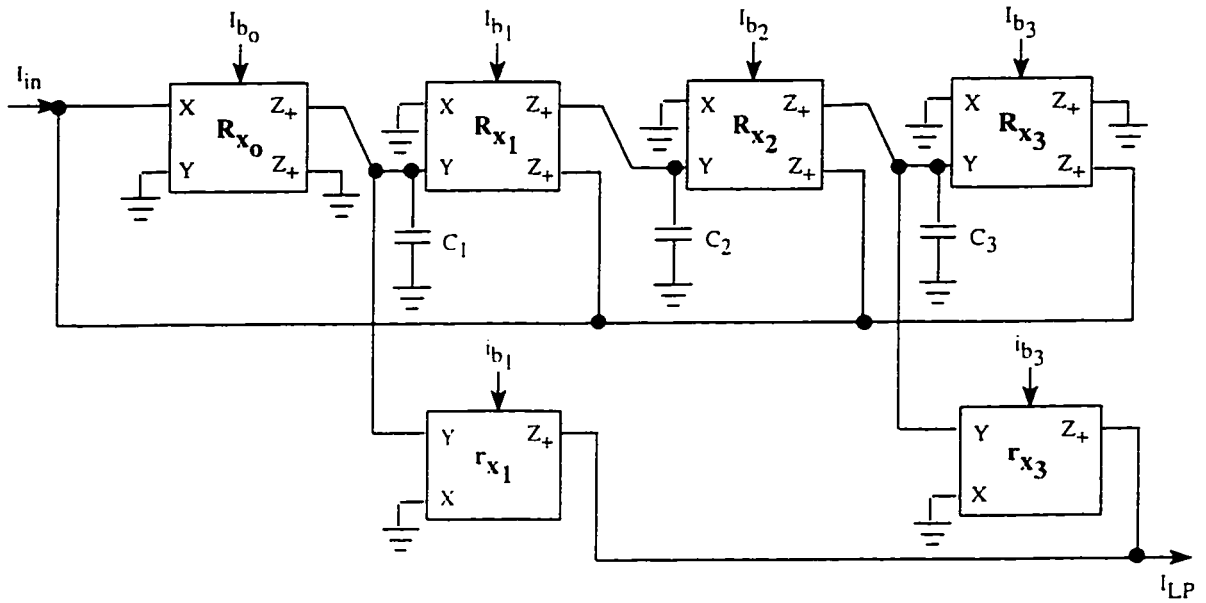


Figure 3.9: Circuit diagram of 3^{rd} order lowpass elliptic filter.

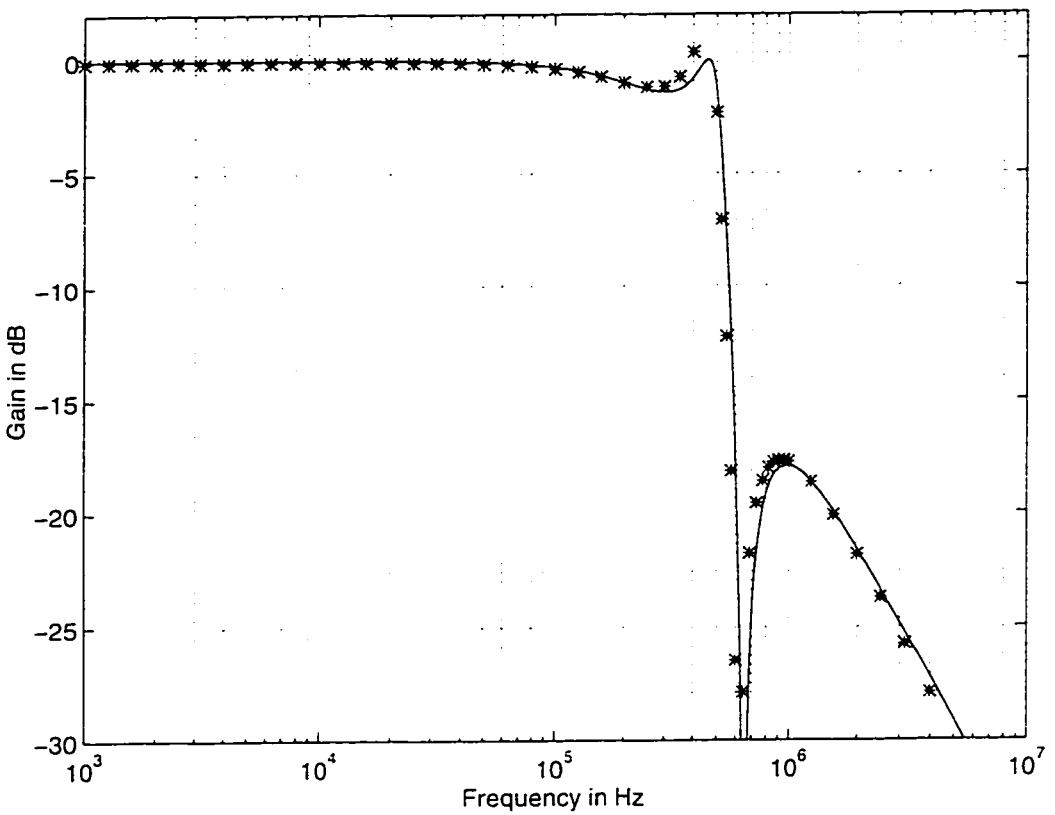


Figure 3.10: Simulation result of third order lowpass elliptic filter. theoretical, ***simulation. $C_1 = C_2 = C_3 = 1nF, I_{b_1} = 34.68\mu A, I_{b_2} = 55.1\mu A, I_{b_3} = 21.34\mu A, i_{b_1} = 14.38\mu A, i_{b_3} = I_3$

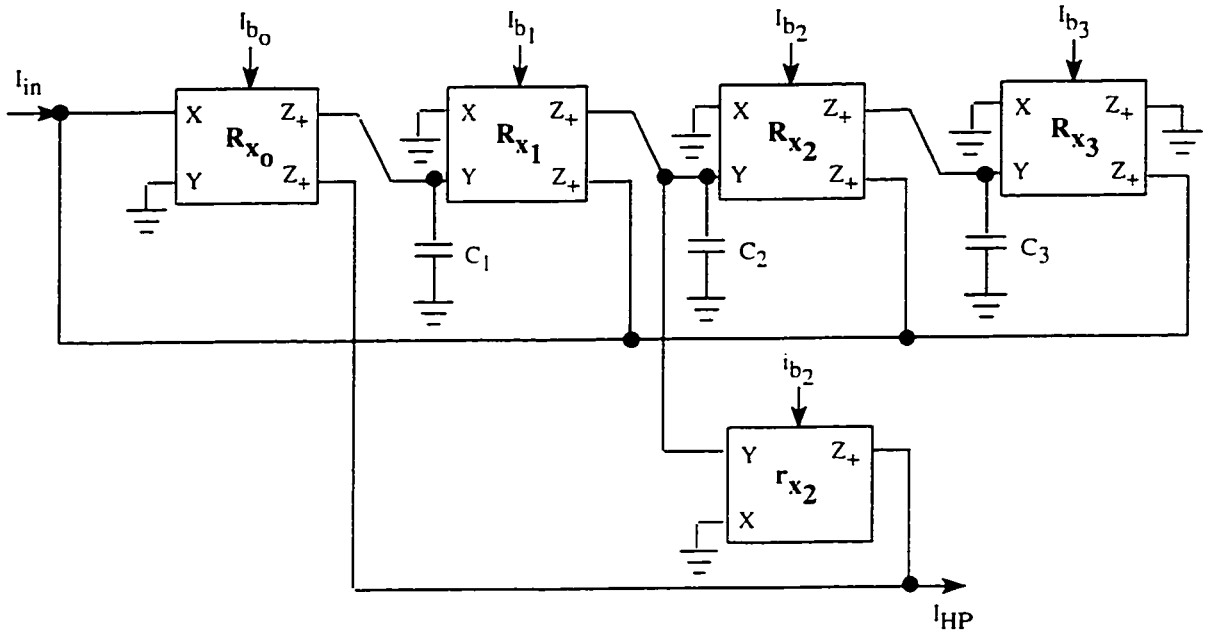


Figure 3.11: Circuit diagram of 3^{rd} order highpass elliptic filter.

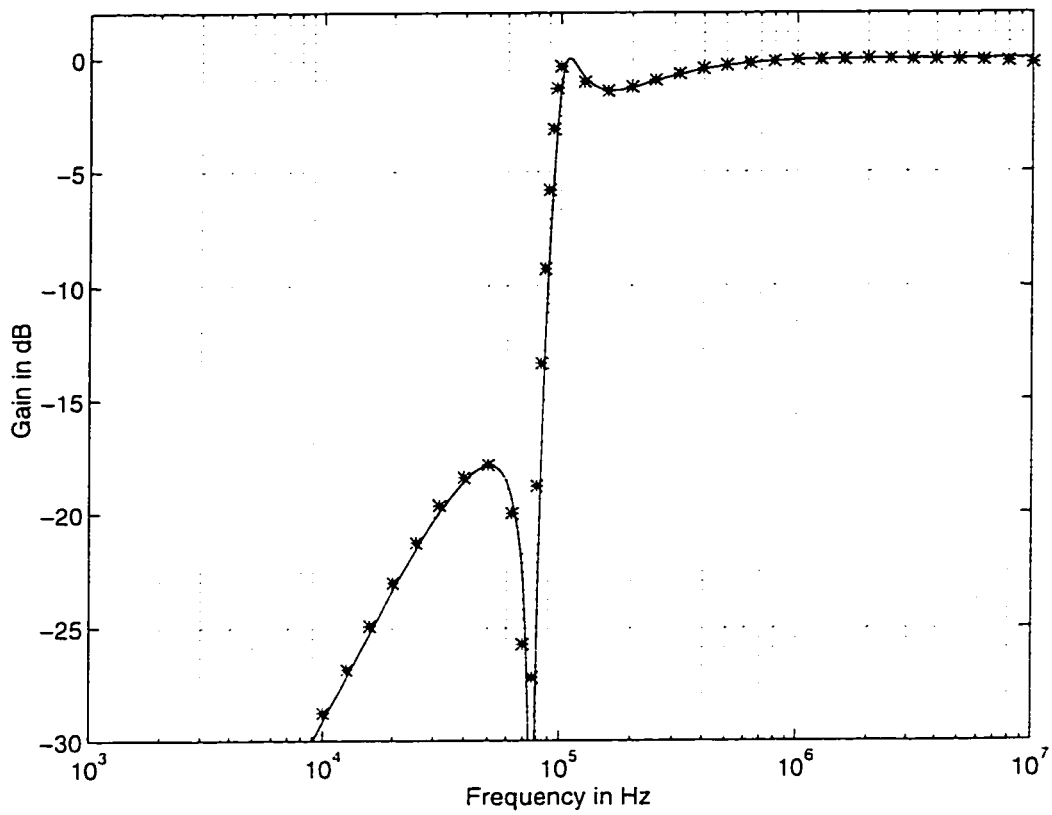


Figure 3.12: Simulation result of third order highpass elliptic filter. theoretical, ***experimental, $C_1 = C_2 = C_3 = 4nF$, $I_{b_1} = 62.53\mu A$, $Ib_2 = 24.22\mu A$, $I_{b_3} = 38.47\mu A$, $i_{b_2} = 10.04\mu A$

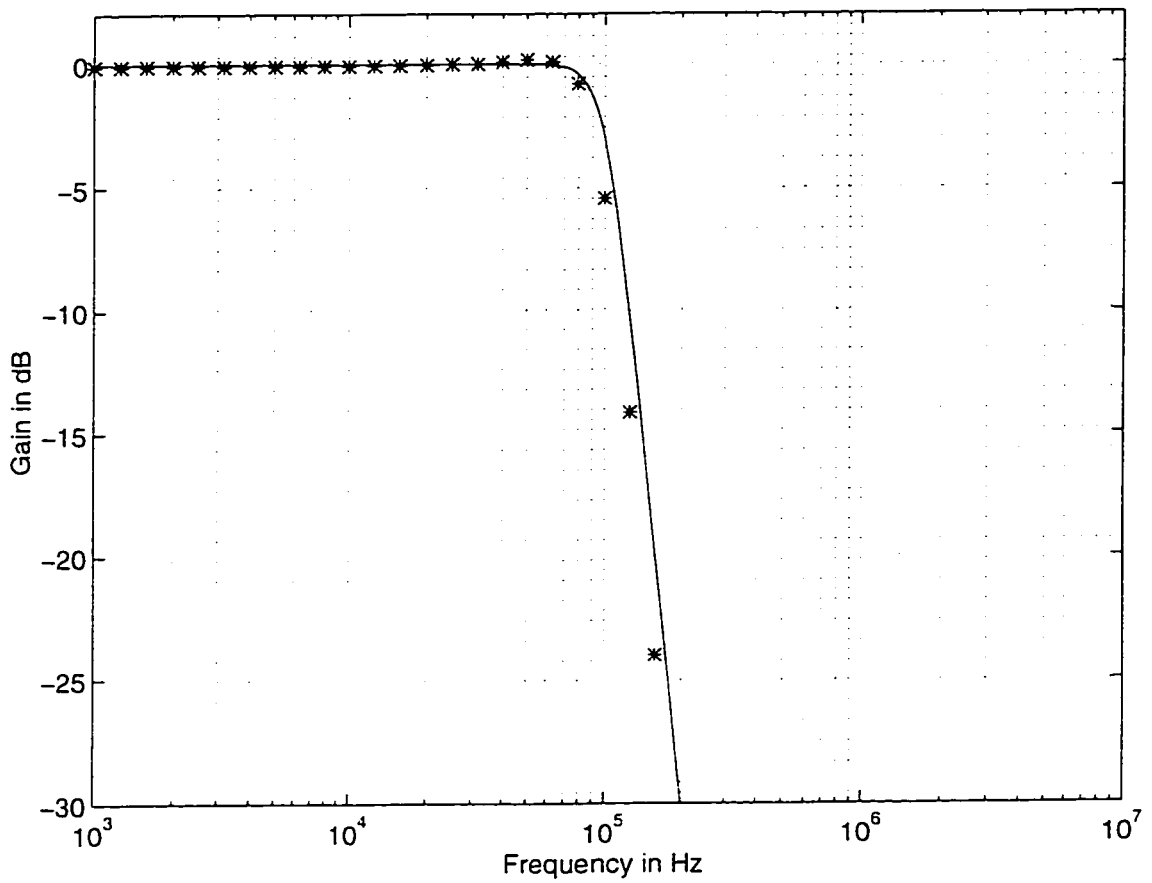


Figure 3.13: Simulation result of fifth order lowpass butterworth filter. theoretical, ***simulation. $C_1 = C_2 = C_3 = C_4 = C_5 = 4nF$, $I_{b_1} = 105.73\mu A$, $Ib_2 = 52.86\mu A$, $I_{b_3} = 32.67\mu A$, $I_{b_4} = 20.19\mu A$, $I_{b_5} = 10.1\mu A$

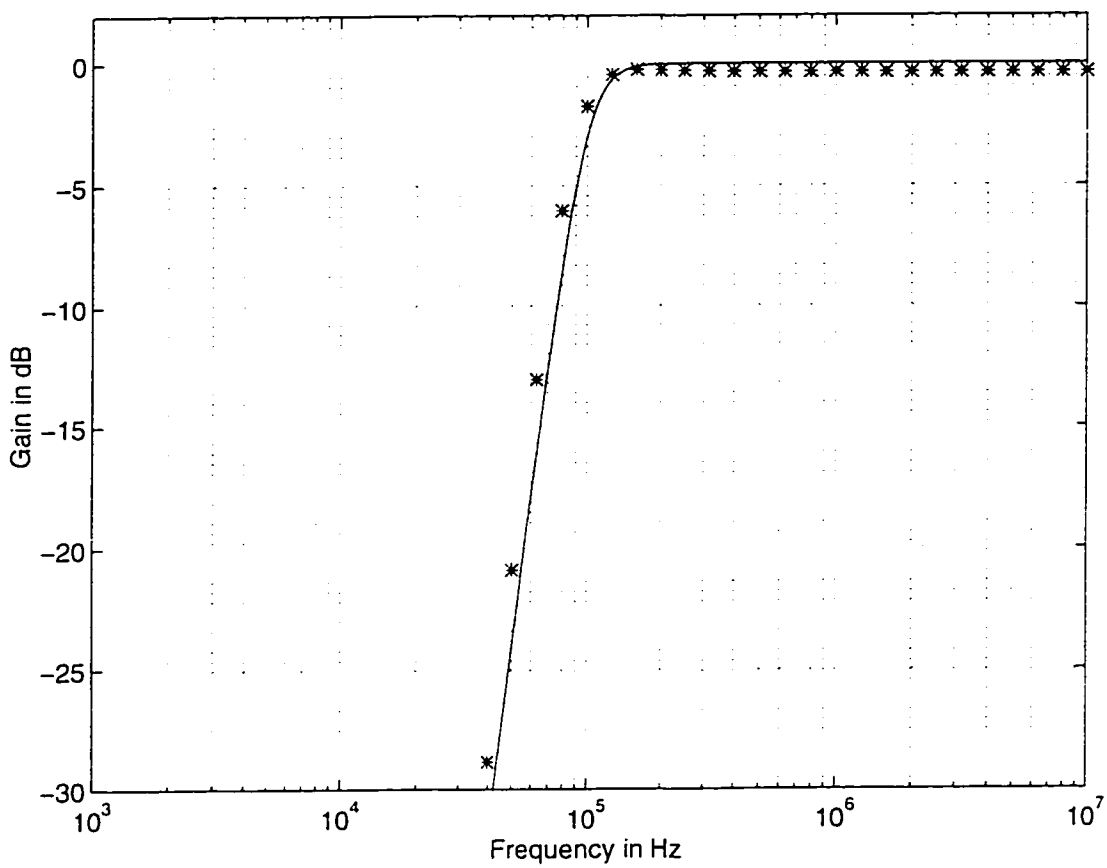


Figure 3.14: Simulation result of fourth order highpass butterworth filter. theoretical, ***simulation. $C_1 = C_2 = C_3 = C_4 = 4nF, I_{b_1} = 85.37\mu A, Ib_2 = 42.69\mu A, I_{b_3} = 25\mu A, I_{b_4} = 12.5\mu A$

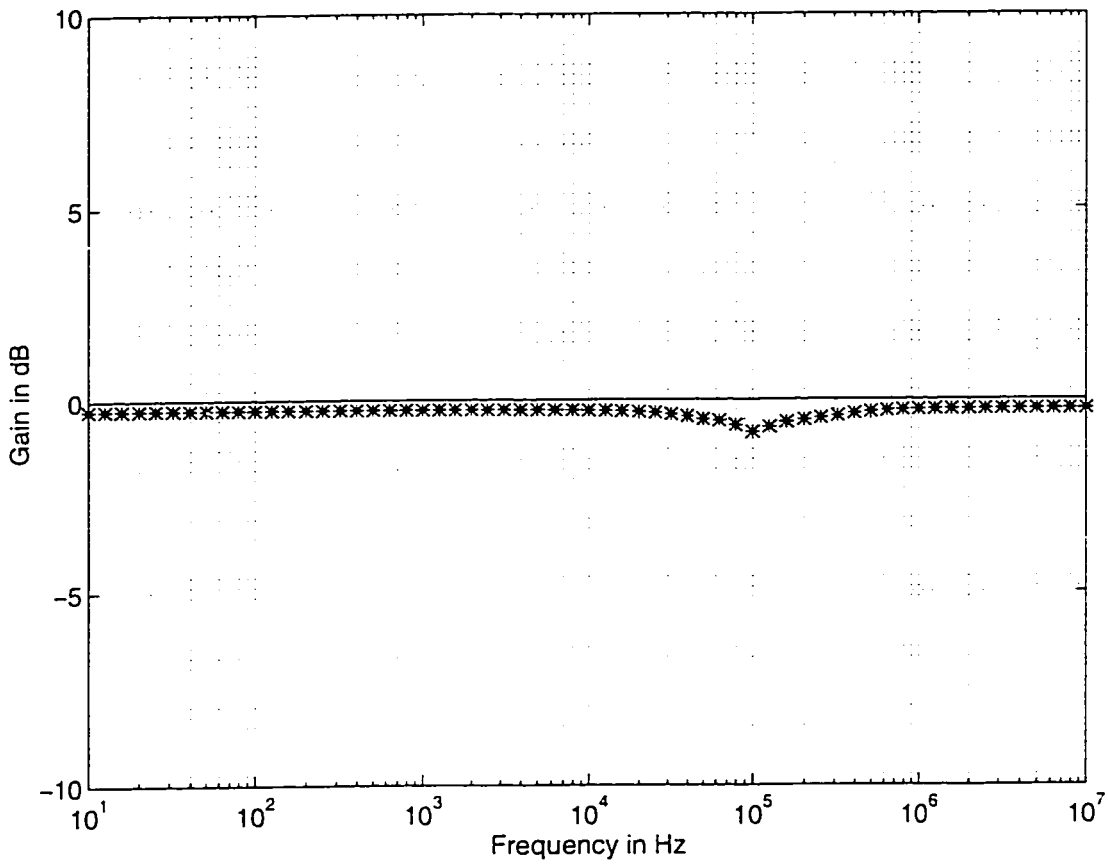


Figure 3.15: Simulation result of gain response of fourth order allpass filter. theoretical, ***simulation. $C_1 = C_2 = C_3 = C_4 = 4nF, I_{b_1} = 85.37\mu A, Ib_2 = 42.69\mu A, I_{b_3} = 25\mu A, I_{b_4} = 12.5\mu A, i_{b_1} = I_{b_1}, i_{b_2} = -I_{b_2}, i_{b_3} = I_{b_3}, i_{b_4} = -I_{b_4}$

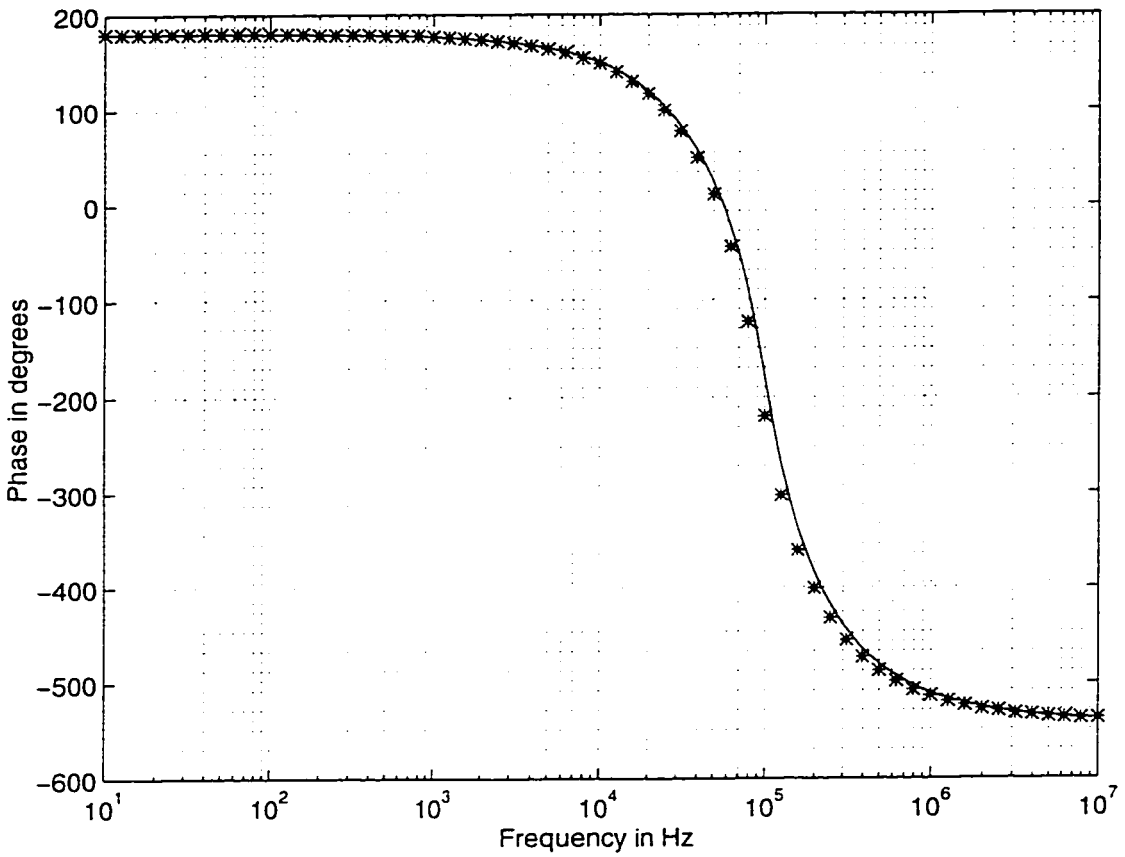


Figure 3.16: Simulation result of phase response of fourth order allpass filter. theoretical, ***simulation. $C_1 = C_2 = C_3 = C_4 = 4nF, I_{b_1} = 85.37\mu A, Ib_2 = 42.69\mu A, I_{b_3} = 25\mu A, I_{b_4} = 12.5\mu A, i_{b_1} = I_{b_1}, i_{b_2} = -I_{b_2}, i_{b_3} = I_{b_3}, i_{b_4} = -I_{b_4}$

Chapter 4

CONCLUSION AND FUTURE WORK

4.1 Conclusion

In this thesis current controlled conveyor and its applications were discussed. It was shown that the programmable internal resistance of current controlled conveyor could be used for the design of tunable filters, oscillator and impedance simulators. The advantages obtained were: no external resistances required, low power dissipation and less silicon area. The disadvantages associated with the use of current controlled conveyor were that the internal resistance was temperature dependent and for very low or very high values of bias current, errors were encountered due to the low values of β.

The literature survey gives the theory of current conveyor and its possible realizations along with advantages and disadvantages.

In the first part of chapter 2, several single input multiple output current mode

universal filters (SIMO) were proposed. The advantages and disadvantages of each filter were discussed. These filters were compared with the available circuits in the literature [50]. The comparison showed that the proposed circuits offer some advantages over the available ones. All the proposed filters use less number of active and passive components, no matching conditions required, use only grounded passive elements.

In the second part of chapter 2, a sinusoidal oscillator was presented. The frequency of oscillation and condition of oscillation were independently controllable and the input current was available at high impedance node. Only grounded passive elements were used. Comparison with previously published circuits [50][57] showed that it has the advantage of independent control and the output current was available at high impedance node.

In the third part of chapter 2, impedance simulation technique using current controlled conveyor was investigated. The circuits proposed can realize a non-ideal grounded capacitance multiplier. It could provide linear electronic tunability of its multiplication factor. The same circuit can also realize a grounded non-ideal 'frequency dependent negative resistance' (FDNR) and can also be extended to realize a floating C-multiplier. Comparison with the published circuits [60][69] showed that it has the advantage of higher bandwidth, and use of grounded capacitor for floating configuration.

In chapter 3, higher order filters were synthesized. Minimum number of components were used for the realization of filter. The filter offered more advantages than the work available in the literature [62]-[65]. For example less number of components, use of only grounded passive components. It can realize Chebyshev, Butterworth

and Elliptic filters.

To verify the theoretical analysis, all the proposed circuits were simulated using ICAPS simulation program. The simulation results were in good agreement with the theoretical ones.

4.2 Future Work

The presented work can be improved and further extended in many directions.

- Designing of multiple input single output (MISO) universal filter with less number of components and no matching conditions.
- Designing of simulation circuits of impedance like, floating FDNR, floating inductor with less number of components.
- Designing of (-R)(-L)(-C) parallel immittance simulator with independent control of circuit parameters.

Appendix A

The nth order current transfer function can be represented as [70],

$$\frac{I_o(s)}{I_{in}(s)} = \frac{A_n s^n + A_{n-1}s^{n-1} + \cdots + A_2 s^2 + A_1 s + A_o}{B_n s^n + B_{n-1}s^{n-1} + \cdots + B_2 s^2 + B_1 s + B_o} \quad (A.1)$$

$$= \frac{A_o s^{-n} + A_1 s^{-n+1} + \cdots + A_{n-1}s^{-1} + A_n}{s^{-n} + B_1 s^{-n+1} + \cdots + B_{n-1}s^{-1} + B_o} \quad (A.2)$$

The resulting signal flow graph (SFG) simulating equation (A.2) is shown in Figure A.1.

Feedback loop gains can be made equal to unity, without disturbing the transfer function of the SFG, if the gain of the branches coming towards the node of feedback loop is divided and the gain of the branches going away from the node of the feedback loop is multiplied by the gain of the feedback loop. This procedure is explained by an example in Figure A.2. Applying this technique to all the feedback loops, SFG of Figure A.3 is obtained.

The SFG of Figure A.3 can be changed to have self loops by applying the property shown in Figure A.4 [70]. For example if,

$$\frac{1}{1-g} = G$$

$$g = 1 - \frac{1}{G} \quad (A.3)$$

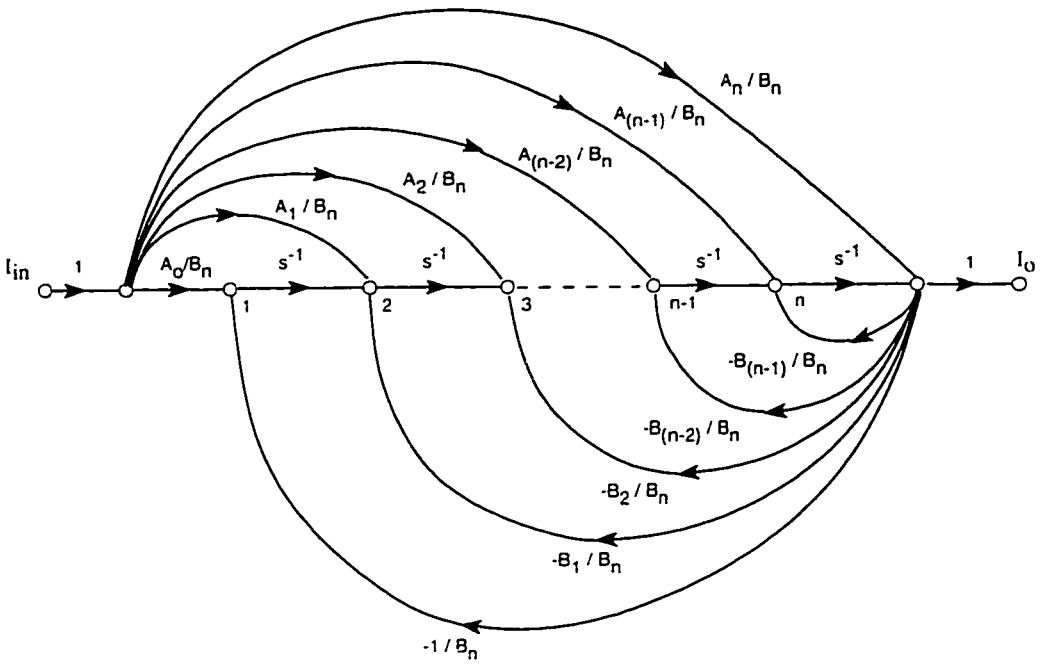


Figure A.1: n^{th} order signal flow graph.

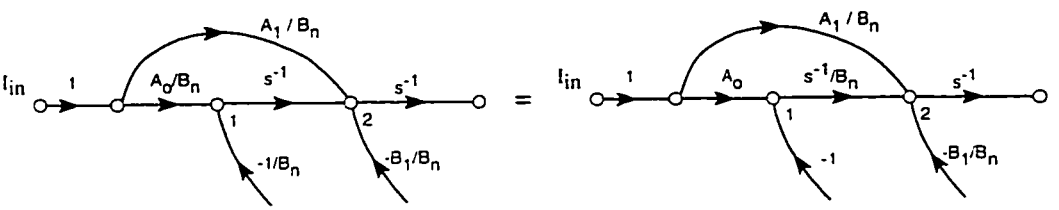


Figure A.2: Unity gain feedback loop subgraph.

The resulting signal flow graph is shown in Figure A.5.

Since transposition of signal flow graph does not change its transfer function. Figure A.5 can be transposed to get the required signal flow graph of Figure A.6.

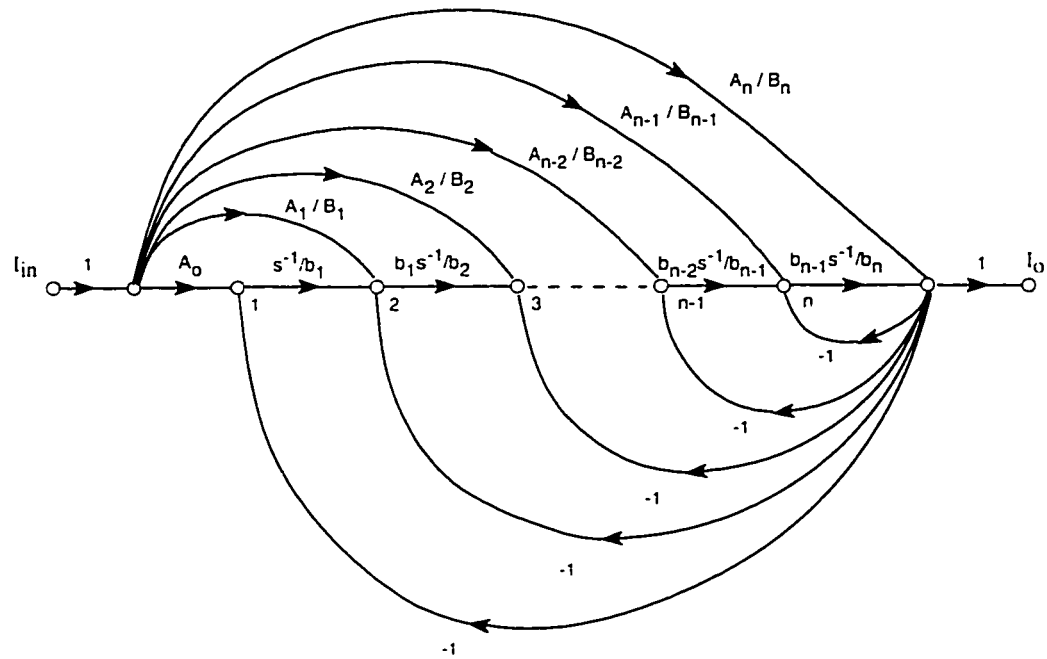


Figure A.3: n^{th} order unity gain signal flow graph.

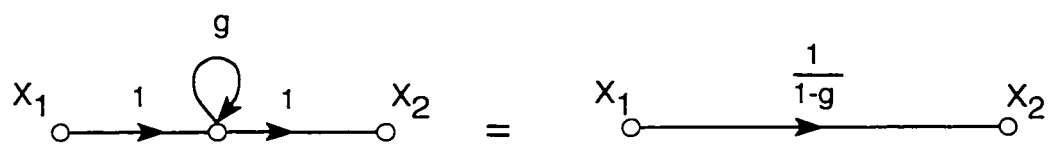


Figure A.4: Self loop transformation property.

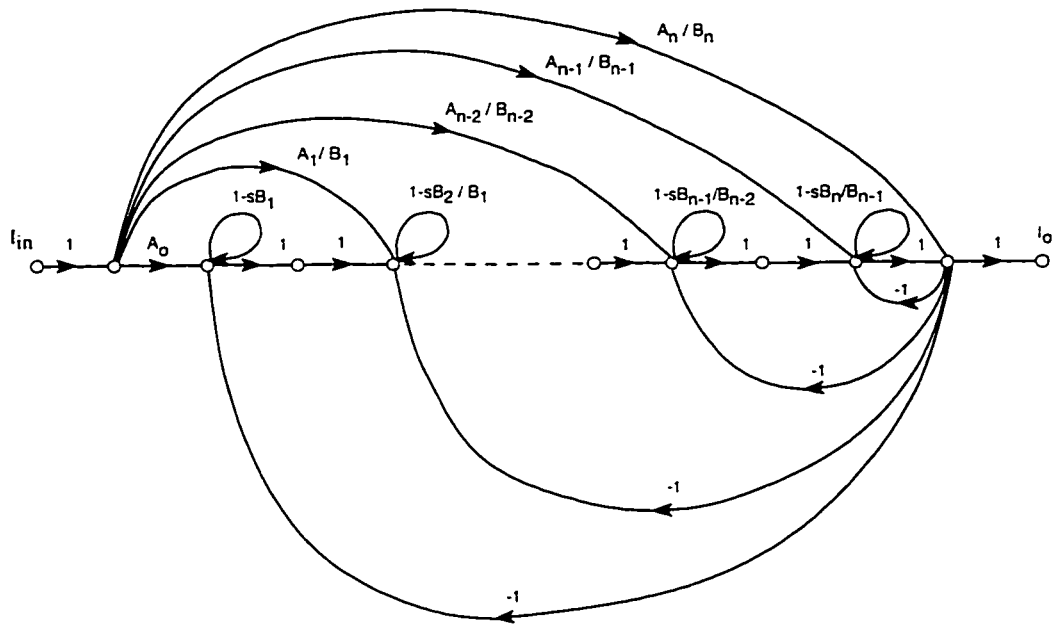


Figure A.5: n^{th} order signal flow graph with self loops.

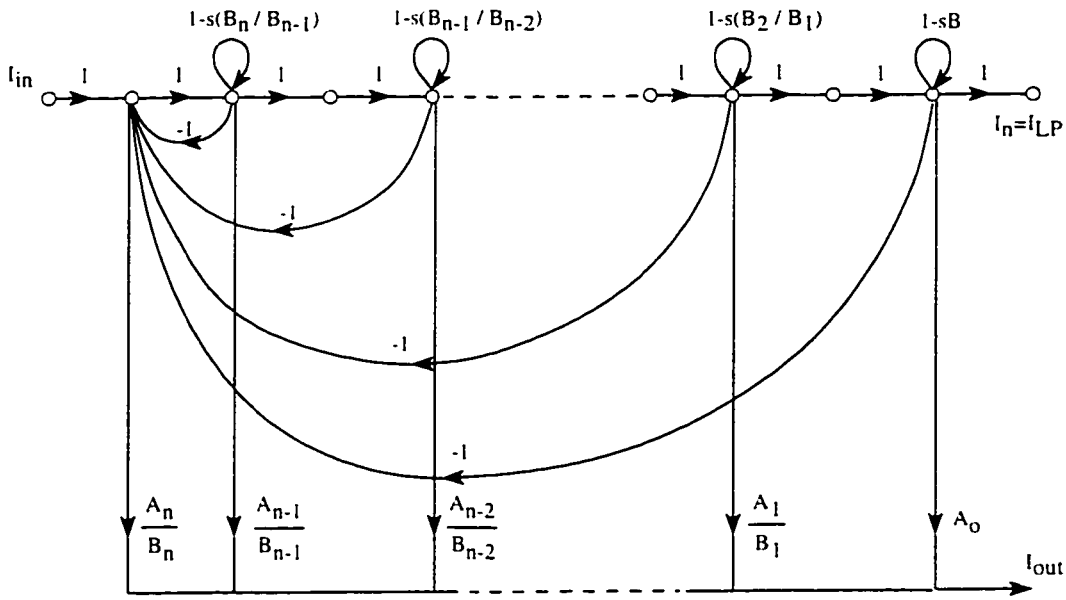


Figure A.6: n^{th} order signal flow graph obtained by transposition.

Appendix B

Proc. Natl. Sci. Counc. ROC(A)
Vol. 22, No. 3, 1998. pp 358-361

(Scientific Note)

Universal Current-Controlled Current-Mode Filters Using the Current Controlled Conveyor

MUHAMMAD TAHER ABUELMA'ATTI AND NOMAN ALI TASADDUQ

King Fahd University of Petroleum and Minerals
Dhahran, Saudi Arabia

(Received April 24, 1997; Accepted October 23, 1997)

ABSTRACT

A new current-mode universal filter is proposed. The filter uses three positive-type current controlled current-conveyors (CCCII+) and can simultaneously realize lowpass, highpass and bandpass responses. Realization of notch and allpass responses is feasible. The parameters ω_o, $\frac{\omega_o}{Q_o}$, and the bandpass gain can be controlled by adjusting the bias currents of the CCCIIs. The proposed circuit enjoys low sensitivities.

Key Words: filters, current conveyors

I. Introduction

Universal active filters using the operational transconductance amplifier (OTA) have many advantages, such as simplicity, integratability and programmability (Chang and Chen, 1991a; Nawrocki and Klein, 1986; Sanchez-Sinencio *et al.*, 1988; Wu and Xie, 1993; Sun and Fidler, 1993). However, they have some problems with dynamic range and at high frequencies of operation. On the other hand, current-mode current-conveyor based filters can offer wider signal bandwidths, greater linearity and larger dynamic ranges of operation (Sun and Fidler, 1994; Chang, 1991a, 1991b, 1993a, 1993b, 1993c; Roberts and Sedra, 1992; Chang *et al.*, 1993, 1994a, 1994b; Wu *et al.*, 1994; Senani, 1992). However, they lack programmability. While programmability can be achieved by combining current conveyors and OTAs (Horng *et al.*, 1995), the recently introduced second-generation current-controlled conveyor (CCCII) (Fabre *et al.*, 1996) allows current conveyor applications to be extended to the domain of electronically programmable functions. Electronic programmability of the CCCII is attributed to the dependence of the parasitic resistance at port X on the bias current of the current-conveyor. Figure 1(a) shows the electrical symbol of the CCCII+. Using two CCCII+ and two grounded capacitors, a voltage-mode bandpass filter was reported by Fabre *et al.* (1996), and a current-mode bandpass filter was also reported by Fabre *et al.* (1995). Moreover, all the CCII-based circuits employing one external resistance connected to port X can be replaced by CCCII-based circuits by exploiting, to advantage, the parasitic resistance at port X. Thus, the CCII-based circuit proposed by Fabre and Alami (1995) can be easily converted into a CCCII-based circuit employing only two externally connected grounded capacitances. The resulting circuit can simultaneously realize lowpass, highpass and bandpass transfer functions. However, the bandpass realization has a unity gain. Moreover, to sense the output-current of the bandpass transfer function, an additional current-conveyor, configured as a current-follower, is needed. Thus, one of the capacitors will not be

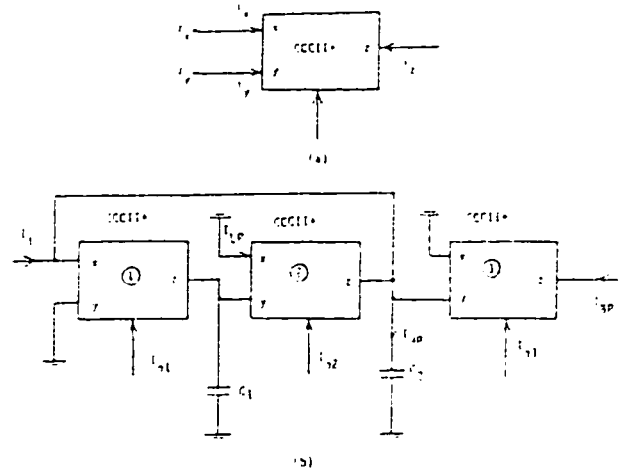


Fig. 1. (a) Electrical symbol of the CCCII+. (b) Proposed current-controlled current-mode universal filter.

grounded.

The major intention of this paper is to present a CCCII-based current-mode universal filter. Similar to the CCCII-based universal filter obtainable from the circuit proposed by Fabre and Alami (1995), the proposed circuit realizes unity-gain lowpass and highpass current transfer functions. However, in contrast with the circuit of Fabre and Alami (1995), the proposed circuit realizes a bandpass current transfer function with electronically programmable gain. Moreover, the output-current of the bandpass transfer function is obtained from a high impedance outlet. Thus, cascading, to realize a higher-order bandpass current transfer function, is feasible without using additional buffer circuits.

II. Proposed Circuit

The proposed circuit is shown in Fig. 1(b). It is worth mentioning here that, while the part of the circuit formed by CCCII-1, CCCII-2, C_1 and C_2 can be obtained by replacing the CCII and the series resistor at port X in the circuit of Fabre and Alami (1995) with a CCCII, the proposed circuit shown in Fig. 1(b) uses an additional CCCII to provide a high-impedance output bandpass current transfer function with electronically programmable gain while keeping the two capacitors grounded. These attractive features can not be obtained from the circuit of Fabre and Alami (1995).

Using standard notations, the CCCII+ can be characterised by $i_v=0$, $V_x=V_y+R_x i_x$ and $i_z=i_x$, where $R_x=\frac{V_T}{2I_o}$, V_T is the thermal voltage = 25.8 mV at 27 °C and I_o is the bias current of the CCCII+. Routine analysis, using Kirchhoff's current law (KCL) at the different nodes, yields the current transfer functions:

$$\frac{I_{BP}}{I_i} = -\frac{sR_{x1}R_{x2}C_1/R_{x3}}{s^2R_{x1}R_{x2}C_1C_2 + sR_{x2}C_1 + 1} \quad (1)$$

$$\frac{I_{LP}}{I_i} = \frac{1}{s^2R_{x1}R_{x2}C_1C_2 + sR_{x2}C_1 + 1} \quad (2)$$

and

$$\frac{I_{HP}}{I_i} = \frac{s^2R_{x1}R_{x2}C_1C_2}{s^2R_{x1}R_{x2}C_1C_2 + sR_{x2}C_1 + 1} \quad (3)$$

From Eqs. (1)-(3), the parameters ω_0 and $\frac{\omega_o}{Q_o}$ can be expressed as

$$\omega_o^2 = \frac{1}{R_{x1}R_{x2}C_1C_2} \quad (4)$$

and

$$\frac{\omega_o}{Q_o} = \frac{1}{R_{x1}C_2} \quad (5)$$

From Eqs. (1)-(3), it can be seen that the lowpass dc gain and the high frequency gain of the highpass are equal to unity while the bandpass gain at ω_0 equals

$$G_{BP} = \frac{R_{x1}}{R_{x3}} \quad (6)$$

From Eqs. (4)-(6), it can be seen that the parameter ω_0 can be adjusted by controlling the resistance R_{x2}, that is, the bias current I_{o2}, without disturbing the parameter $\frac{\omega_o}{Q_o}$ and the bandpass gain G_{BP}. Moreover, the bandpass gain can be adjusted by controlling the resistance R_{x3}, that is, the bias current I_{o3}, without disturbing the parameters ω_0 and $\frac{\omega_o}{Q_o}$. However, the parameter $\frac{\omega_o}{Q_o}$ can not be adjusted without disturbing the parameter ω_0 and the bandpass gain. A possible strategy for adjusting the parameters ω_0 and $\frac{\omega_o}{Q_o}$ and the bandpass gain is, therefore, as follows: first the resistance R_{x1}, that is, the bias current I_{o1}, is adjusted to control the parameter $\frac{\omega_o}{Q_o}$; then, the bias current I_{o2} is adjusted to control the parameter ω_0; finally, the bias current I_{o3} is adjusted to control the bandpass gain.

From Eqs. (1)-(3), it can also be seen that, by using two additional current followers to sense the currents I_{HP} and I_{LP}, a notch response can be realized by connecting the sensed I_{HP} and I_{LP} output terminals. An allpass response can be realized by connecting I_{BP} with the sensed I_{HP} and I_{LP} output terminals, provided that $R_{x1}=R_{x3}$, that is, $I_{o1}=I_{o3}$.

Taking into consideration the current-tracking error of the CCCII+, we find that $i_{zk}=\alpha_k i_{xk}$, where $\alpha_k=1-\varepsilon_k$, $|\varepsilon_k|<<1$ is the current-tracking error of the kth CCCII+. Reanalysis of the circuit shown in Fig. 1(b) yields the current transfer functions:

$$\frac{I_{BP}}{I_i} = -\frac{s\alpha_3R_{x1}R_{x2}C_1/R_{x3}}{s^2R_{x1}R_{x2}C_1C_2 + sR_{x2}C_1 + \alpha_1\alpha_2} \quad (7)$$

$$\frac{I_{LP}}{I_i} = \frac{\alpha_1\alpha_3}{s^2R_{x1}R_{x2}C_1C_2 + sR_{x2}C_1 + \alpha_1\alpha_2} \quad (8)$$

and

$$\frac{I_{HP}}{I_i} = \frac{s^2\alpha_3R_{x1}R_{x2}C_1C_2}{s^2R_{x1}R_{x2}C_1C_2 + sR_{x2}C_1 + \alpha_1\alpha_2} \quad (9)$$

From Eqs. (7)-(9), the parameter ω_0 can be expressed as

$$\omega_o^2 = \frac{\alpha_1\alpha_2}{R_{x1}R_{x2}C_1C_2}. \tag{10}$$

and $\frac{\omega_0}{Q_0}$ will be the same as in Eq. (5). From Eqs. (7)-(9), it can be seen that the lowpass dc gain is equal to $\alpha_1\alpha_2$, the high frequency gain of the highpass is equal to α_3 and the bandpass gain at ω_0 equals

$$G_{BP} = \alpha_3\frac{R_{x1}}{R_{x3}} \tag{11}$$

It is worth mentioning here that inclusion of the parasitic capacitances, C_y and C_z, at terminals Y and Z of the current-conveyors into the analysis will not affect the results obtained in Eqs. (1)-(10). In fact, these parasitic capacitances will be connected in parallel with the capacitances C_1 and/or C_2, and their effect can be easily compensated by subtracting their values from C_1 and/or C_2.

From Eqs. (5) and (10), it is easy to show that the active- and passive-sensitivities of the parameters ω_0 and Q_0 are

$$S_{R_{x1}}^{\omega_o} = S_{R_{x2}}^{\omega_o} = S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = S_{R_{x2}}^{Q_o} = S_{C_1}^{Q_o} = -S_{R_{x1}}^{Q_o} = -S_{C_2}^{Q_o}$$
$$= -S_{I_{o1}}^{\omega_o} = -S_{I_{o2}}^{\omega_o} = -S_{I_{o2}}^{Q_o} = S_{I_{o1}}^{Q_o} = -S_{\alpha_1}^{\omega_o} = -S_{\alpha_2}^{\omega_o}$$
$$= -S_{\alpha_1}^{Q_o} = -S_{\alpha_2}^{Q_o} = -\frac{1}{2}$$

and

$$S_{R_{x3}}^{\omega_o} = S_{R_{x3}}^{Q_o} = S_{I_{o3}}^{\omega_o} = S_{I_{o3}}^{Q_o} = S_{\alpha_3}^{\omega_o} = S_{\alpha_3}^{Q_o} = 0,$$

all of which are small.

III. Simulation Results

The universal filter circuit shown in Fig. 1(b) has been simulated using the ICAPS circuit simulation program. The CCCII+ has been simulated using the schematic implementation proposed by Fabre *et al* (1996) with dc supply voltage = ±2.5 V. The results obtained with C_1=1 nF, C_2=3 nF, $I_{o1}=I_{o3}$=300 μA and I_{o2}=50 μA are shown in Fig. 2. The parameter $f_o=\frac{\omega_0}{2\pi}$, calculated using Eq. (4), is 870.2 kHz. The parameter f_o, obtained from simulation results, is 812.8 kHz. The results obtained by means of simulation are in fairly good agreement with the presented theory. The difference is attributed to the parasitic capacitances of the current-conveyor. These capacitances will manifest themselves at high frequencies.

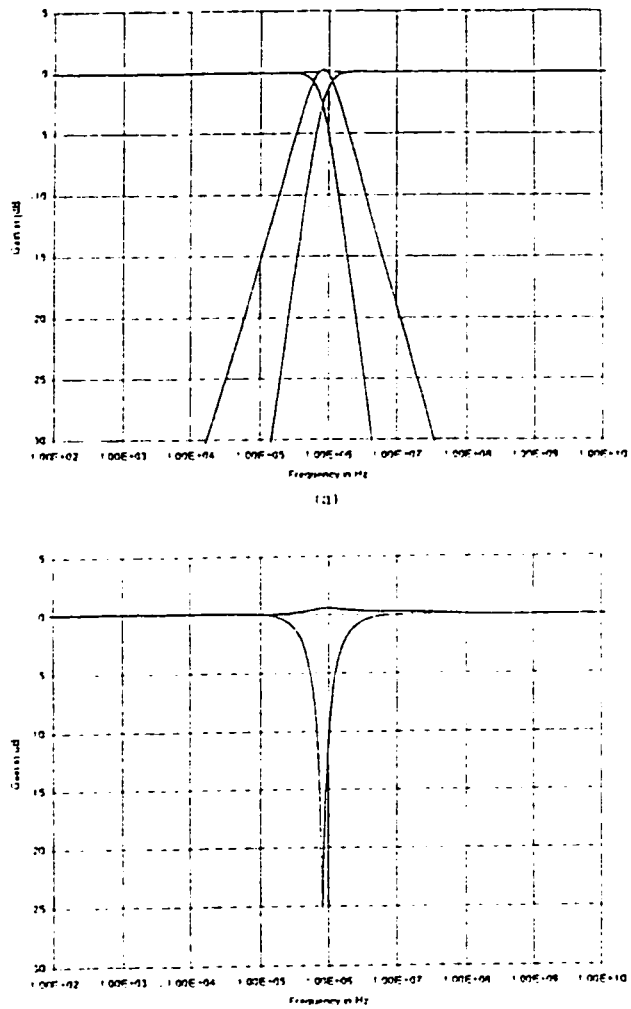


Fig. 2. Simulated results obtained from the circuit shown in Fig. 1(b) with C_1=1 nF, C_2=3 nF, $I_{o1}=I_{o3}$=300 μA, I_{o2}=50 μA, I_o=10 μA

IV. Conclusion

A new universal second-order current-mode filter has been presented. The proposed filter uses the current-controlled current-conveyor and enjoys the following advantages:

(1) current control of the parameters ω_0 and $\frac{\omega_0}{Q_0}$ of the filters and the gain of the bandpass filter;
(2) independent control of the parameter ω_0 without disturbing the parameter $\frac{\omega_0}{Q_0}$ or the bandpass gain;
(3) independent control of the bandpass gain without disturbing the parameters ω_0 and $\frac{\omega_0}{Q_0}$;
(4) low sensitivities of the parameters ω_0 and Q_0;

(5) the feasibility of realizing all the standard filter functions: lowpass, highpass, bandpass, notch and allpass.

References

Chang, C. M. (1991a) Universal active current filters using single second-generation current conveyor. *Electronics Letters*, 27, 1614-1617.

Chang, C. M. (1991b) Current mode allpass/notch and bandpass filter using single CCII. *Electronics Letters*, 27, 1812-1813.

Chang, C. M. (1993a) Universal active current filter with single input and three outputs using CCIIs. *Electronics Letters*, 29, 1932-1933.

Chang, C. M. (1993b) Novel universal current-mode filter with single input and three outputs using five current conveyors. *Electronics Letters*, 29, 2005-2006.

Chang, C. M. (1993c) Current-mode lowpass, bandpass and highpass biquads using two CCIIs. *Electronics Letters*, 29, 2020-2021.

Chang, C. M. and P. C. Chen (1991a) Universal active filter with current gain using OTAs. *International Journal of Electronics*, 71, 805-808.

Chang, C. M. and P. C. Chen (1991b) Universal active current filter with three inputs and one output using current conveyors. *International Journal of Electronics*, 71, 817-819.

Chang, C. M., C. C. Chien, and H. Y. Wang (1993) Universal active current filters using single second-generation current conveyor. *Electronics Letters*, 29, 1159-1160.

Chang, C. M., C. C. Chien, and H. Y. Wang (1994a) Universal active current filter with three inputs using current conveyors-Part 2. *International Journal of Electronics*, 76, 87-89.

Chang, C. M., S. H. Tu, and P. W. Tieh (1994b) Synthesis of analog signal filtering circuits using second-generation current conveyors. *Proceedings National Science Council, ROC(A)*, 18, 421-427.

Fabre, A. and M. Alami (1995) Universal current mode biquad implemented from two second generation current conveyors. *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, 42, 383-385.

Fabre, A., O. Saaid, F. Wiest, and C. Boucheron (1995) Current controlled bandpass filter based on translinear conveyors. *Electronics Letters*, 31, 1727-1728.

Fabre, A., O. Saaid, F. Wiest, and C. Boucheron (1996) High frequency applications based on a new current controlled conveyor. *IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications*, 43, 82-91.

Horng, J. W., M. H. Lee, and C. L. Hou (1995) Universal active filter using four OTAs and one CCII. *International Journal of Electronics*, 78, 903-906.

Nawrocki, R. and U. Klein (1986) New OTA-capacitor realization of a universal biquad. *Electronics Letters*, 22, 50-51.

Roberts, G. W. and A. S. Sedra (1992) A general class of current amplifier-based biquadratic filter circuits. *IEEE Transactions on Circuits and Systems*, 39, 257-263.

Sanchez-Sinencio, E., R. L. Geiger, and H. Navarez-Lozano (1988) Generation of continuous-time two integrator loop OTA filter structures. *IEEE Transactions on Circuits and Systems*, 35, 936-945.

Senani, R. (1992) New current-mode biquad filter. *International Journal of Electronics*, 73, 735-742.

Sun, Y. and J. K. Fidler (1993) Novel OTA-C realization of biquadratic transfer functions. *International Journal of Electronics*, 75, 333-340.

Sun, Y. and J. K. Fidler (1994) Versatile active biquad based on second generation current conveyors. *International Journal of Electronics*, 76, 91-98.

Wu, D. S., Y. S. Hwang, S. I. Liu, and Y. P. Wu (1994) New multifunction filter using an inverting CCII and a voltage follower. *Electronics Letters*, 30, 551-552.

Wu, J. and C. Y. Xie (1993) New multifunction active filter using OTAs. *International Journal of Electronics*, 74, 235-239.

使用電流控制傳輸器的泛用型電流模式濾波器

MUHAMMAD TAHER ABUELMA'ATTI AND NOMAN ALI TASADDUQ

King Fahd University of Petroleum and Minerals
Dhahran, Saudi Arabia

摘 要

本篇論文提出一個新型電流控制泛用型濾波器。此濾波器使用三個正型式電流控制電流傳輸器，可同時實現低通、高通、帶通、帶阻與全通響應，藉由調整電流傳輸器的偏壓電流可控制此濾波器的振盪頻率、頻寬與中頻增益。此外本論文所提出的電路具有低靈敏度的特性。

Bibliography

[1] Toumazou C., F. J. Lidgey, and D. Haigh. *Analogue IC Design: The Current-Mode Approach.* Peter Peregrinus, 1990.

[2] Toumazou C., F. J. Lidgey, and D. Haigh. Extending voltage-mode opamps to current-mode performance. *IEE Proceedings, Pt. G*, 137(2):116 130, 1990.

[3] Sedra A. S., G. W. Roberts, and F. Gohh. The current conveyors: history progress and new results. *IEE Proceedings, Pt. G*, 137(2):78 87, 1990.

[4] Roberts G. W. and A. S. Sedra. All current mode frequency selective circuits. *Electronics Letters*, 25(12):759 761, 1989.

[5] Geiger R. L. and E. Sanchez-Sinencio. Active filter design using operational transconductance amplifiers: a tutorial. *IEEE Circuits Devices Mag.*, 1(1):20 35, 1985.

[6] Ramirez-Angulo J., M. Robinson, and E. Sanchez-Sinencio. Current-mode continuous time filters: Two approaches. *IEEE Trans. Circuits Syst. II*, 39(6):337 341, 1992.

[7] Wu J. Current-mode high-order OTA-C filters. *Int. J. Electron.*, 74:1135 1139, 1994.

[8] Hughes J. B., I. C. Macbeth, and D. M. Pattullo. Switched current filters. *IEE Proceedings. Pt. G*, 137(2):156 162, 1990.

[9] Wilson B. Recent developments in current conveyors and current mode circuits. *IEE Proceedings. Pt. G*, 137(2):63 77, 1990.

[10] Smith K. C. and A. Sedra. The current conveyor: a new circuit building block. *Proc. IEEE*, 56:1368 1369, 1968.

[11] Smith K. C. and A. Sedra. A second generation current conveyor and its applications. *IEEE Trans.*, CT-17:132 134, 1970.

[12] Fabre A. Third-generation current conveyor: a new helpful active element. *Electronics Letters*, 31(5):338 339, 1995.

[13] Sharif-Bakhtiar M. and P. Aronhime. A current conveyor realization using operational amplifiers. *Int. J. Electron.*, 45:283 288, 1978.

[14] Senani R. Novel circuit implementation of current conveyors using an OA and an OTA. *Electronics Letters*, 16(1):2 3, 1980.

[15] Wilson B. Low distortion feedback voltage-current conversion technique. *Electronics Letters*, 17(4):157 159, 1981.

[16] Wilson B. High-performance current conveyor implementation. *Electronics Letters*, 20(24):990 991, 1984.

[17] Lidgey F. J. and C. Toumazou. Floating impedance convertors using current conveyors. *Electronics Letters*, 21(15):640 642, 1985.

[18] Wilson B. Floating FDNR employing a new CCII conveyor implementation. *Electronics Letters*, 21(21):996 997, 1985.

[19] Toumazou C. and F. J. Lidgey. Universal active filter using current conveyors. *Electronics Letters*, 22(12):662 664, 1986.

[20] Carloswa A. and Moschytz G. S. Design of variable-gain current conveyors. *IEEE Trans. Circuits Syst. I*, 41(1):79 81, 1994.

[21] Gilbert B. A new wide-band amplifier technique. *IEEE J. Solid-State Circuits*, SC3:353 365, 1968.

[22] Fabre A. and M. Alami. A versatile translinear cell-library to implement high performance analog ASICs. *Proceedings EUROASIC'90 Conf., Paris*, pages 89 94, 1990.

[23] Gilbert B. Translinear circuits: A proposed classification. *Electronics Letters*, 11:14 16, 1975.

[24] Gilbert B. Translinear circuits-25 years on, part I: the foundations. *Electronic Engineering*, pages 21 24, 1993.

[25] Palmer W. Transimpedance amplifiers: fast yet accurate. *Electron.*, pages 151 156, 1988.

[26] Fabre A. Analysis of analogue circuit implementations from translinear blocks. *IEE Proceedings, Pt. G*, 138:483 491, 1991.

[27] Fabre A. Dual translinear voltage/current convertor. *Electronics Letters*, 19:1030 1031, 1983.

[28] Fabre A. Ultra low distortion current conversion technique. *Electronics Letters*, 20:674–676, 1984.

[29] Fabre A. Wideband translinear current convertor. *Electronics Letters*, 20:241–242, 1984.

[30] Fabre A. Current processing circuits with translinear operational current amplifiers. *Int. J. Electron.*, 63:9–28, 1987.

[31] Normand G. Translinear current conveyors. *Int. J. Electron.*, 59:771–777, 1985.

[32] Fabre A. Translinear current conveyors implementation. *Int. J. Electron.*, 59:619–623, 1985.

[33] Fabre A., F. Dayoub, L. Duruisseau, and M. Kamoun. High input impedance insensitive second-order filters implemented from current conveyors. *IEEE Trans. Circuits and Syst.-I*, 41(12):918–921, 1994.

[34] Surakampontorn N. Integrable wide dynamic range negative resistance circuits. *Electronics Letters*, 21:506–508, 1985.

[35] Fabre A. and P. Rochedgude. Performance comparisons of a new negative impedance converter with a translinear implementation. *Int. J. Electron.*, 62:341–345, 1987.

[36] Fabre A., O. Saaid, F. Wiest, and C. Boucheron. High frequency applications based on a new current controlled conveyor. *IEEE Trans. Circuits and Syst.-I*, 43(2):82–91, 1996.

[37] Fabre A. Bidirectional current-controlled PTAT current source. *IEEE Tran. on Circuits and Syst.-I*, 41(12), 1994.

[38] Nawrocki R. and U. Klein. New OTA-capacitor realization of a universal biquad. *Electronics Letters*, 22(1):50 51, 1986.

[39] Geiger R. L. and E. Sanchez-Sinencio. Active filter design with operational transconductance amplifiers: a tutorial. *IEEE Circuits and Devices Mag.*, 1(2):20 32, 1985.

[40] Chang C. and P. C. Chen. Universal active current filter with current gain using OTAs. *Int. J. Electron.*, 71:805 808, 1991.

[41] Wu J. and C. Y. Xie. New multifunction active filter using OTAs. *Int. J. Electron.*, 74:235 239, 1993.

[42] Sun Y. and J. K. Fidler. Novel OTA-C realization of biquadratic transfer functions. *Int. J. Electron.*, 75:333 340, 1993.

[43] Bowron P., K. A. Mezher, and H. W. Ng. A performance assessment of audio filters using current-mode analogue devices. *IEE Saraga Colloqium on Digital and Anologue Filters*, 226:15/1 15/4, 1995.

[44] Bowron P., K. A. Mezher, and A. A. Muhieddine. A re-appraisal of OTA-C circuits as continuous-time filters. *IEE Saraga Colloqium on Digital and Anologue Filters*, pages 8/1 8/5, 1994.

[45] Fabre A. and M. Alami. Insensitive current-mode biquad implementation based translinear current conveyors. *IEEE Proc. EUROASIC'92 Conf.*, pages 126 130, 1992.

[46] Chang C. M. and P. C. Chen. Universal active current filter with three inputs and one output using current conveyors. *Int. J. Electron.*, 75:897 901, 1991.

[47] Chang C. M. Universal active current filters using second generation current conveyors. *Electronics Letters*, 27:1614 1617, 1991.

[48] Liu S. I., J. H. Kuo, and J. H. Tsay. New CCII based current-mode biquadratic filters. *Int. J. Electron.*, 72:243 252, 1992.

[49] Chang C. M., C. C. Chien, and H. Y. Wang. Universal active current filters using single second generation current conveyor. *Electronics Letters*, 29:1159 1160, 1993.

[50] Kiranon W., J. Kesorn, W. Sangpisit, and N. Kamprasert. Electronically tunable multifunctional translinear-C filter and oscillator. *Electronics Letters*, 33(7):573 574, 1997.

[51] Abuelma'atti M. T., A. A. Al-Ghumaiz, and M. H. Khan. Novel CCII- based single-element controlled oscillators employing grounded resistors and capacitors. *Int. J. Electron.*, 78(6):1107 1112, 1995.

[52] Abuelma'atti M. T. Two minimum component CCII-based RC oscillators. *IEEE Trans. Circuits and Syst.-I*, 34:980 981, 1987.

[53] Abuelma'atti M. T. Minimal realization for single resistor controlled sinusoidal oscillator using single CCII. *Electronics Letters*, 28:1264 1265, 1992.

[54] Celma S., P. A. Martinez, and I. Gutierrez. Generation of current conveyor based sinusoidal oscillators for integrated circuits. *Microelectronics Journal*, 25:407 414, 1994.

[55] Chang C. M. Novel current conveyor based single-resistance-controlled/voltage-controlled oscillator employing grounded resistors and capacitors. *Electronics Letters*, 30:181–183, 1994.

[56] Linares-Barranco B. and A. Rodriguez-Vazquez. Generation and design of sinusoidal oscillators using OTAs. *Proc. IEEE/ISCAS*, 3:2863–2866, 1988.

[57] Kiranon W., J. Kesorn, and P. Wardkein. Current controlled oscillator based on translinear conveyors. *Electronics Letters*, 32(15):1330–1331, 1996.

[58] Leonard T. Bruton. *RC-Active circuits: Theory and design.* Prentice-Hall.

[59] Wai-Kai Chen. *Passive and active filters: Theory and implementation.* John Wiley and sons.

[60] Ahmed M. T., I. A. Khan, and N. Minhaj. Novel electronically tunable C-multipliers. *Electronics Letters*, 31(1), 1995.

[61] Kiranon W. and P. Pawarangkoon. Floating inductance simulation based on current conveyors. *Electronics Letters*, 33(21):1748–1749, 1997.

[62] Acar C. Nth-order voltage transfer function synthesis using a commercially available active component: signal-flow graph approach. *Electronics Letters*, 32(21):1933–1932, 1996.

[63] Acar C. and S. Ozoguz. High-order voltage transfer function synthesis using CCII+ based unity gain current amplifiers. *Electronics Letters*, 32(22):2030–2031, 1996.

[64] Gunes E. O. and F. Anday. Realisation of current-mode low pass filters using CFCCIIs. *Electronics Letters*, 31(25):2161 2162, 1995.

[65] Jie Wu. Current-mode high-order OTA-C filters. *Int. J. Electron.*, 76(6):1115 1120, 1994.

[66] Abuelma'atti M. T. and N. A. Tasadduq. Universal current-controlled current-mode filters using the current controlled conveyor. *Proc. Natl. Sci. Counc.*, 22(3):358 361, 1998.

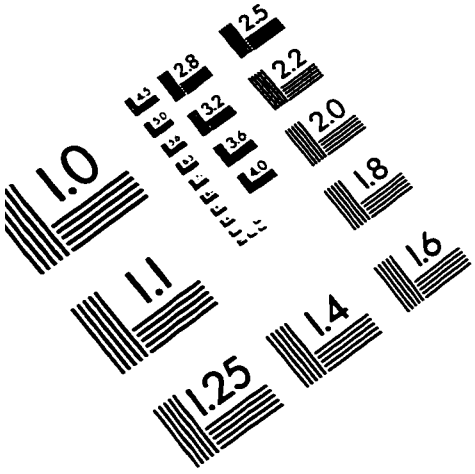
[67] Frey D. R. Log domain filtering: an approach to current-mode filtering. *IEE Proceedings, Pt. G*, 140(6):406 416, 1993.

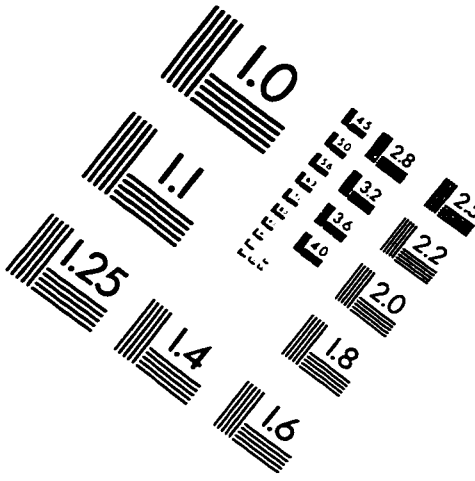
[68] Jack Winzer. *Linear integrated circuits*. Saunders College Publishing, 1992.

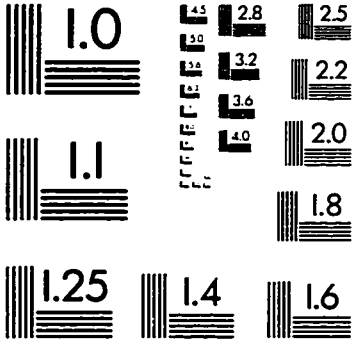
[69] Khan I.A. and M. T. Ahmed. OTA-based integrable voltage/current-controlled ideal C-multiplier. *Electronics Letters*, 22(7), 1986.

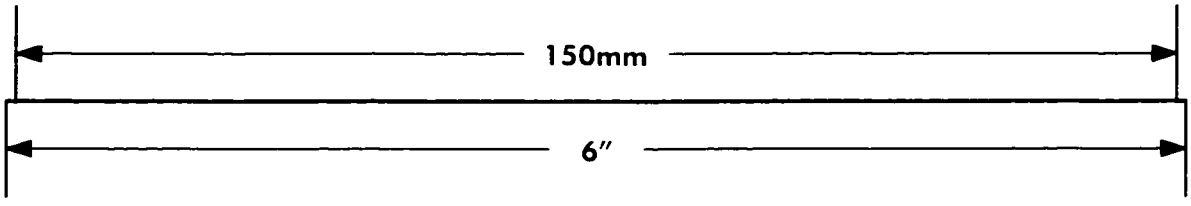
[70] Robichaud P. A., Boisvert M., and Robert J. *Signal flow graph and applications*. Prentice Hall.

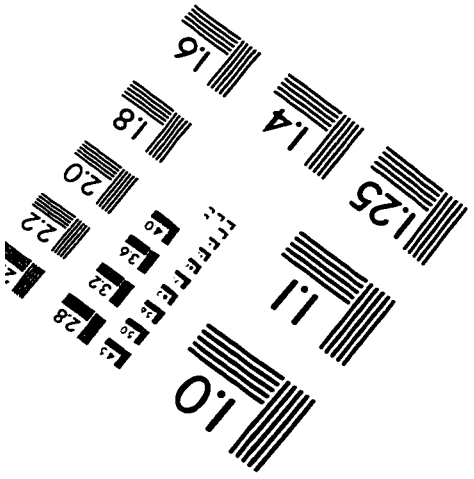
IMAGE EVALUATION
TEST TARGET (QA-3)

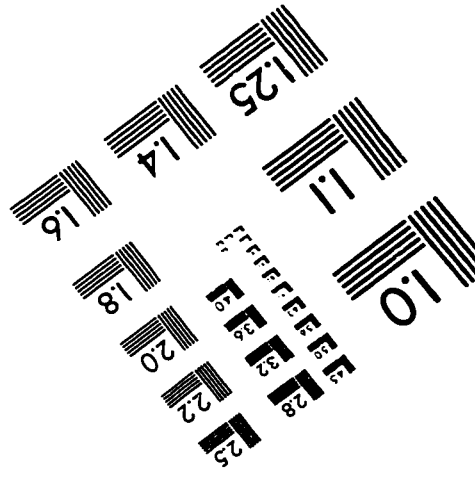












APPLIED IMAGE, Inc
1653 East Main Street
Rochester, NY 14609 USA
Phone: 716/482-0300
Fax: 716/288-5989