Hardware Design And VLSI Implementation Of A Byte-Wise CRCgenerator Chip

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Summary

The hardware design and VLSI implementation of a byte-wise CRC generator is presented. The algorithm is based on the work presented by Perez, Wismer and Becker (1983) in which a software implementation was proposed. The byte-wise CRC algorithm is translated to hardware and pressed in APHL (VLSI design automation language). The method used calculates CRC `on the fly' and is much faster then the look-up table method proposed by Lee (1981). The chip is 8 times faster than the serial implementation of Sait and Khan (see ibid., vol. 39, no.4, p.911-910, 1993) with smaller hardware requirements (occupies lesser area). The number of clock cycles required to generate and transmit any CRC (for an 8 byte message) is just two more than the time required to calculate it (in all 10 clock pulses). The CRC chip can be used in a number of applications. These include areas such as error detection and correction in data communications, signature analysis, and mass storage devices for parallel information transfers