Generic DFT Approach For Pattern Sensitive Faults In Word-Orientedmemories

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Summary

The testability problem of word-oriented memories (WOMs) for pattern sensitive faults is addressed. A novel design for testability (DFT) strategy allows efficient built-in self-testing (BIST) of WOMs. By proper selection of the memory array tiling scheme, it is possible to implement O(n) BIST algorithms which test WOMs for various types of neighbourhood pattern sensitive faults (NPSFs). The inputs of the column decoders are modified to allow parallel writing into multiple words, and coincidence comparators are added to allow parallel verification of row data with minimal effect on chip area and performance

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