Design, Selection And Implementation Of Flash Erase EEPROM Memorycells

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Summary

The author reports an investigation into the design and process constraints of flash EEPROM memory cells. He describes several possible structures which were developed by the MOS memory RD group of National Semiconductor Corporation at West Jordan, Utah. These structures were implemented and tested on a specially designed test chip. In addition to the typical structures of poly 1 floating gate and poly 2 control gate, new novel structures of poly 2 floating gate and poly 1 control gate were implemented. A total of five major structures are described. The author discusses the principle of operation, advantages and disadvantages of each of these structures. Also included are characteristic results and a discussion of the performance of these candidate cells