DFT For Controlled-Impedance I/O Buffers

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Summary

This paper presents an architecture that enhances the testability of controlled-impedance buffers (CIBs). By testing CIBs digitally, the new architecture overcomes most of the problems with the traditional testing method. Most of these problems are test cost related. While reducing the test cost, the new architecture allows for higher test quality that even includes delay testing capabilities.

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