Efficient O(N) BIST Algorithms For DDNPS Faults In Dual Portmemories

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Summary

The testability problem of dual port memories is investigated. Architectural modifications which enhance testability with minimal overhead on both silicon area and device performance are described. New fault models for both the memory array and the address decoders are proposed and efficient O(n) test algorithms are presented. The new fault models account for the simultaneous dual access property of the device. In addition to the classical static neighborhood pattern sensitive faults, the array test algorithm covers a new class of pattern sensitive faults, Duplex Dynamic Neighborhood Pattern Sensitive faults (DDNPSF)

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