A Static Test Compaction Technique For Combinational Circuits Based On Independent Fault Clustering

Osais, Y.E. El-Maleh, A.H.; Dept. of Comput. Eng., King Fahd Univ. of Pet. & Miner., Dhahran, Saudi Arabia;

Electronics, Circuits and Systems, 2003. ICECS 2003. Proceedings of the 2003 10th IEEE International conference;Publication Date: 14-17 Dec. 2003;Vol: 3,On page(s): 1316- 1319 Vol.3;ISBN: 0-7803-8163-7

King Fahd University of Petroleum & Minerals

http://www.kfupm.edu.sa

Summary

Testing system-on-chip involves applying huge amounts of test data, which is stored in the tester memory and then transferred to the circuit under test during test application. Therefore, practical techniques, such as test compression and compaction, are required to reduce the amount of test data in order to reduce both the total testing time and the memory requirements for the tester. In this paper, a new static compaction algorithm for combinational circuits is presented. The algorithm is referred to as independent fault clustering. It is based on a new concept called test vector decomposition. Experimental results for benchmark circuits demonstrate the effectiveness of the new static compaction algorithm.

For pre-prints please write to:abstracts@kfupm.edu.sa

© Copyright: King Fahd University of Petroleum & Minerals;
http://www.kfupm.edu.sa